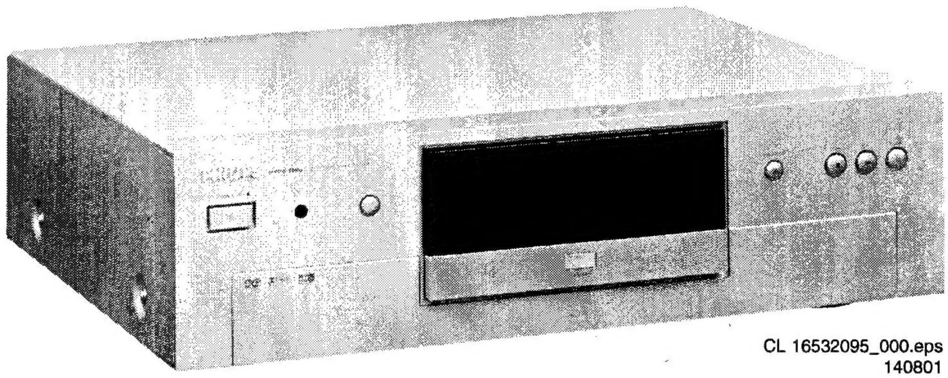
DVD-Video Recorder **DVDR1000**

/001 /021 /051 /691

Service Service Service



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Service Manual

CLASS 1
LASER PRODUCT

DVD+ReWritable

DVD VIDEO

COMPACT disc DIGITAL VIDEO

COMPACT disc DIGITAL AUDIO

Contents

Contents

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PHILIPS

1. Technical Specifications and Connection Facilities

1.1 General:

Mains voltage	:	230V (198 -264V AC) for Europe/Asia
Mains frequency	:	50 Hz - 60Hz
Power consumption mains	:	< 32 W
Power consumption standby	:	< 7 W
Power consumption low power stand-by	:	< 3 W

1.2 RF Tuner

Test equipment:Fluke 54200 TV Signal generator
Test streams:PAL BG Philips Standard test pattern

1.2.1 System:

PAL B/G, PAL D/K, SECAM L/L', PAL I

1.2.2 RF - Loop Through:

Frequency range	:	45 MHz - 860 MHz
Gain: (ANT IN - ANT OUT)	:	-4 dB /±2 dB

1.2.3 Radio Interference:

input voltage /3 tone method (+40 dB min)	:	typ. 80 dBμV at 75Ω

1.2.4 Receiver:

PLL tuning with AFC for optimum reception

Frequency range:	:	45.25 MHz - 860 MHz
Sensitivity at 40 dB S/N	:	≥ 60dBμV at 75Ω (video unweighted)

1.2.5 Video Performance:

Channel 25 / 503,25 MHz,
Test pattern: PAL BG PHILIPS standard test pattern,
RF Level 74 dBV
Measured on SCART 1

Frequency response:	:	1 MHz - 4.00 MHz ± 2 dB
Group delay (0.1 MHz - 4.4 MHz)	:	0 nsec ± 30 nsec

1.2.6 Audio Performance:

Audio Performance Analogue - HiFi:

Frequency response at SCART 1 (L+R) output:	:	40 Hz - 15 kHz / ± 1.5 dB
S/N according to DIN 45405, 7, 1967	:	
and PHILIPS standard test pattern video signal:	:	-50 dB unweighted
Harmonic distortion (1 kHz, ± 25 kHz deviation):	:	0.5 %

Audio Performance NICAM:

Frequency response at SCART 1(L+R) output:	:	40 Hz - 15 kHz ± 1.5 dB
S/N according to DIN 45405, 7, 1967	:	
and PHILIPS standard test pattern video signal:	:	-60 dB unweighted
Harmonic distortion (1 kHz):	:	0.1 %

1.2.7 Tuning

Automatic Search Tuning

scanning time without antenna	:	2.5 min. PAL
stop level (vision carrier)	:	75 V, 75
Maximum tuning error of a recalled program	:	± 62.5 kHz
Maximum tuning error during operation	:	± 100 kHz

Tuning Principle
automatic B,G, I, DK and L/L'detection
manual selection in "STORE" mode

1.3 Analogue Inputs

1.3.1 SCART II (Connected to TV)

Pin Signals:

1 - Audio R	1.8V RMS	
2 - Audio R		
3 - Audio L	1.8V RMS	
4 - Audio GND		
5 - Blue/Chroma GND		
6 - Audio L		
7 - Blue out/ Chroma in	0.7Vpp ± 0.1V into 75 Ohm (*)	
8 - Function switch	<2V = TV >4.5V / <7V = asp. ratio 16:9 DVD >9.5V / <12V = asp. ratio 4:3 DVD	
9 - Green GND		
10- P50 control		
11- Green	0.7Vpp ± 0.1V into 75 Ohm (*)	
12- Nc		
13- Red/Chroma GND		
14- fast switch GND		
15- Red out/ Chroma out	0.7Vpp ± 0.1V into 75 Ohm (*) ± 3dB 0.3Vpp Chroma (burst)	
16- fast switch RGB/ CVBS	or Y <0.4V into 75 Ohm = CVBS >1V / <3V into 75 Ohm = RGB	
17- Y/CVBS GND		
18- fast switching GND		
19- CVBS/Y/RGB sync	1Vpp ± 0.1V into 75 Ohm (*)	
20- CVBS/Y		
21- Shield		

1.3.2 SCART I (Connected to AUX)

Pin Signals:

1 - Audio R	1.8V RMS	
2 - Audio R		
3 - Audio L	1.8V RMS	
4 - Audio GND		
5 - Blue/Chroma GND		

6 - Audio L		
7 - Blue in/ Chroma out	± 3dB 0.3Vpp Chroma (burst)	
8 - Function switch		
9 - Green GND		
10- P50 control		
11- Green		
12- Nc		
13- Red/Chroma GND		
14- fast switch GND		
15- Red in/ Chroma in		
16- fast switch RGB/ CVBS or Y		
17- CVBS GND		
18- fast switching GND		
19- CVBS/Y/RGB sync	1Vpp ± 0.1V into 75 Ohm (*)	
20- CVBS/Y		
21- Shield		

(*) for 100% white

1.3.3 Audio/Video Front Input Connectors

Audio

Input voltage	: 2 Vrms
Input impedance	: >10kΩ

Video - Cinch

Input voltage	: 1 Vpp ± 0.1V
Input impedance	: 75 Ω

Video - YC (Hosiden)

Input voltage Y	: 1Vpp ± 0.1V
Input impedance Y	: 75 Ω
Input voltage C	: burst 300 mVpp ± {x} dB
Input impedance C	: 75 Ω

1.3.4 Cinch Audio/Video Line Input Rear

Audio (EXT1)

Input voltage	: 2 Vrms
Input impedance	: >10k Ω

Video (EXT4)

Input voltage	: 1 Vpp ± 0.1V
Input impedance	: 75 Ω

1.3.5 YC Input Rear (Hosiden; EXT3)

1 - GND	
2 - GND	
3 - Input voltage Y	1Vpp ± 0.1V/ 75 Ω
4 - Input voltage C	Burst 300 mVpp ± {x} dB/ 75 Ω

1.4 Video Performance

All outputs loaded with 75 Ohm
SNR measurements over full bandwidth without weighting.

1.4.1 CVBS Output Rear (EXT4)

SNR Luminance	: > -65 dB
SNR Chrominance AM	: > -65 dB
SNR Chrominance PM	: > -65 dB
Bandwidth Luminance	: 5 MHz ± 1 dB

1.4.2 YC Output Rear (Hosiden ; EXT3)

SNR	: > -65 dB
SNR C - AM	: > -65 dB
SNR C - PM	: > -65 dB
Bandwidth Y	: 5 MHz ± 1 dB

1.4.3 SCART (RGB)

SNR	: > -65 dB on all output
Bandwidth	: 5 MHz ± 1 dB

1.5 Audio Performance

1.5.1 Cinch Output Rear

Output voltage 2 channel mode	: 2Vrms ± 1.5dB
Output voltage 5.1 channel Dolby	: 1.41Vrms ± 1.5dB
Channel unbalance (1kHz)	: <0.85dB
Crosstalk 1kHz	: >105dB
Crosstalk 20Hz-20kHz	: > 95dB
Frequency response 20Hz- 20kHz	: ± 0.1dB max
Signal to noise ratio	: >100 dB
Dynamic range 1kHz	: >90dB
Dynamic range 20Hz-20kHz	: >88dB
Distortion and noise 1kHz	: >90dB
Distortion and noise20Hz-20kHz	: >80dB
Intermodulation distortion	: >87dB
Phase non linearity	: ± 1° max.
Level non linearity	: ± 0.5dB max.
Mute (spin-up, pause, access)	: >100dB
Outband attenuation:	: > 50dB above 25kHz

1.5.2 Scart Audio

Output voltage 2 channel mode	: 2Vrms ± 1.5dB
Output voltage 5.1 channel Dolby	: 1.41 Vrms ± 1.5dB
Channel unbalance (1kHz)	: <0.85dB
Crosstalk 1kHz	: >105dB
Crosstalk 20Hz-20kHz	: > 95dB
Frequency response 20Hz- 20kHz	: ± 0.1dB max
Signal to noise ratio	: >100 dB
Dynamic range 1kHz	: >90dB
Dynamic range 20Hz-20kHz	: >88dB
Distortion and noise 1kHz	: >90dB
Distortion and noise20Hz-20kHz	: >80dB
Intermodulation distortion	: >87dB
Phase non linearity	: ± 1° max
Level non linearity	: ± 0.5dB max
Mute (spin-up, pause, access)	: >100dB
Outband attenuation:	: > 50dB above 25kHz

1.6 Digital Output

1.6.1 Coaxial

CDDA/ LPCM (incl MPEG1)	: according IEC958
MPEG2, AC3 audio	: according IEC1937
DTS	: according IEC1937, amendment 1

1.6.2 Optical

identical to coaxial

1.7 Digital Video Input (IEEE 1394)

1.7.1 Applicable Standards

Implementation according:
IEEE Std 1394-1995
IEC 61883 - Part 1
IEC 61883 - Part 2 SD-DVCR (02-01-1997)
Specification of consumer use digital VCR's using 6.3 mm magnetic tape - dec.1994
Mechanical connection according:
Annex A of 61883-1

1.7.2 Audio Quality

Output voltage 2 channel mode	:	2Vrms +/- 1.5dB
Channel unbalance (1kHz)	:	Tbd
Crosstalk 1kHz	:	> 95 dB
Crosstalk 20Hz-20kHz	:	> 95 dB
Frequency response 20Hz- 12kHz	:	+/- 0.2dB max
Signal to noise ratio	:	>85 dB
Dynamic range 1kHz	:	tbd
Dynamic range 20Hz-20kHz	:	Tbd
Distortion and noise 1kHz	:	>75dB
Distortion and noise 20Hz-20kHz	:	>75dB
Intermodulation distortion	:	>80dB
Phase non linearity	:	tbd
Level non linearity	:	tbd
Mute (spin-up, pause, access)	:	tbd
Outband attenuation	:	tbd

1.8 P50 System Control

Via SCART pin nr 10

1.9 Dimensions and Weight

Place and height of feet	:	acc. to Philips Harmonisation line
Apparatus tray closed	:	WxDxH :435 x 330 x 110
Apparatus tray open	:	WxDxH :435 x 470 x 110
Weight without packaging	:	ca. 8.8 Kg ± 0.5 kg
Weight in packaging	:	ca. Tbc (>9 Kg)

1.10 Laser Output Power & Wavelength

1.10.1 DVD

Output power during reading	:	0.8mW
Output power during writing	:	20mW
Wavelength	:	660nm

1.10.2 CD

Output power	:	0.3mW
Wavelength	:	780nm

2. Warnings And Laser Safety Instructions

GB **WARNING**

All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD).
Careless handling during repair can reduce life drastically.
When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.
Keep components and tools also at this potential.

ESD

NL **WAARSCHUWING**

Alle IC's en vele andere halfgeleiders zijn gevoelig voor elektrostatische ontladingen (ESD).
Onzorgvuldig behandelen tijdens reparatie kan de levensduur drastisch doen verminderen.
Zorg ervoor dat u tijdens reparatie via een polsband met weerstand verbonden bent met hetzelfde potentiaal als de massa van het apparaat.
Houd componenten en hulpmiddelen ook op ditzelfde potentiaal.

F **ATTENTION**

Tous les IC et beaucoup d'autres semi-conducteurs sont sensibles aux décharges statiques (ESD).
Leur longévité pourrait être considérablement écourtée par le fait qu'aucune précaution n'est prise a leur manipulation.
Lors de réparations, s'assurer de bien être relié au même potentiel que la masse de l'appareil et enfiler le bracelet serti d'une résistance de sécurité.
Veiller a ce que les composants ainsi que les outils que l'on utilise soient également a ce potentiel.

D **WARNUNG**

Alle IC und viele andere Halbleiter sind empfindlich gegen elektrostatische Entladungen (ESD).
Unsorgfältige Behandlung bei der Reparatur kann die Lebensdauer drastisch vermindern.
Sorgen sie dafür, das Sie im Reparaturfall über ein Pulsarmband mit Widerstand mit dem Massepotential des Gerätes verbunden sind.
Halten Sie Bauteile und Hilfsmittel ebenfalls auf diesem Potential.

I **AVVERTIMENTO**

Tutti IC e parecchi semi-conduttori sono sensibili alle scariche statiche (ESD).
La loro longevita potrebbe essere fortemente ridatta in caso di non osservazione della piu grande cauzione alla loro manipolazione.
Durante le riparazioni occorre quindi essere collegato allo stesso potenziale che quello della massa dell'apparecchio tramite un braccialetto a resistenza.
Assicurarsi che i componenti e anche gli utensili con quali si lavora siano anche a questo potenziale.

GB

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

NL

Veiligheidsbepalingen vereisen, dat het apparaat in zijn oorspronkelijke toestand wordt terug gebracht en dat onderdelen, identiek aan de gespecifieerde worden toegepast.

D

Bei jeder Reparatur sind die geltenden Sicherheitsvorschriften zu beachten.
Der Originalzustand des Gerats darf nicht verandert werden.
Fur Reparaturen sind Original-Ersatzteile zu verwenden.

I

Le norme di sicurezza esigono che l'apparecchio venga rimesso nelle condizioni originali e che siano utilizzati pezzi di ricambiago idetici a quelli specificati.

F

Les normes de sécurité exigent que l'appareil soit remis a l'état d'origine et que soient utilisées les pièces de rechange identiques à celles spécifiées.

SHOCK, FIRE HAZARD SERVICE TEST:

CAUTION: After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom,
Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before return to user/customer.
Ref.UL Standard NO.1492.

NOTE ON SAFETY:

Symbol ⚠ : Fire or electrical shock hazard. Only original parts should be used to replace any part with symbol ⚠
Any other component substitution(other than original type), may increase risk or fire or electrical shock hazard.

"Pour votre sécurité, ces documents doivent être utilisés par des spécialistes agrées, seuls habilités à réparer votre appareil en panne."

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LASER SAFETY

This unit employs a laser. Only a qualified service person should remove the cover or attempt to service this device, due to possible eye injury.

LASER DEVICE UNIT

Type:	SemiconductorlaserGaAlAs
Wave length:	660 nm (DVD) 780 nm (VCD/CD)
Output Power: (out of objective)	20 mW (DVD+RW writing) 0,8 mW (DVD reading) 0,3 mW (VCD/CD reading)
Beam divergence:	60 degree

CLASS 1
LASER PRODUCT

USE OF CONTROLS OR ADJUSTMENTS OR PERFORMANCE OF PROCEDURE OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.

AVOID DIRECT EXPOSURE TO BEAM

WARNING

The use of optical instruments with this product will increase eye hazard.
Repair handling should take place as much as possible with a disc loaded inside the player

WARNING LOCATION: INSIDE ON LASER COVERSHIELD

CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLEN
VARNING SYNLIG OCH OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD BETRAKTA EJ STRÅLEN
VARO! AVATTAESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN
VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETSEN
DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM
ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

CAUTION

ONLY QUALIFIED SERVICE PERSONNEL SHOULD REMOVE THE COVER

OR ATTEMPT TO SERVICE THIS DEVICE.

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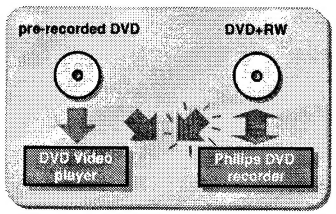
Introduction

DVD Video Recorder

DVD (Digital Versatile Disc) is the new storage medium that combines the convenience of the Compact Disc with the latest advanced digital video technology.
DVD Video uses state-of-the-art MPEG2 data compression technology to register an entire movie on a single 5-inch disc. DVD's variable bitrate compression, running at up to 9.8 Mbits/second, captures even the most complex pictures in their original quality.
The crystal-clear digital pictures have a horizontal resolution of over 500 lines, with 720 pixels (picture elements) to each line. This resolution is more than double that of VHS, superior to Laser Disc, and entirely comparable with digital masters made in recording studios.

DVD+ReWritable (DVD+RW) is the next step in video technology. DVD+RW uses phase-change media, the same technology that formed the basis for CD-ReWritable. A high-power laser is used to change the reflectivity of the recording layer. This process can be repeated more than a thousand times.

Your Philips DVD recorder is a **recorder** and **player** for digital video discs, with a **two-way compatibility** to the universal DVD Video standard. This means that:
- existing **pre-recorded DVD Video** discs can be played on your Philips DVD recorder and
- **recordings**, made on your Philips DVD recorder, can be played on existing DVD Video players and DVD-ROM drives.



With it, you will be able to record TV programmes or to edit and archive your own camcorder recordings. Superb digital picture and sound quality, quick access to the tracks you have recorded and extensive playback features contribute to a completely new video experience.

From now on you will enjoy full-length movies with true cinema picture quality, and stereo or Multi-channel sound (depending on the disc, and on your playback set-up).You will find your recorder remarkably easy to use, by way of the On-Screen Display and recorder display, in combination with the remote control.

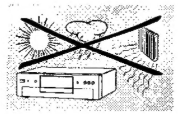
Box contents

First check and identify the contents of your DVD recorder package, as listed below:
- DVD recorder
- Remote Control Handset with separately-packed batteries
- 2-core power cord
- SCART cable
- S-video cable
- Antenna (aerial) cable
- Audio cable
- Video cable
- DVD+RW disc
- User Manual
- Warranty card

If any item should be damaged or missing, please inform your supplier without delay.

Keep the packaging materials; you may need them to transport your recorder in the future.

Placement



- Place the recorder on a firm, flat surface.
- Keep away from domestic heating equipment and direct sunlight.
- In a cabinet, allow about 2.5 cm (1 inch) of free space all around the recorder for adequate ventilation.
- The lense may cloud over when the DVD recorder is suddenly moved from cold to warm surroundings. Playing a CD/DVD is not possible then. Leave the DVD recorder in a warm environment for two hours before use, so the moisture can evaporate.
- The recorder should not be exposed to dripping or splashing, no object filled with liquids, such as vases, should be placed on the recorder.

Cleaning discs

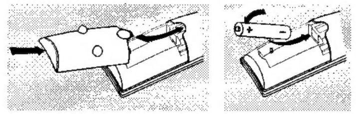
Some problems may occur because the disc inside the recorder is dirty. To avoid these problems clean your discs regularly, in the following way:

- When a disc becomes dirty, clean it with a cleaning cloth. Wipe the disc from the centre out.

Caution:
Do not use solvents such as benzine, thinner, commercially available cleaners, or anti-static spray intended for analogue discs.
Do not use commercially available cleaning discs to clean the lens, as these discs may damage the optical unit.

Remote control

Loading the batteries



- Open the battery compartment cover.
- Insert two 'AA' (LR-6) batteries as indicated inside the battery compartment.
- Close the cover.

Caution:
Do not mix old and new batteries. Never mix different types of batteries (standard, alkaline, etc.). This may reduce the lifetime of the batteries.

Connections - back side of your DVD recorder

- Please refer to your TV set, VCR, Stereo System and any other User Manual(s) as necessary to make the optimal connections.
- Do not connect the power until all other connections are made.
- Do not connect your DVD recorder to your TV set via your VCR, because the video quality could be distorted by the copy protection system.
- For better sound reproduction you can connect the recorder audio outputs to your amplifier, receiver, stereo system or A/V equipment. For this see 'Connecting to A/V receiver or A/V amplifier'.

Caution:
Do not connect the recorder's audio output to the phono input of your audio system in order to avoid damage to your equipment.

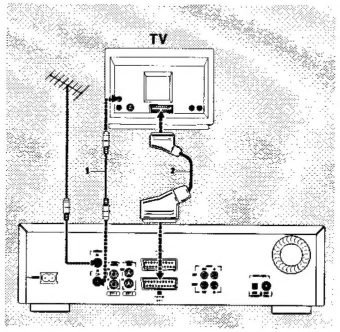
Connecting to the antenna

- Remove the antenna (aerial) cable plug from your TV set and insert it into the antenna socket at the back of the DVD recorder.
- Plug one end of the antenna (aerial) cable supplied ***(1)*** into the TV socket on the DVD recorder and the other end into the antenna input socket on your TV set.

Connecting to a TV set

To obtain the highest possible picture and sound quality from your TV set it is recommended to use the SCART connector on both DVD recorder and TV set.

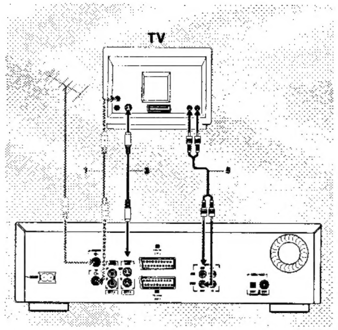
- Connect the bottom SCART connector (EXT 1) to the corresponding connector on the TV set, using the SCART cable supplied ***(2)*** as shown in the drawing.



If your TV set is not equipped with a SCART connector, you can connect the DVD recorder with the S-video (Y/C) sockets.

S-video (Y/C) connection

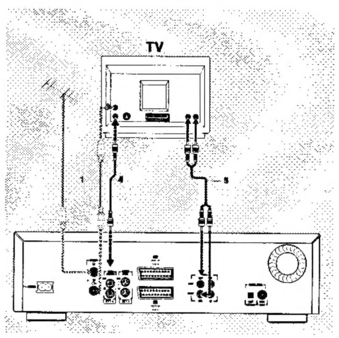
- Connect the S-video output socket to the corresponding input socket on the TV set, using the supplied S-video cable ***(3)***.
- Connect the audio Left and Right output sockets to the corresponding sockets on the TV set using the audio cable supplied ***(5)***.



If your TV set is not equipped with S-video sockets, then connect the DVD recorder with the CVBS sockets to your TV set.

Video (CVBS) connection

- Connect the Video (CVBS) output socket (yellow) to the corresponding input socket on the TV set using the video cable supplied ***(4)***.
- Connect the audio Left (white) and Right (red) output sockets to the corresponding sockets on the TV set using the audio cable supplied ***(5)***.



Connecting to audio equipment

Connecting to A/V receiver or A/V amplifier with digital Multi-channel decoder

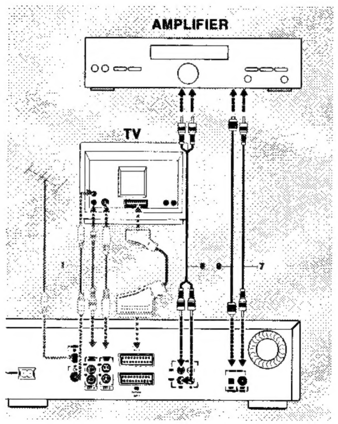
The best possible sound quality is obtained by connecting your DVD recorder to an A/V receiver with Multi-channel decoder (Dolby Digital, MPEG 2 and DTS).

Digital Multi-channel sound
Digital Multi-channel connection provides the optimum sound quality. For this you need a Multi-channel A/V receiver that supports one or more of the audio types supported by your DVD recorder (MPEG 2, Dolby Digital and DTS). For this you can check the receiver manual and the logos on the front of the receiver.

- Connect the recorder's digital audio output to the corresponding input on the receiver. Use a digital coaxial cable ***(7)*** or a digital optical audio cable ***(8)***.

If you do not have a digital coaxial audio cable, you may use the supplied video cable ***(4)***.

Note:
If the audio type of the digital output does not match the capabilities of your receiver, the receiver will produce a strong, distorted sound. The audio type of the DVD disc in play is displayed in the Status Window, when changing the language. 6 Channel Digital Surround Sound via digital connection can only be obtained if your receiver is equipped with a Digital Multi-channel decoder.



If you cannot connect your DVD recorder to an A/V receiver with Multi-channel decoder, choose one of the following alternatives.

Connecting to a receiver equipped with two channel digital stereo (PCM)

- Connect the recorder's digital audio output to the corresponding input on your receiver. Use the supplied video (CVBS) cable ***(7)*** or an optional digital optical audio cable ***(8)***.
- After installation you will need to activate PCM on the DVD recorder's digital output (see 'User Preferences').

Connecting to a receiver equipped with Dolby Pro Logic

- Connect the recorder to the TV set and connect the recorder's audio Left and Right output sockets to the corresponding inputs on the Dolby Pro Logic Audio/Video receiver, using the audio cable supplied ***(6)***.
- Make the appropriate Sound settings for Analogue Output in the user preferences menu.

Connecting to a TV set equipped with a Dolby Pro Logic decoder

- Connect the recorder to the TV set as described in chapter 'Connecting to a TV set'.

Connecting to a receiver with two channel analogue stereo

- If you have a receiver with two-channel analogue stereo without any of the above mentioned sound systems, connect the audio Left and Right output sockets to the corresponding sockets on your receiver, amplifier or stereo system. Use the audio cable supplied ***(6)***.

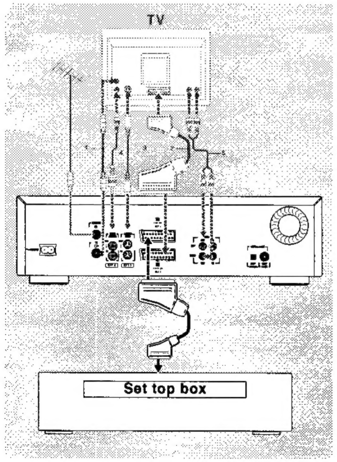
English

Connecting to other equipment

Use the top SCART connector (EXT 2) on your DVD recorder to make connections to a:

- Satellite receiver or Set top box,
- VCR,
- DVD Video player
Most pre-recorded video cassettes and DVD discs are copy protected. If you try to copy them the display shows 'COPY PROTECT'.

For installation of a decoder, see 'User Preferences' - 'Installation'.

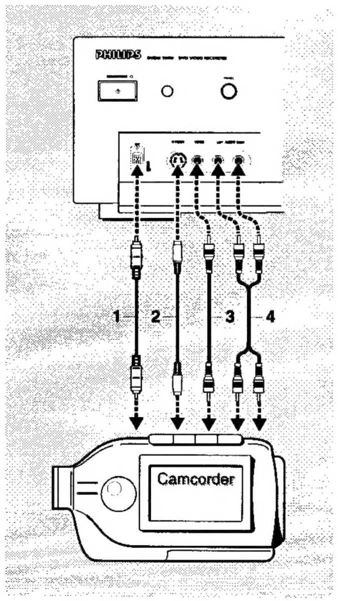


Note:
If the power is off or Low Power Standby is selected (see User Preferences - features), the signal from EXT 2 will not be passed on to the TV set on EXT 1.

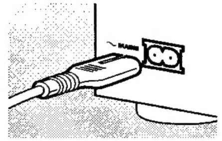
Connections - frontside of your DVD recorder

Camcorder connection

- If you have a DV or Digital 8 camcorder, connect the i-link DV input socket ***(1)*** to the corresponding output socket on the camcorder using the i-link cable of your camcorder.
- If you have a Hi-8 or S-VHS(C) camcorder, connect the S-video input socket to the corresponding output socket on the camcorder, using the S-video cable supplied ***(2)*** and connect the audio cable ***(4)*** supplied.
- Otherwise connect the Video input socket (yellow) to the corresponding output socket on the camcorder using the video cable supplied ***(3)*** and connect the audio Left (white) and Right (red) input sockets to the corresponding sockets on the camcorder using the audio cable supplied ***(4)***.



Power supply



- Make sure that all necessary connections are made before connecting the DVD recorder to the power supply.
- Plug the power cable supplied into the Power connector on the rear of the recorder.
- Plug the mains plug into an AC outlet.

Note:
Always check if the local mains voltage matches the required 220V - 240V.
When the recorder is in the Standby position, it is still consuming some power.
If you wish to disconnect your DVD recorder completely from the mains, withdraw the plug from the AC Outlet.
When the DVD recorder is disconnected from the mains, TV channels and timer data will be stored typically 1 year.

First time set-up: virgin mode

After switching on the DVD recorder for the very first time the 'virgin mode screen' will appear.

In 'virgin mode' you may have to set your preferences for some of the recorder features.

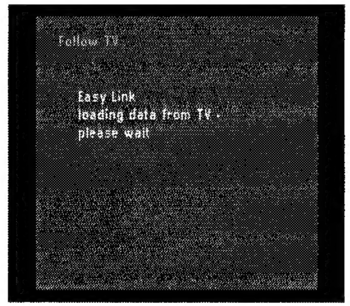
If the 'virgin mode screen' does not appear, your DVD recorder has been installed already. You may still change the settings via the 'installation menu'.
Depending on the kind of TV set, preferences will have to be set manually or they will be taken over automatically from the TV set.

Automatic setting

When your TV set is equipped with EasyLink™, Cinema Link™, NEXTVIEW Link™, SmartLink™, Q-Link™ or MegaLogic™, the TV settings will be taken over from the TV set but they cannot be changed manually afterwards.

When preferences are taken over from your TV set, the message '**Easy Link loading data from TV - please wait**' will appear.
Menus for which no preferences are available will be displayed. They have to be set manually.

Notes:
Preferences have to be set in the order in which the item menus will appear on the screen.
If the recorder is switched off while setting user preferences, all preferences have to be set again after switching the recorder on again.
The 'virgin mode' will only be concluded after the preferences for the last item have been confirmed.



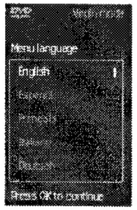
Manual setting

When a menu is displayed:

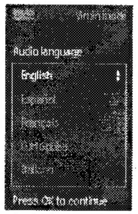
- Use the ▽ △ (down up cursor) keys to go through the options in the menu. The icon of the selected option will be highlighted.
- Use **OK** to confirm your selection and to select the next menu.

The following items may have to be set in virgin mode:

Menu language
The on-screen menus will be displayed in the language you choose.

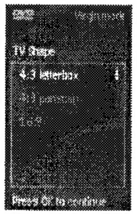


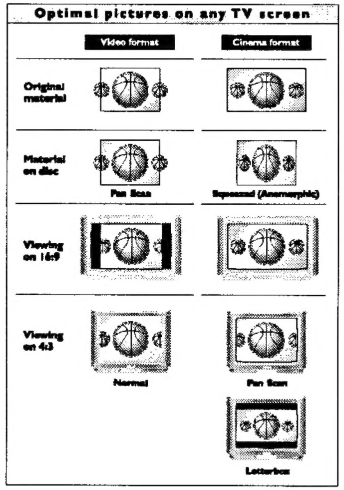
Audio language
The sound will be in the language you choose, provided this is available on the disc in play. If not, speech will revert to the first spoken language on the disc. Also the DVD Video disc menu will be in the language you choose, provided this is available on the disc.



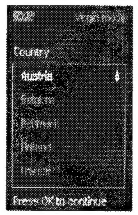
Subtitle language
The subtitles will be in the language you choose provided this is available on the disc in play. If not, subtitles will revert to the first subtitle language on the disc.

TV Shape
You can choose:
- **16:9** if you have a wide screen (16:9) TV set.
- **4:3** if you have a regular (4:3) TV set. In this case you can also choose between:
  - **Letterbox** for a 'wide-screen' picture with black bars top and bottom,
  - **Pan Scan**, for a full-height picture with the sides trimmed. If a disc has Pan Scan, the picture then moves (pans) horizontally to keep the main action on the screen.



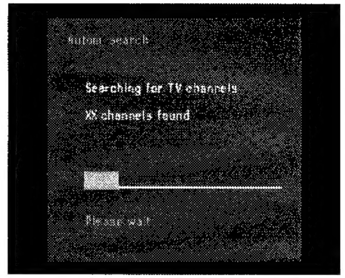


Country
Select your country. This is used as input for the 'Parental Control' feature (see 'Access Control') as well as the searching of TV channels.



Auto TV Channel Search
Make sure the antenna is connected. See 'Connecting to the antenna'. Your DVD recorder will search for all TV channels.
It stores channels in the sequence they are found.

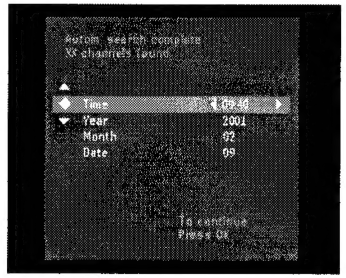
- Confirm with **OK**.
  ➤ Auto search starts. This can take several minutes.



➤ When Auto search is completed 'Autom search complete - XX channels found' appears on the TV screen.

After Auto channel search you can have TV channels stored automatically in the same order as your TV set. See 'User preferences installation' - 'Follow TV'.

Time/Date
When Channel auto search is completed the actual Time and Date are also set automatically.
If the time in the DVD recorder display is not correct, the clock must be set manually.



- Adjust 'Time', 'Year', 'Month', 'Date' if required, with the ▽ (down cursor) or △ (up cursor) key.
- Change values with the the ◁ (left cursor) or ▷ (right cursor) key or the digit keys **0-9**.
- To end, press **OK**.

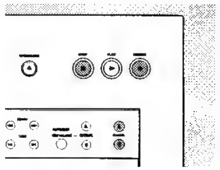
Note:
All these items may have to be set after first start up ('virgin mode'). After that they can always be adapted in the user preferences menu. When your TV set is equipped with Easy Link the TV set presets will be taken over from the TV set but they cannot be changed manually afterwards.

Virgin mode settings are now completed.
All settings can still be changed. See 'User preferences'.

English

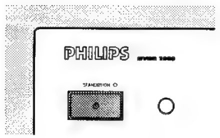
Quick start

Recording and playback are the basic functions of your DVD recorder. In this chapter the elementary operations for recording or playing a disc are presented separately for quick reference purposes.
Detailed information on different modes, settings and features can be found in the chapter 'Operation'.

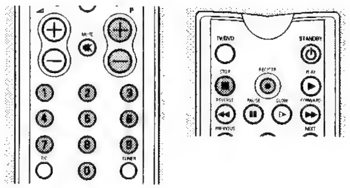


Switching on

- Switch on the TV set and select the programme number that you have chosen for video playback (see operating manual for your TV set).
- Press ⏻ **STANDBY/ON**.
  ➤ The recorder display lights up, and the 'virgin mode screen' appears.



The virgin mode will only occur after the very first start up of the recorder. In virgin mode you may have to set your personal preferences for some of the recorder's most relevant items. See virgin mode in the previous chapter.



Manual recording

Checking input

Normally, the DVD recorder displays the contents of the disc on screen. Use the **TUNER** key in order to switch to the internal tuner, or whichever other source is selected, if you want to check the input before starting a recording. Press **TUNER** again to go back to disc mode.

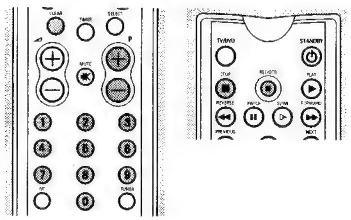
Recording

- Insert a recordable DVD+RW disc.
- Use **CHANNEL ▲** or **CHANNEL ▼** (on the recorder) or **P+**, **P-** or the digit keys **0-9** (on the remote control) to select the programme number (programme name) from which you wish to record.

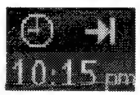
When a TV channel transmits a channel name, it will be shown on the display and on screen.

- Press **RECORD** (on recorder) or **REC/OTR** (on remote control).
  ➤ RECORD is shown on the display.
- Press ■ STOP to stop recording.
  ➤ MENU UPDATE is shown on the display.

Recording with automatic switch-off (OTR One-Touch Recording)



- Insert a recordable DVD+RW disc.
- Use **CHANNEL ▲** or **CHANNEL ▼** (on the recorder) or **P+**, **P-** or the digit keys **0-9** (on the remote control) to select the programme number (programme name) from which you wish to record.
- Press **RECORD** (on recorder) or **REC/OTR** (on remote control) twice.
  ➤ A recording will be made of 30 minutes.
  ➤ The required end time of the recording is shown in the timer box on screen. The remaining recording time is shown in the status box on screen and on the display.



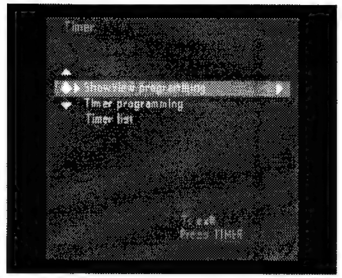
- Press **RECORD** or **REC/OTR** again to obtain a 30-minute increment.
- Shortly after pressing **REC/OTR**, OTR can be cancelled by pressing **CLEAR**.

Timer programming

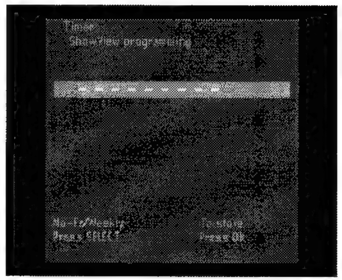
Timer programming with 'ShowView'

A ShowView programming number is a number of up to nine digits, printed in most TV guides next to the start time of a TV programme. It contains all information you need for programming a timer.

- Press **TIMER** on the remote control.
- Select 'ShowView programming' with △ (up cursor) or ▽ (down cursor).



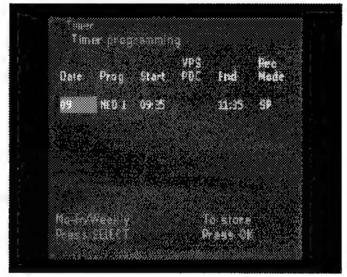
- Press ▷ (right cursor).



- Enter the entire ShowView programming number. You can correct it if you made a mistake, with **CLEAR**.
- Confirm with **OK**.
  ➤ The data will appear on the TV screen.
- Confirm with the **OK** key.
  ➤ The data has been stored in a timer block.
- To end, press **TIMER**.
- Please make sure that you inserted a disc without erase protection. If you inserted a disc with erase protection, it will be ejected.
- Switch off with ⏻ **STANDBY/ON**.

Timer programming without 'ShowView'

- Press **TIMER** on the remote control.
- Select 'Timer programming' with △ (up cursor) or ▽ (down cursor).
- Press ▷ (right cursor).



- Enter the date with △ (up cursor) or ▽ (down cursor), or with the digit keys **0-9**.
- Press ▷ (right cursor).
- Enter the programme number from which you want to record.
- Press ▷ (right cursor).
- Enter the Start time.
- Press ▷ (right cursor).
- Enter the End time.
- If you made a mistake, you can go back with ◁ (left cursor).
- Confirm with **OK**.
  ➤ The data has been stored in a timer block.
- To end, press **TIMER**.
  ➤ Make sure that you inserted a disc without write protection. If you inserted a write-protected (locked) disc, recording will be refused.
- Switch off with ⏻ **STANDBY/ON**.

English

Directions For Use

DVDR1000 /0x1 /691

3.

Playing a pre-recorded DVD-Video disc

- Insert a pre-recorded DVD-Video disc.
  ➤ When 'Autoresume' is set to 'On' (see 'User Preferences') playback starts automatically from the point where it was stopped, the last time the disc was played.
  ➤ When 'Autoresume' is set to 'Off', the disc will play from the start of the disc. You can however resume play from the point at which you stopped, the last time the disc was played, by pressing ▶ **PLAY** shortly after the disc starts to play.
- The disc may invite you to select an item from a menu. If the selections are numbered, press the appropriate numerical key; if not, use the ▽ △ (down up cursor) or ◁ ▷ (left right cursor) keys to highlight your selection, and press **OK**.
  ➤ The currently playing title and chapter number are displayed in the System menu bar and the recorder display. The elapsed time is shown in the disc status window and the recorder display.

- To stop playback at any time, press ■ **STOP** or **DISC MENU**.

Playing a recordable DVD+RW disc

- Insert a recordable DVD+RW disc.
  ➤ If the disc is a new blank disc, the display will show 'EMPTY DISC'.
  ➤ If the inserted disc is write-protected, playback always starts automatically.
- When you press ▶ **PLAY**, playback always starts automatically from the point where it was stopped the last time the disc was played or recorded. If you want to start playback from the beginning of the disc, you can do so via the Index Picture Screen (see 'Index Picture Screen').
- With ⏮ **PREVIOUS** and ⏭ **NEXT** you can go to the previous or next title.
- To stop playback at any time, press ■ **STOP** or **DISC MENU**.
  ➤ You return to the Index Picture Screen.

Functional overview

Front of recorder

⏻ STANDBY/ON
- switches the recorder to Power/Standby mode

Standby indicator
- lights up red when the recorder is in standby mode
- lights up green when the recorder is operative

PANEL
- to open and close the panel

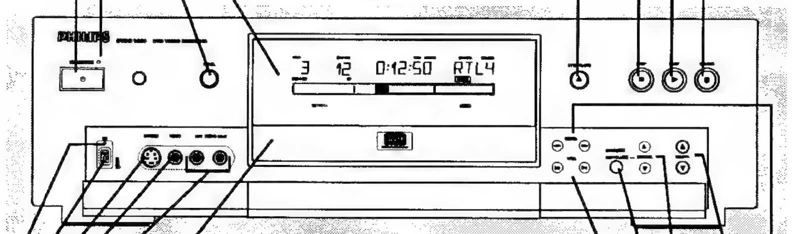
DISPLAY
- displays the current status of the recorder

● RECORD
- direct recording of the selected programme on TV set or the recorder (depending on the DIRECT RECORD setting)

▶ PLAY
- starts video/audio play

■ STOP
- stops video/audio play or recording

▲ OPEN/CLOSE
- opens/closes the disc tray



Disc loading tray

AUDIO (Left/Right)
- Audio input socket left/right to connect a camcorder or video recorder

VIDEO (CVBS)
- Video input socket to connect a camcorder or video recorder

S-VIDEO
- Video input socket to connect a camcorder or video recorder

DV
- Audio/Video input socket to connect a digital camcorder

DV-indicator
- Lights up red when DV input is active

TITLE
- ⏮ selects previous title /chapter/track/index or beginning current title/chapter/track/index
- ⏭ selects next title/ chapter/track/index

AUTO/MAN REC VOLUME
- to adjust the recording level automatically or manually

MANUAL
- ▲ ▼ to increase/decrease the recording level

CHANNEL
- to select channels manually

SEARCH
- ◀◀ search backward
- ▶▶ search forward

English

Rear of recorder

MAINS
- connection to the mains

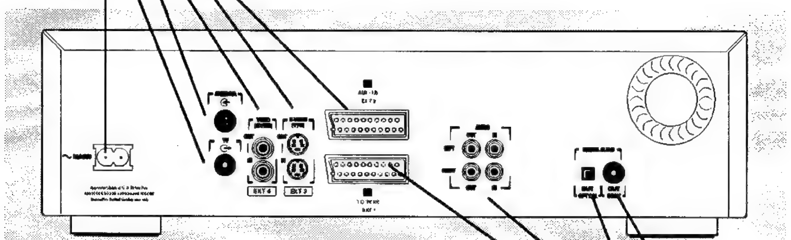
TV
- RF connection to TV set

ANTENNA
- RF connection to antenna/cable TV signal

VIDEO (CVBS)
- OUT: for connection to a TV set, receiver or amplifier with CVBS video inputs
- IN: for connecting a video source with CVBS outputs

S-video (Y/C)
- OUT: for connection to a TV set, receiver or amplifier with S-video (Y/C) inputs
- IN: for connecting a video source with S-video (Y/C) outputs

AUX I/O (EXT II)
- for connection to a satellite receiver, decoder, video recorder, set top box etc. via SCART



TO TV I/O (EXT I)
- for connection to a TV set with SCART

AUDIO OUT L/R
- connection to an amplifier, receiver, stereo system or to a TV set that is not equipped with a SCART connector

AUDIO IN L/R
- connection to the audio output of a video source that is not equipped with a SCART connector

OUT OPTICAL
- connection to an amplifier, receiver or stereo system with a digital (optical) audio input

OUT COAX
- connection to an amplifier, receiver or stereo system with a digital (coaxial) audio input

English

Display

DVD
- DVD Video disc inserted

DVD+RW
- DVD+Rewritable disc inserted

TITLE
- DVD title number

TRACK
- VCD/CD track number

VCD
- Video CD inserted

CD
- Audio CD inserted

SVCD
- Super Video CD inserted

HQ - SP - LP - EP
- Selected recording mode: High Quality, Standard Play, Long Play or Extended Play

CHAPTER
- DVD chapter number

DECODER
- Decoder activated for current preset

VPS/PDC
- Video Programming System/Programme Delivery Control active on current preset

CHANNEL
- Preset name or number

RECORD
- Recording in progress

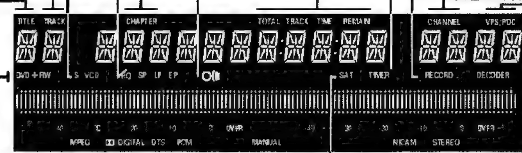
TIMER
- Timer programmed or active

TRACK TIME
- Track time in minutes and seconds

TOTAL TIME
- Total playback or recording time in hours, minutes and seconds

TOTAL REMAIN
- Total remaining playback or recording time in hours, minutes and seconds

- remote control active (flashing)



SAT
- Recorder prepared for or engaged in satellite recording

NICAM
- NICAM digital stereo sound on current preset

STEREO
- Stereo sound from tuner

dB scale
- indicates recording volume when using manual level control

Disc bar
- Displays disc content, recording level or formatting progress

MANUAL
- Manual recording level control

DD DIGITAL - DTS - MPEG - PCM
- Active audio format

Remote control

TV/DVD switch
- DVD mode/TV mode selector for TV set*

■
- stop

●
- direct recording of the currently selected programme

▶
- play

◀◀
- search backward

II
- pause

I▷
- slow motion

▶▶
- search forward

I◀
- previous chapter, track or title

EDIT
- displays edit menu for DVD+RW disc

▶I
- next chapter, track or title

◁ **+/-**
- TV volume up/down

🔇
- TV Mute ON/OFF

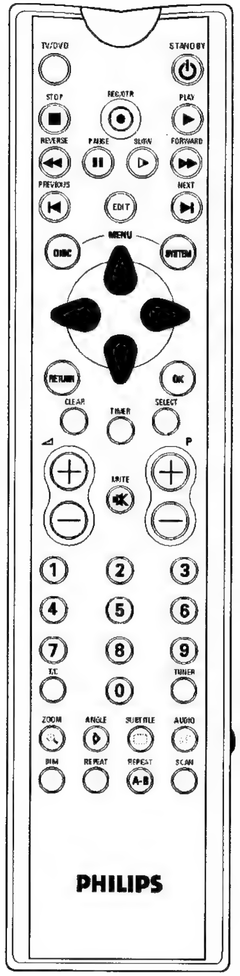
P +/-
- programme up/down

ZOOM
- enlarge video image

ANGLE
- select DVD camera angle

SUBTITLE
- subtitle language selector

AUDIO
- audio language selector



STANDBY ⏻

DISC MENU
- displays DVD disc menu or index picture screen

SYSTEM MENU
- displays recorder menu bar

▽ △ ▷ ◁
- down/up/right/left cursor movement

RETURN
- go back to previous menu step

CLEAR
- delete last entry/clear TIMER

TIMER
- displays the 'timer menu'

SELECT
- switches between different values in a menu

OK
- acknowledge menu selection

0-9
- numerical key pad

T/C
- select title
- select chapter

TUNER
- switches between disc mode and tuner mode

SIDE SWITCH
- enables other keys to operate the TV set (see Appendix)

DIM
- changes brightness setting of display

REPEAT
- repeat chapter, track, title, disc

REPEAT A-B
- repeat sequence

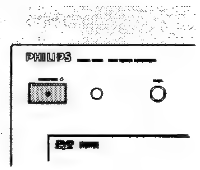
SCAN
- playback of the first 10 seconds of each chapter within a title (DVD) or the first 10 seconds of each track on a disc (VCD/CD)

*Note:
In a TV set - DVD recorder - Set top box configuration use the 'TV/DVD' switch to switch back and forth between Set top box reception and DVD recorder reception. This only functions when you used a Scart cable to connect the DVD recorder to your TV set and if your TV set responds to this switch-over. This function is useful when, for example, you want to watch a channel from the Set top box on your TV set and make at the same time a recording from another source.

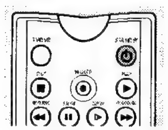
Operation

Important notes for operation

You can switch on the DVD recorder with the ⏻ **STANDBY/ON** key. Keep your DVD recorder connected to the mains at all times to ensure that programmed recordings can be made and that the television functions normally.



Both the DVD recorder and the remote control have an 'Emergency interrupt' button. You can use the ⏻ **STANDBY** button to interrupt a function. When you have an operating problem, you can interrupt the function and start again.



Loading discs

1 Press ▲ **OPEN/CLOSE** on the front of the recorder. The disc loading tray opens.
2 Lay your chosen disc in the tray, label side up. Make sure it is sitting properly in the correct recess.
3 Press ▲ **OPEN/CLOSE**, to close the tray.
➤ 'READING' appears in the status window and on the recorder display. If the inserted disc is pre-recorded or write-protected, playback always starts automatically.

You can always unload a disc by pressing ▲ **OPEN/CLOSE** again or pressing ■ **STOP** on the remote control for two seconds.

Note: If 'Child Lock' is set to ON and the disc inserted is not in the 'child safe' list (not authorized), the PIN code must be entered and/or the disc has to be authorized. (see 'Access Control')

Disc types

You will recognize the different types of discs, that can be used in your DVD recorder by the logo. Depending on the disc type you can either use it for recording and playback or playback only. Some discs are not suitable at all to be used in the DVD recorder.
In the next table a summary is given of all excisting disc types and their DVD recorder compatibility.

The following disc types can be used for recording and playback:

DVD+RW
Records and plays; In case of a new blank disc, after the first recording, some more time (up to two minutes) is needed to make the disc compatible with DVD video players.

The following disc types can be used for playback only:

DVD-Video

DVD-R
Only plays if it contains DVD-Video.

DVD-RW
Only plays if it is recorded in video mode and has been finalized.

CD Digital Audio
You can play digital audio CDs in conventional style through a stereo system, using the keys on the remote control and/or front panel, or via the TV set using the on-screen display (OSD).

Super Audio CD
Of hybrid SACD discs, the CD layer can be played.

(Super) Video CD
Depending on the material on the disc (a movie, video clips, a drama series, etc.) these discs may have one or more tracks, and tracks may have one or more indexes, as indicated on the disc case. To make access easy and convenient, your recorder lets you move between tracks, and between indexes.

CD-R
Plays if it contains Audio CD.

CD-RW
Plays if it contains Audio CD.

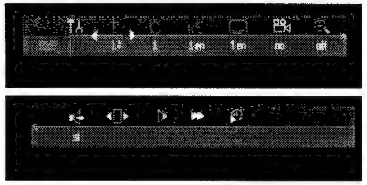
The following disc types cannot be used at all, neither for recording nor for playback:

DVD-RAM

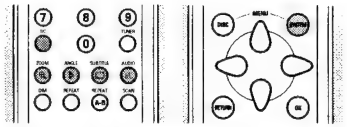
DVD-Audio

On-screen display information

System menu bar



The System menu bar can be called up by pressing any of the following keys on the remote control: **SYSTEM MENU, T/C, ANGLE, SUBTITLE, AUDIO** and **ZOOM**.

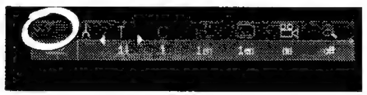


A number of recorder functions can be controlled via the system menu bar. You can navigate between the two parts of the system menu bar with the ◁ (left cursor) and the ▷ (right cursor) key.

Menu bar icons

PART 1	PART 2
User preference	Sound
Title/Track	Picture by Picture
Chapter/Index	Slow motion
Audio language	Fast motion
Subtitle language	Time search
Angle	
Zoom	

Temporary Feedback Field



The system menu bar contains a 'Temporary Feedback Field' with information concerning prohibited actions, playback modes, available angles, etc.

Scan

Repeat All

Repeat Title

Repeat Track

Repeat Chapter

Repeat A to end

Repeat A-B

Angle

Child Lock On

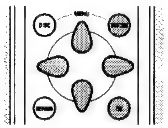
Child Safe

Resume

Action prohibited

User preference menu operation

- Press **SYSTEM MENU** on the remote control.
- Select in the system menu bar and press ▽ (down cursor).
  ➤ The user preferences menu appears.
- Use the ◁ ▷ △ ▽ (left right up down cursor) keys to toggle through the menus, sub menus and submenu options.
  ➤ When a menu item is selected, the cursor keys (on the remote control) to operate the item are displayed next to the item.
- Press **OK** to confirm and return to the main menu.

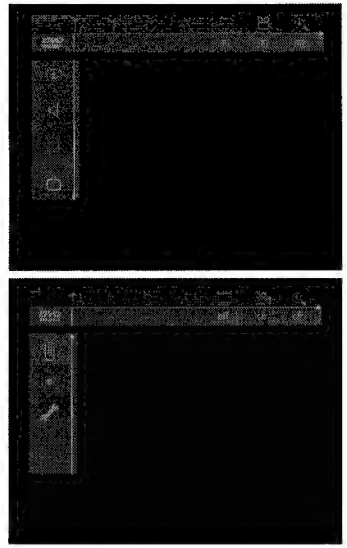


The following functions can be operated via the user preference menu.

User preference menu icons

Picture settings
Sound settings
Language settings
Feature settings
Remote control settings
Record settings
Installation

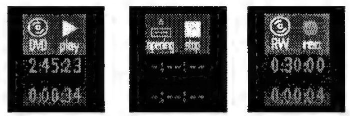
- You can navigate between the various items of the user preferences menu with the △ (up cursor) and the ▽ (down cursor) key. To select an item press ▷ (right cursor) key.



- By pressing **SYSTEM MENU** the system menu bar will disappear from the screen.

Status box

The status box displays the current status of the recorder and the disc type loaded.



Disc type icons

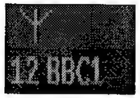
DVD+RW
DVD-Video
Video-CD
no disc
disc error

Disc status icons

- rec — recording
- stop — stop
- play — playing
- pause — pause play
- pause — record pause
- erasing — erasing
- fast forward
- fast reverse
- slow — slow motion

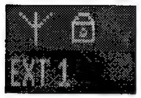
Tuner info box

The tuner info box is located at the bottom left of the screen and is displayed in tuner mode (See: Recording Checking input). It displays the currently selected input. When the tuner is selected it shows programme number and/or channel name.



Current channel

No signal

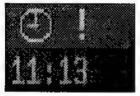


Copy-protected signal

Timer info box

The timer info box is located above the tuner info box and is displayed in tuner mode. It displays the current status of the timer.

When a timer is programmed it shows a timer indication and the start time or date of the first programmed recording.



Timer event due today

Timer event due on another day

When an OTR recording is in progress it shows the end time.

OTR recording in progress

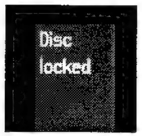
When no timer is programmed it displays the current time.

Current time

Note: Tuner info box and timer info box disappear during playback and after recording is started.

Warning box

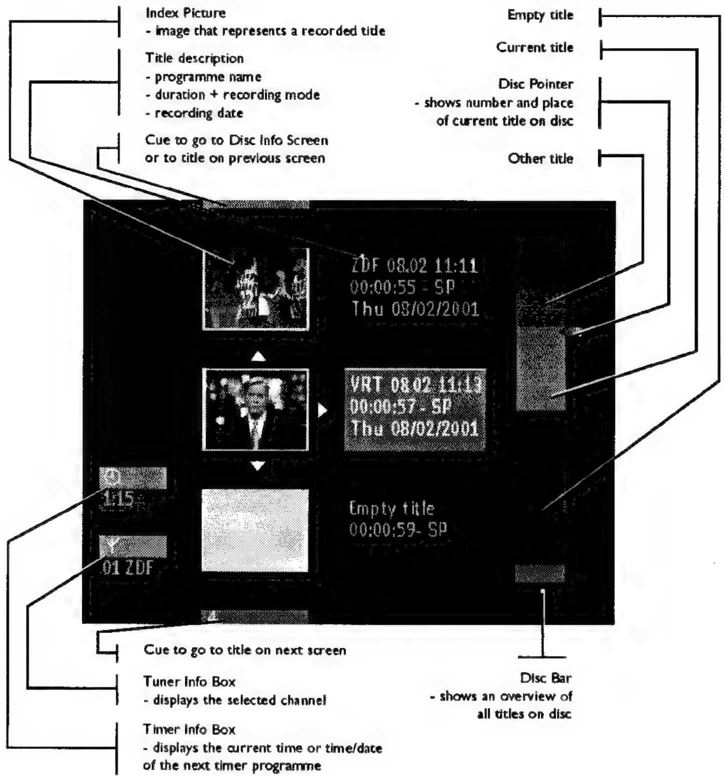
The warning box will be displayed on the location of the status box. For instance: 'Disc locked'



Index Picture Screen

The Index Picture Screen displays an overview of the titles recorded on the disc. Each title is represented by an index picture. Next to the index picture the programme name, duration, recording mode and recording date of the title are shown. If no name is known, the DVD recorder will fill in the source and the time of the recording instead.
Empty spaces (erased titles, or blank space at the end of the disc) are also shown as such.

- At maximum three titles will be shown on the screen at once. If more titles are present, you can navigate to those with the ▽ △ (down up cursor) keys.
- On the right hand side of the Index Picture Screen, you can see the disc bar. This gives an overview of all titles on the disc, as well as any empty spaces. On the disc bar, an arrow – the disc pointer – indicates your current position on the disc. From this point you may resume playback or recording.
- If you navigate trough the list of titles with ▽ △ (down up cursor) or ⏮ **PREVIOUS**/⏭ **NEXT**, the disc pointer will move along.
- Press ■ **STOP** to reset the disc pointer to the beginning of the disc.
- To move the disc pointer to the end of the last title, keep ⏭ **NEXT** pressed.
- If you navigate from an Index Picture to the box right next to it (containing name, rec mode, etc.), you enter the title settings menu (see under 'Managing disc content - Title settings').



English

User preferences

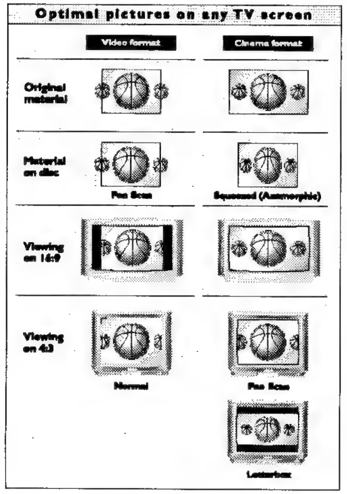
Setting user preferences

You can set your user preferences for some of the recorder features. (See 'Operation' - 'User preferences menu operation'.)

The following items can be adapted:

Picture settings

TV Shape
With TV Shape you can adjust the output of your DVD Video Recorder to optimally fit your TV screen.
You can choose:
- **16:9** if you have a wide screen (16:9) TV set.
- **4:3** if you have a regular (4:3) TV set. In this case you can also choose between:
  - **Letterbox**: for a 'wide-screen' picture with black bars at the top and bottom.
  - **Pan Scan**: for a full-height picture with the sides trimmed. If a disc has Pan Scan, the picture then moves (pans) horizontally to keep the main action on the screen.



Black level shift (NTSC only)
Adapts the colour dynamics to obtain richer contrasts. Select *On* or *Off*.

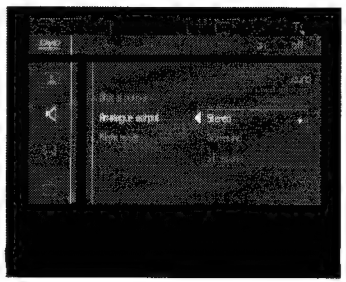
Video shift
Factory setting is such that the video will be centered on your screen. Use this setting to adjust the position of the picture on your TV set by scrolling it to the left or right.

SCART Video
Factory setting is RGB. Select S-video (Y/C) via SCART when connecting to an S-VHS recorder.

Sound settings

Digital output
Factory setting 'All' means that both coaxial and optical outputs are switched on, and that Dolby Digital and MPEG-2 Multi-channel is fed to the outputs as such.
If your equipment doesn't include a digital Multi-channel decoder, set the digital output to 'PCM only' (Pulse Code Modulation). Both coaxial and optical outputs are then switched on, and Dolby Digital and MPEG2 Multi-channel are converted to PCM. If you are not connecting equipment with a digital input, change the setting to 'Off'.

Analogue output



Select Stereo, Surround or 3D Sound. Factory setting is Stereo.

Surround: Select this setting when using equipment with a Dolby Surround Pro Logic decoder. In this setting the 5.1 audio channels (Dolby Digital, MPEG-2) are downmixed to a Surround-compatible 2-channel output.
3D Sound: In a set-up without rear speakers (analogue stereo output), this option remixes the six channels of digital surround (Dolby Digital, MPEG-2) into a two speaker output, while retaining all of the original audio information. The result is the listening sensation of being surrounded by multiple speakers.

Connected audio system	Digital out	Analogue out
Amplifier or TV with two channel analogue stereo	*Off*	*Stereo*
Amplifier or TV with Dolby Surround or Dolby Pro Logic	*Off*	*Surround*
Amplifier with two channel digital stereo	*PCM only*	*Stereo*
A/V receiver with Multi-channel decoder (Dolby Digital, MPEG, DTS)	*All*	*Stereo or Surround*
Multi-channel A/V receiver with 6-ch connectors	*Off*	*Surround*

Night Mode
Night mode optimizes the dynamics of the sound with low volume playback for less disturbance in quiet environments. This only works for Dolby Digital audio on DVD video discs.

Language settings

The preferred language can be adapted via the system menu bar. Also see 'virgin mode'. Settings can be changed for:
- Menu language
- Playback audio language
- Subtitle language
- Country setting.

Feature settings

Access Control
Access Control contains the following features:
Child Lock - When Child Lock is set on, a 4-digit code needs to be entered in order to play discs.
Parental Level - Allows the conditional presentation of DVD discs containing Parental Level information.
Change country - Allows conditional presentation of DVD-Video discs containing country information.
Change code - To change the pin code.
See 'Access Control'.

Adapt disc format
This options adapts the menu of a DVD+RW disc, recorded on a different brand of recorder, to the own recorder.
A DVD+RW video disc that has been recorded on a different type or brand of recorder can be played, but may not provide all features commonly available to DVD+RW discs, such as the on-screen disc bar, the disc settings menu, the title settings menu, and editing. If the disc is not write-protected, the disc format can be adapted to the own recorder, after which these functions are available.

Status box
The status box displays the current status of the recorder and the disc type loaded (See 'Operation' - 'On-screen display information'). You can switch it on or off.
Off = always Off.
On = displayed together with the system menu bar or displayed temporarily (disappears after time-out) when changing the playback or record status.
Factory setting is 'On'.

Low Power Standby
If Low Power Standby is 'On', the recorder will consume minimum power in standby mode.
Factory setting is 'Off'.

Note:
When the recorder is in low power standby mode:
- the output of the equipment connected to EXT 2 will not be passed through to the TV set on EXT 1,
- the Display will be Off,
- the Standby indicator on the recorder will still light up in standby mode.

Auto resume
The Auto resume setting only applies to pre-recorded DVD-video and Video CD discs only - not only to the disc in the recorder but also to the last twenty discs you have played.
If Autoresume is set to 'On', playback will start from the point where it was stopped the last time the disc was played.

English

When Autoresume is set to 'Off', the recorder will start playing from the beginning of a disc. In this case you can still resume when [icon] appears on screen by pressing ▶ **PLAY**. Factory setting is 'On'.

PBC
This feature allows you to disable or enable the PBC (Playback Control) menu of VCD discs. See under 'Special VCD features': Factory settings is 'On'.

Remote Control settings

Key sound
The recorder makes a 'beep' sound upon every key command given via recorder or remote control keys. Select 'Off' to disable this sound. Factory setting is 'On'.

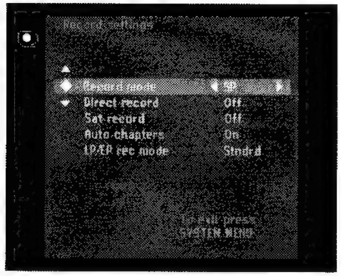
Remote control used
If you want to use the remote control of a Philips DVD player instead of the standard DVD recorder remote control, select 'DVD player'. Factory setting is 'DVD recorder'.

Record Settings

Record mode
By selecting a recording mode you define picture quality of recordings and maximum recording time for a disc.

Mode	Picture quality	Total recording time
HQ (High Quality)	best possible picture quality	60 minutes
SP (Standard Play)	pre-recorded DVD quality	120 minutes
LP (Long Play)	better than S-VHS picture quality	180 minutes
EP (Extended Play)	better than VHS picture quality	240 minutes

For playback, the correct recording mode will automatically be selected. Depending on the selected mode the available recording time on a disc varies.
- In the record settings menu, select 'Record mode'.



- Alter the recording mode with ◁ or ▷ (left right cursor).
- Confirm with the **OK** key.
- To end, press **SYSTEM MENU**.

Direct record
With the Direct Record function switched On and the DVD recorder switched to standby, the channel number selected on your television will be automatically taken over by the DVD recorder, at the moment it starts recording. This only applies for televisions connected via SCART, Easy Link and NEXTVIEW Link. Factory setting is Off.
- In the record settings menu, select 'Direct record'.
- Select On. If you select Off, the function will be switched off.
- Confirm with **OK**.
- To end, press **SYSTEM MENU**.

Sat record
You can only use this function, when you have a satellite receiver, which can control other equipment by a 'programming' function. In this mode your DVD recorder starts recording when the satellite receiver releases a signal. The start and end of the recording is controlled via one of the SCART sockets.
- In the record settings menu, select 'Sat record'.
- Select the SCART socket to which the satellite receiver is connected with ◁ or ▷ (left right cursor).
- Confirm with **OK**.
- Insert a recordable DVD+RW disc.
- Press ⏻ **STANDBY/ON**.
  ➤ When this function is switched on, SAT appears on the display.
  ➤ The DVD recorder is now prepared for recording.

Factory setting is Off.

Auto chapters
If autochapters is 'On' every five to six minutes a chapter marker (beginning of a new chapter) is inserted during recording. This enables easy navigation through a title during playback. In either case, you can manually insert chapter markers afterwards. (See 'Managing disc content' - 'Edit in playback mode'.)

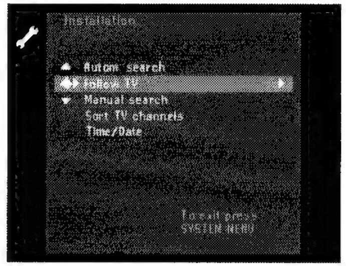
LP/EP rec mode
In long play or extended play recording mode you can select the Sport setting to optimize the video recording for images that contain fast movements, like sports programmes. The setting does not influence high quality or standard play recording mode.
Factory setting is Stndrd.

Installation

Auto TV Channel Search
Your DVD recorder will search for all TV channels. It stores channels in the sequence they are found. (See 'Installation - First time Set-up')

Note: All channels stored so far will be erased.

Follow TV
With Follow TV you can programme the same channel sequence on the DVD recorder as on the TV set. This only functions if the recorder socket (EXT1) and the TV set are connected with a SCART cable. Additional equipment connected to socket EXT2 must be switched off.



- Press **OK**.
  ➤ If the DVD recorder recognizes that the TV set has been connected with a SCART cable, 'TV 01' appears on the display.

➤ When 'NOTV' (no signal from TV set) appears on the display, the TV channels can not be allocated automatically. In this case read 'Manual TV channel search'.
- Select programme number '1' on the TV set.
- Confirm with **OK** on the remote control of the DVD recorder.
  ➤ The DVD recorder compares the TV channels on the TV set and the DVD recorder. If the channels match, this channel is stored at 'P01'.
- Wait until 'TV 02' appears and repeat the previous two steps for programme number 2 and the rest of the channels you want to store.
- To end, press **SYSTEM MENU**.

English

Manual TV channel search
You can perform a search to select and store TV channels manually.

- Press **SYSTEM MENU**.
- Select Installation.
- Select Manual search.
- In the line Channel/freq. select the display for:
  Freq : frequency
  CH : channel
  S-CH : special channel
- If you know the frequency or channel of the desired TV channel, you can enter the data in line Entry/search with the digit keys **0-9**. If you don't know the frequency or channel of the TV channel of your choice, press ▷ (right cursor) to start channel search.
- In the line Programme number select the programme number you want, using ◁ or ▷ (left right cursor) or digit keys **0-9**.
- If you want to change the TV channel name, press the ▷ (right cursor) key in line TV channel name.
- Select the character you want to change with the ◁ (left cursor) or ▷ (right cursor) key.
- Change the character with the ▽ (down cursor) or △ (up cursor) key.
- Press **OK** to confirm.

This DVD recorder can receive HiFi sound transmissions in NICAM Stereo. However, if sound distorsion occurs, due to poor reception, you can switch off NICAM:

- In the line NICAM select On or Off with the ◁ (left cursor) or ▷ (right cursor) key.

If you want to change the automatic TV channel setting, select the line Fine tuning. With the ◁ (left cursor) or ▷ (right cursor) key you can vary the automatic TV channel setting.

Important: This re-tuning is only necessary and useful in special cases, e.g. when stripes appear on your TV screen when using a cable-TV system.

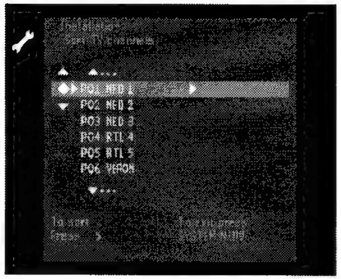
- Press **OK** to store the TV channel.
- To end, press **SYSTEM MENU**.

Connecting a decoder:

- Switch on the TV set and select the programme number for the DVD recorder.
- Select the TV programme you wish to link with the decoder function with **P+** or **P-**.
- Press **SYSTEM MENU**
- Select Installation
- Select Manual search
- Select Decoder.
- Select On with ◁ (left cursor) or ▷ (right cursor).
- Confirm with **OK**.
  ➤ 'DECODER' apperars on the display.
- To end, press **SYSTEM MENU**.

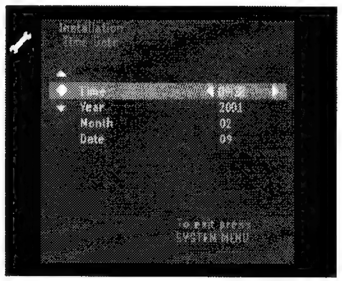
Sort/Clear TV channels manually

- If the DVD recorder is connected to the TV set with Easy Link or a similar system, manual sort cannot be executed. In all other cases, you can select.
- Press **SYSTEM MENU**.
- Select the line 'Installation'.
- Select the line 'Sort TV channels'.



- Select the TV channel to which you want to allocate a programme number (starting with P01) with the △ (up cursor) or ▽ (down cursor) key and press the ▷ (right cursor) key.
- Select the desired position with △ or ▽ (up down cursor) key.
- To store, press **OK**.
- To end, press **SYSTEM MENU**.

Time/Date
To adjust 'Time', 'Year', 'Month' and 'Date' with the digit keys **0-9**. Switch between fields with the ▽ △ (down up cursor) keys.



Recording

Before you start recording

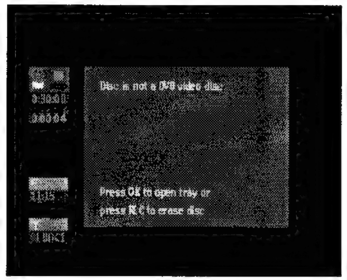
Recordings on a disc are started from the position of the so-called disc pointer, i.e. the point where the last recording was stopped. From there on earlier recordings may be overwritten without notice, unless the disc is write protected. In this respect your DVD recorder behaves just like a Video Cassette Recorder.

In the Index Picture Screen you can select the point where you want to start your recording. Use the ▽ △ (down up cursor) and **◂◂ REVERSE/▸▸ FORWARD** keys. You can see the the current location on the disc bar, indicated by the arrow.

Your DVD recorder always checks the disc that you have inserted:

➤ When a DVD+RW disc is inserted on which recordings have been made, the Index Picture Screen is shown on your TV screen.
➤ If the inserted disc is a completely empty recordable disc, the message EMPTY DISC appears, on the display.
➤ If the inserted disc is a DVD+RW disc with a content that is not DVD video compatible (e.g. a data disc), a dialog box is shown with the option to erase or eject the disc. You can only record on this disc after erasing it with the **RECORD** key.

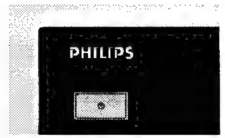
Note: On a disc containing PAL recordings, no NTSC recordings can be made and vice versa. On an empty disc, either type of recordings can be made.



➤ A disc can hold up to 48 titles (including empty titles). When this maximum is reached the on-screen message 'Too many titles' appears. If you want to make a new recording. You have to erase a title first next to an empty title. See 'Managing Disc Content'.

Switching on

- Switch on the TV set and select the programme number that you have chosen for video playback (see operating manual for your TV set).
- Press ⏻ **STANDBY/ON**.
  ➤ The recorder display lights up. If you have not yet installed your DVD recorder, it will enter 'virgin mode'. In this mode you will have to set your personal preferences. (See 'virgin mode'.)



English

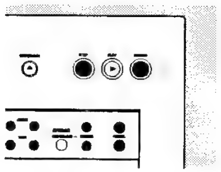
Manual recording

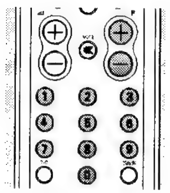
Checking input

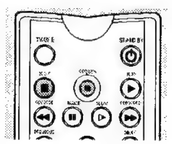
Normally, the DVD recorder displays the contents of the disc on screen. Use the **TUNER** key in order to switch to the internal tuner, or whichever other source is selected, if you want to check the input before starting a recording. Press **TUNER** again to go back to disc mode.

Recording

- Insert a recordable DVD+RW disc.
- Use **CHANNEL ▲** or **CHANNEL ▼** (on the recorder) or **P+**, **P-** or the digit keys **0-9** (on the remote control) to select the programme number (programme name) from which you wish to record.
  ➤ When a TV channel transmits a channel name, it will be shown on the display.







The following programme numbers are provided for recording from external sources:
'EXT1' : TV set via SCART 1 socket
'EXT2' : for recording from external sources via SCART 2 socket
'EXT3' : rear S-video
'EXT4' : rear CVBS
'CAM1': front S-video
'CAM2': front CVBS
'CAM3': front DV.

- Press **RECORD** (on the recorder) or **REC/OTR** (on the remote control).
  ➤ RECORD is shown on the display.
- Press ■ **STOP** to stop recording.
- The Index Picture Screen is updated.
  ➤ MENU UPDATE is shown on the display.
- After a short recording on a new disc, a few minutes will be needed to complete the formatting of the disc.

Direct record

- Make sure 'Direct record' is switched On. (See record settings).
- On the TV set, select the programme number you want make the recording from.
- Press **RECORD** (on recorder) or **REC/OTR** (on remote control) with the DVD recorder switched to standby.

Notes:
- Don't select another programme number on your TV set, until the 'WAIT' on the display of your DVD recorder disappears. This can take up to one minute.
- When 'NOTV' appears on the display, the programme number could not be found. The DVD recorder switches off automatically.
- If your loudspeakers are connected (via an amplifier / receiver) to your DVD recorder, the sound will be delayed relative to the TV picture when recording directly from the TV set.

Manual audio control

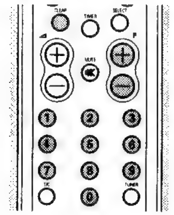
You can control the audio recording level of your DVD recorder manually.

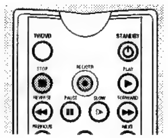
- In tuner mode, press **AUTO/MAN REC VOLUME** on the DVD recorder.
  ➤ The display will show the current audio level and MANUAL appears.

- Adjust the recording level with **MANUAL ▲** or **▼** on the DVD recorder, so that the '0 dB' mark lights up during the loudest parts of the recording.
- You can switch back to automatic audio level control by pressing **AUTO/MAN REC VOLUME** again.
  ➤ The display will show the current disc position and MANUAL disappears.

Note:
When DV input is selected, manual volume control is disabled.

Recording with automatic switch-off (OTR One-Touch Recording)





- Insert a recordable DVD+RW disc.
- Use **CHANNEL ▲** or **CHANNEL ▼** (on the recorder) or **P+**, **P-** or the digit keys **0-9** (on the remote control) to select the programme number (programme name) from which you wish to record.
- Press **RECORD** (on the recorder) or **REC/OTR** (on the remote control) twice.
  ➤ A recording will be made of 30 minutes.
  ➤ The required end time of the recording is shown in the timer box on screen. The remaining recording time is shown in the status box on screen and on the display.

- Press **RECORD** or **REC/OTR** again to obtain a 30 minute increment.
- Shortly after pressing **REC/OTR**, OTR can be cancelled by pressing **CLEAR**.

Timer programming

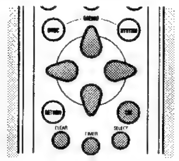
The DVD recorder needs the following information for every programmed recording:
- the date on which the recording is to be made;
- the channel;
- the start and stop time of the recording;
- VPS/PDC on or off;
- the recording mode (HQ, SP, LP or EP).

The DVD recorder stores all the information mentioned above in a timer block. You can programme up to six timer blocks, one month in advance.

What is 'VPS'/'PDC'?
With 'VPS/PDC', the TV station controls the beginning and the length of the programmed recording. This means that the video recorder switches itself on and off at the right time even if a TV programme you have programmed begins earlier or finishes later than expected.
Usually the start time is the same as the VPS/PDC time. If, however, in the TV guide, in addition to a TV programmes start time, a different VPS/PDC time is given, e.g.: '20.15 (VPS 20.14)', you must enter '20.14' as the start time exactly to the minute. If you want to enter a time that differs from the VPS/PDC time, you must switch off 'VPS/PDC'.

When all Timer blocks are full, the options timer programming and ShowView programming cannot be accessed. For clearing a timer block, see 'How to clear a timer block'.

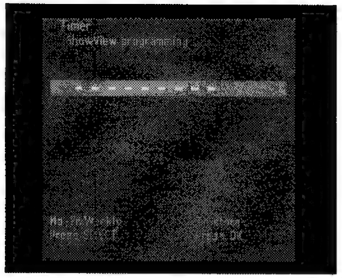
Timer programming with 'ShowView'



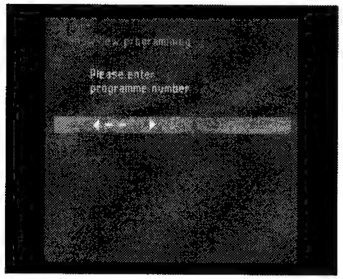
A ShowView programming number is a number of up to nine digits, printed in most TV guides next to the start time of a TV programme.
All the information required for a programming is contained encoded in the ShowView programming number.

- Press **TIMER** on the remote control.
- Select '**ShowView programming**' with △ (up cursor) or ▽ (down cursor).

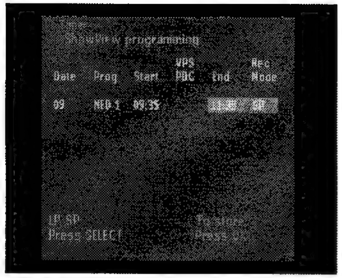
- Press ▷ (right cursor).



- Enter the entire ShowView programming number (up to nine digits) printed in your TV guide next to the start time of a TV programme. If you made a mistake, you can correct it with **CLEAR**.
- Confirm with **OK**.
- If the ShowView system does not recognize the TV channel, the message '**Please enter programme number**' will appear on screen. Select the required programme number (programme name) with ◁ ▷ (left right cursor) and confirm with **OK**.

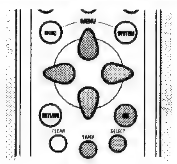


➤ The data will appear on the TV screen.
- Use **SELECT** to select the programming key at daily or weekly intervals. **Mo-Fr**: Recording at daily intervals from Mondays to Fridays inclusive. **Weekly**: Recording at weekly intervals on the same day of the week.
- Press ▷ (right cursor).
- Use **SELECT** to switch VPS/PDC on or off.
  ➤ When VPS/PDC is switched on, the start time is marked with an asterisk.
- Use **SELECT** to select the recording mode (HQ,

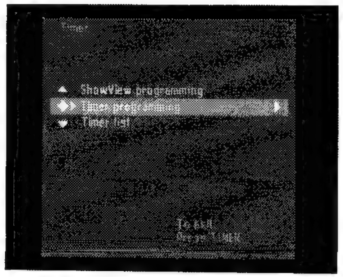


- Confirm with **OK**.
  ➤ The data has been stored in a timer block.
- To end, press **TIMER**.
- Make sure that you inserted a recordable disc. If you inserted a write-protected disc recording will be refused.
- Switch off with ⏻ **STANDBY/ON**.

Timer programming without 'ShowView'

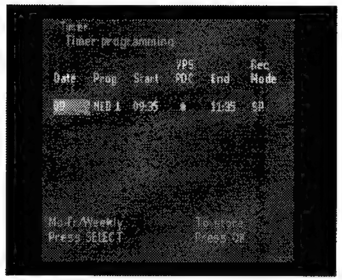


- Press **TIMER** on the remote control.
- Select '**Timer programming**' with △ (up cursor) or ▽ (down cursor).



- Press ▷ (right cursor).
- Enter the date with △ (up cursor) or ▽ (down cursor), or with the digit keys **0-9**.

- If desired, select recording at daily or weekly intervals in the field '**Date**' with **SELECT**. '**Mo-Fr**': Recording to be made from Mondays to Fridays inclusive. '**Weekly**': Recording at weekly intervals on the same day of the week.
- Press ▷ (right cursor).
- Enter the programme number from which you want to record. If you want to record from an external source, select **EXT1**, **EXT2**, **EXT3**, **EXT4**, **CAM1**, **CAM2** or **CAM3** with △▽ (up down cursor).
- Press ▷ (right cursor).
- Enter the Start time with △▽ (up down cursor) or the digit keys **0-9**.
- After entering the Start time, use **SELECT** to switch VPS/PDC on or off. With most TV stations the VPS/PDC time is always the same as the start time.
  ➤ When VPS/PDC is switched on, the start time is marked with an asterisk.
- Press ▷ (right cursor).
- Enter the End time with △▽ (up down cursor) or the digit keys **0-9**.
- Use **SELECT** to choose the recording mode **HQ**, **LP**, **SP** or **EP**.
- If you made a mistake, you can go back with ◁ (left cursor).



- Confirm with **OK**.
  ➤ The data has been stored in a timer block.
- To end, press **TIMER**.
  ➤ Make sure that you inserted a disc without write protection. If you inserted a write-protected (locked) disc, recording will be refused.
- Switch off with ⏻ **STANDBY/ON**.

Programming with 'NEXTVIEW Link'

This DVD recorder is equipped with the function 'NEXTVIEW Link'. If your television is also equipped with this function, you can mark TV programmes on the television for programming. These TV programmes will automatically be transmitted to a timer block on the DVD recorder. If you clear the marking of the TV programme on the television, the corresponding timer block on the DVD recorder will also be cleared.
For more information, read the instruction manual of your TV set.

If a timer setting is incorrect

The following warnings can be displayed in the timer menu:

Collision
recording programme overlaps with another recording programme.
Solution:
- Ignore by pressing **TIMER**. The programme with the earlier start time will be recorded completely before the later programme starts.
- Edit one or both timers.
- Delete one of the recording programmes.

Please enter programme number
The ShowView system does not recognize the TV channel.
Solution:
- Select the required programme number (programme name) with ◁ or ▷ (left right cursor).
- Confirm with **OK**.

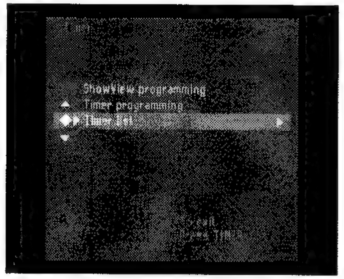
ShowView number wrong
You entered an incorrect ShowView programming number or the incorrect date.
Solution:
- Repeat the entry or end by pressing **TIMER**.

Weekend programming - not possible
Date was incorrectly entered. Daily programming can only be used for recordings to be made from Mondays to Fridays inclusive.

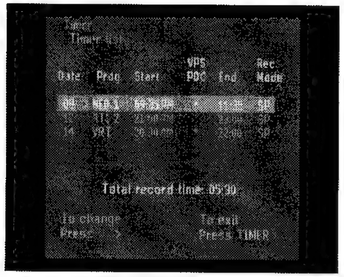
Memory full
The maximum number of recording programmes is used.
Solution:
- Delete one of the recording programmes.

How to check or alter a timer block

- Press **TIMER** on the remote control.
- Select '**Timer list**' with ▽ or △ (down up cursor).

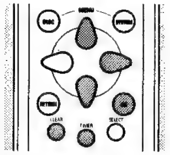


- Press ▷ (right cursor).



- Select the timer block you want to check or alter with ▽ or △ (down up cursor).
- Press ▷ (right cursor).
- Select what you want to check or alter with ◁ or ▷ (left right cursor).
- Alter data with ▽ or △ (down up cursor) or with the digit keys **0-9**.
- Confirm with **OK**.
- To end, press **TIMER**.
- Switch off by pressing ⏻ **STANDBY/ON**.

How to clear a timer block



- Press **TIMER** on the remote control.
- Select **Timer list** with ▽ or △ (down up cursor).
- Press ▷ (right cursor).
- Select the timer block you want to clear with ▽ or △ (down up cursor).
- Press **CLEAR**.
- Confirm with **OK**.
- Switch off by pressing **TIMER**.

Playback

Playing a pre-recorded DVD-Video disc

Some DVD discs are produced in a way that requires specific operation or allows only limited operation during playback. In these cases the recorder may not respond to all operating commands. When this occurs, please refer to the instructions in the disc inlay. When a ⊠ appears on the TV screen, the operation is not permitted by the recorder or the disc.

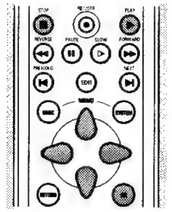
- Insert a pre-recorded DVD-Video disc.
  ➤ When '**autoresume**' is set to '**On**' (see 'User Preferences') playback starts automatically from the point where it was stopped, the last time the disc was played.
  ➤ When '**autoresume**' is set to '**Off**', the disc will play from the start of the disc. You can however resume play from the point at which you stopped, the last time the disc was played, by pressing ▶ **PLAY** when ▶ appears on screen.
  ➤ The currently playing title and chapter number are displayed on the recorder display. The elapsed time is shown also.

Notes:
- Since it is usual for DVD movies to be released at different times in different regions of the world, all players have region codes and discs can have an optional region code. If you load a disc of a different region code to your recorder, you will see the region code notice on the screen. The disc will not play, and should be unloaded.
- The region code is stated on a label on the back side of your recorder.
- Regional coding is not applicable for recordable DVD discs.

- The disc may invite you to select an item from a menu. If the selections are numbered, press the appropriate numerical key; if not, use the ▽ △ ▷ ◁ (down up right left cursor) keys to highlight your selection, and press **OK**.

Note:
*During playback you can display and enter the menu by pressing **DISC MENU**.*

- To stop play at any time, press ■ **STOP**.
  ➤ The default screen will appear, giving information about the current status of the recorder.



Playing a (Super) Video CD disc

- Insert a (Super) Video CD.
  ➤ When '**autoresume**' is set to '**On**' (see 'User Preferences') playback starts automatically from the point where it was stopped, the last time the disc was played.
  ➤ The disc may invite you to select an item from a menu. If the selections are numbered, press the appropriate numerical key **0-9**.
- To stop play at any time, press ■ **STOP**.
  ➤ The default screen will appear.

Playing a DVD+RW disc

RW DVD+ReWritable

- Insert a DVD+RW disc.
  ➤ If the inserted disc is write-protected, playback starts automatically otherwise the Index Picture Screen appears.
- Press ▶ **PLAY.**
  ➤ Playback starts automatically from the point where it was stopped the last time the disc was played or recorded. If you want to start playback from the beginning of the disc, you can do so via the Index Picture Screen (see 'Index Picture Screen').
  ➤ If the disc is a new blank disc, the display will show 'EMPTY DISC'.
- With ⏮ **PREVIOUS** and ⏭ **NEXT** you can go to the previous or next title.
- To stop playback at any time, press ■ **STOP.**
  ➤ You return to the Index Picture Screen.

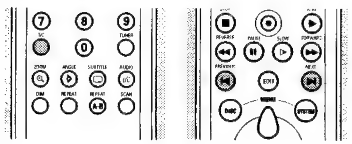
General features

RW DVD+ReWritable | DVD VIDEO | COMPACT disc DIGITAL VIDEO

Note: Unless stated otherwise, all operations described are based on remote control operation. A number of operations can also be carried out via the system menu bar on the screen. (see 'System menu bar operation')

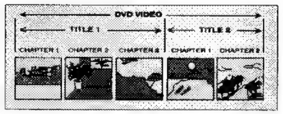
Moving to another title/track

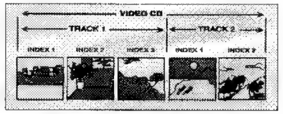
When a disc has more than one title or track, you can move to another title as follows:



- Press **T/C**.
- Press ⏭ **NEXT** during play to step forward to the next title.
- Press ⏮ **PREVIOUS** during play to return to the beginning of the current title. Rapidly press ⏮ **PREVIOUS** twice to step back to the previous title.
- To go directly to any title or track, enter the title number using the numerical keys **0-9**.

Note:
- If the number has more than one digit, press the keys in rapid succession.
- If the system menu bar is on screen, make sure the T icon is selected.





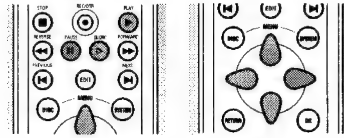
Moving to another chapter/index

When a title on a disc has more than one chapter or a track has more than one index, you can move to another chapter/index as follows:

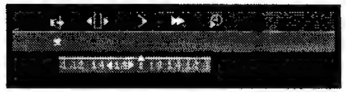
- Press ⏭ **NEXT** during play to select the next chapter/index.
- Press ⏮ **PREVIOUS** during play to return to the beginning of the current chapter/index. Rapidly press ⏮ **PREVIOUS** twice to step back to the previous chapter/index.
- To go directly to any chapter or index, enter the chapter or index number using the numerical keys **0-9**.

Note:
- If the number has more than one digit, press the keys in rapid succession.
- If the system menu bar is on screen, make sure the C icon is selected.

Slow Motion



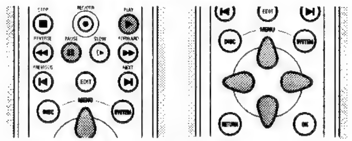
- Select (Slow motion) in the system menu bar.
- Use the ▽ (down cursor) key to enter the slow motion menu.
  ➤ The recorder will now go into pause mode.



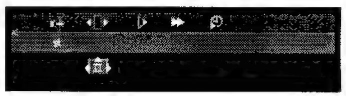
- Use the ◁ ▷ (left right cursor) keys to select the required speed: -1, -1/2, -1/4 or -1/8 (backward); 1/8, 1/4, 1/2 or 1 (forward).
- Select 1 to play at normal speed again.
- If ⏸ **PAUSE** is pressed, the speed will be set to 0.
- Press ▶ **PLAY** to exit slow motion mode.
- Press △ (up cursor) to delete the slow motion menu.

You can also select Slow motion speeds by using the ▷ **SLOW** key on the remote control.

Still Picture and Step Frame



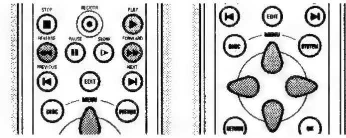
- Select (picture by picture) in the system menu bar.
- Use the ▽ (down cursor) key to enter the picture by picture menu.
  ➤ The recorder will now go into pause mode.



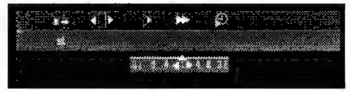
- Use ◁ ▷ (left right cursor) keys to select previous or next picture.
- Press ▶ **PLAY** to exit picture by picture mode.
- Press △ (up cursor) to exit the picture by picture menu.

You can also step forward by using the ⏸ **PAUSE** repeatedly on the remote control.

Search



- Select (Fast motion) in the system menu bar.
- Use the ▽ (down cursor) keys to enter the fast motion menu.



- Use the ◁ ▷ (left right cursor) keys to select the required speed: -32, -8 or -4 (backward); 4, 8, 32 (forward).
- Select 1 to play at normal speed again.
- Press ▶ **PLAY** to exit fast motion mode.
- Press △ (up cursor) to delete the fast motion menu.

To search forward or backward through different speeds, you can also press ◀◀ **REVERSE** or ▶▶ **FORWARD** again.

Repeat

DVD Discs - Repeat chapter/title/disc

- To repeat the currently playing chapter, press **REPEAT**.
  ➤ chapter appears on screen.
- To repeat the currently playing title, press **REPEAT** a second time.
  ➤ title appears on screen.
- To repeat the entire disc, press **REPEAT** a third time.
  ➤ repeat appears on screen.
- To exit repeat mode, press **REPEAT** a fourth time.

Video CDs - Repeat track/disc

- To repeat the currently playing track, press **REPEAT**.
  ➤ track appears on screen.
- To repeat the entire disc, press **REPEAT** a second time.
  ➤ repeat appears on screen.
- To exit repeat mode, press **REPEAT** a third time.

Repeat A-B

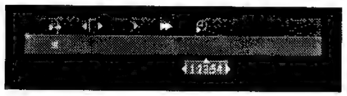
To repeat or loop a sequence in a title:
- Press **REPEAT A-B** at your chosen starting point;
  ➤ [A-] appears on screen.
- Press **REPEAT A-B** again at your chosen end point;
  ➤ [A-B] repeat appears on screen, and the repeat sequence begins.
- To exit the sequence, press **REPEAT A-B**.

Scan

Plays the first 10 seconds of each chapter/index on the disc.
- Press **SCAN**.
- To continue play at your chosen chapter/index, press **SCAN** again or press ▶ **PLAY**.

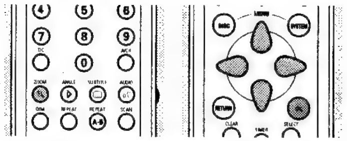
Time search

The Time Search function allows you to start playing at any chosen time stamp.
- Select (Time Search) in the system menu bar.
- Press ▽ (down cursor).
  ➤ The recorder will now go into pause mode.
  ➤ A time entry box appears on the screen showing the elapsed playing time of the current disc.

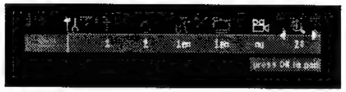


- Use the digit keys **0-9** to enter the required start time. Enter hours, minutes and seconds in the box.
  ➤ Each time an item has been entered, the next item will be highlighted.
- Press **OK** to confirm the start time.
  ➤ The time entry box will disappear and play starts from the selected time position.

Zoom



The Zoom function allows you to enlarge the video image and to pan through the enlarged image.
- Select 🔍 Zoom in the system menu bar.
- Press ▽ △ (down up cursor) to activate the Zoom function and select the required zoom factor; 1.33 or 2 or 4.
  ➤ The recorder will go into pause mode.
  ➤ The selected zoom factor appears below the Zoom icon in the system menu bar and 'Press OK to pan' appears below the system menu bar.



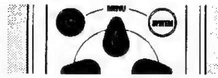
  ➤ The picture will change accordingly.
- Press **OK** to confirm the selection.
  ➤ The panning icons appear on the screen: ▽ △ ▷ ◁ (down up right left cursor) and **OK**.
- Use the ▽ △ ▷ ◁ (down up right left cursor) keys to pan all over the screen.
- When **OK** is pressed only the zoomed picture will be shown on the screen.
- If you wish to zoom at any moment, press 🔍 Zoom and select the required zoom factor as described above.
- Press ▶ **PLAY** to exit zoom mode.

Special DVD-Video features

Menus on the disc

For titles and chapters, selection menus may be included on the disc.
The DVD's menu feature allows you to make selections from these menus. Press the appropriate numerical key; or use the ▽ △ ▷ ◁ (down up right left cursor) keys to highlight your selection, and press **OK**.

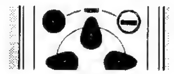
Title menus



- Press **DISC MENU**.
  ➤ If the current title has a menu, this appears on the screen. If no menu is present in the title, the disc menu will be displayed.
- The menu can list camera angles, spoken language and subtitle options, and chapters for the title.
- To exit the title menu, press **DISC MENU** again.

Note: Most DVD discs do not have seperate disc and title menus, but only a disc menu.

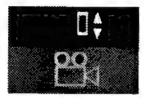
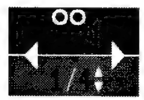
Disc menu

- Press **T/C** followed by **DISC MENU**.
  ➤ The disc menu is displayed.
- To remove the disc menu, press **DISC MENU** again.

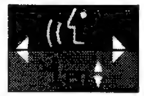
Camera Angle

If the disc contains sequences recorded from different camera angles, the angle icon appears, showing the number of available angles, and the angle being shown. You can then change the camera angle if you wish.

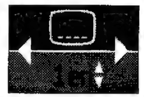
- Use the ▽ △ keys to select the required angle in the angle icon.
- To go to any angle directly, enter the angle number using the numerical keys **0-9**.
  ➤ After a small delay, play changes to the selected angle. The angle icon remains displayed until multiple angles are no longer available.

Changing the audio language

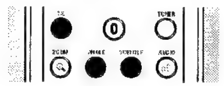


- Select (Audio) in the system menu bar.
- Press **AUDIO** or ▽ △ (down up cursor) repeatedly to step through the different languages.
- You can enter the required language number directly using the numerical keys **0-9**.

Subtitles

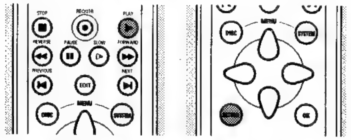


- Select (Subtitle) in the system menu bar.
- Press **SUBTITLE** or ▽ △ (down up cursor) repeatedly to step through the different subtitles or to switch subtitles off.
- You can enter the required subtitle number directly using the numerical keys **0-9**.



Special VCD features

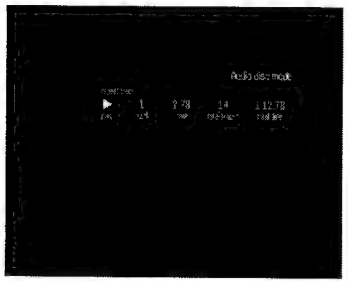
Playback Control (PBC)



- Make sure PBC is switched On. See 'User Preferences-features settings'.
- Load a (Super) Video CD with PBC and press ▶ **PLAY**.
  ➤ The PBC menu appears on screen.
- Go through the menu with the keys indicated on the TV screen until your chosen passage starts to play. If a PBC menu consists of a list of titles, you can select a title directly.
- Enter your choice with the numerical keys **0-9**.
- Press **RETURN** to go back to the previous menu.

Playing an audio CD

- Insert the disc.
  ➤ After loading the disc, playback starts automatically.
  ➤ If the TV set is on, the Audio CD screen appears.
  ➤ During play, the current track number and its elapsed playing time will be shown on the screen and the recorder display.

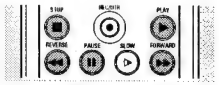


- To stop play at any time, press ■ **STOP**.
  ➤ The number of tracks and the total playing time will be shown on the screen and the recorder display.

Pause

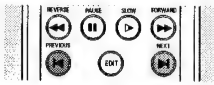
- Press **II PAUSE** during play.
- To return to play, press ▶ **PLAY**.

Search

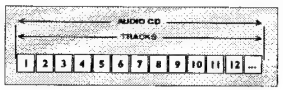


- To search forwards or backwards through the disc at 4x normal speed, press ◀◀ **REVERSE** or ▶▶ **FORWARD**.
  ➤ Search begins.
- To step up to 8x normal speed, press ◀◀ **REVERSE** or ▶▶ **FORWARD** again.
  ➤ Search goes to 8x speed, and the sound is muted.
- To return to 4x normal speed, press ◀◀ **REVERSE** or ▶▶ **FORWARD** again.
- If the TV set is on, search speed and direction are indicated on the screen each time ◀◀ **REVERSE** or ▶▶ **FORWARD** is pressed.
- To end the search, press ▶ **PLAY** or ■ **STOP** as desired.

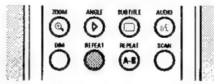
Moving to another track



- Press ▶I **NEXT** during play to step forward to the next track.
- Press I◀ **PREVIOUS** during play to return to the beginning of the current track. Rapidly press I◀ **PREVIOUS** twice to step back to the previous track.
- To go directly to any track, enter the track number using the numerical keys **0-9**.

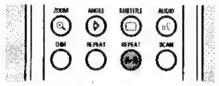


Repeat track/disc



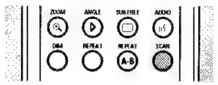
- To repeat the currently playing track, press **REPEAT**.
  ➤ Repeat track appears on screen.
- To repeat the entire disc, press **REPEAT** a second time.
  ➤ Repeat disc appears on screen.
- To exit repeat mode, press **REPEAT** a third time.

Repeat A-B



To repeat or loop a sequence:
- Press **REPEAT A-B** at your chosen starting point;
  ➤ Repeat A appears on screen.
- Press **REPEAT A-B** again at your chosen end point;
  ➤ Repeat A-B appears on the display, and the repeat sequence begins.
- To exit the sequence, press **REPEAT A-B** again.

Scan



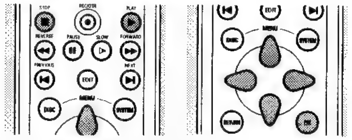
Plays the first 10 seconds of each track on the disc.
- Press **SCAN**.
- To continue play at your chosen track, press **SCAN** again or press ▶ **PLAY**.

Access control

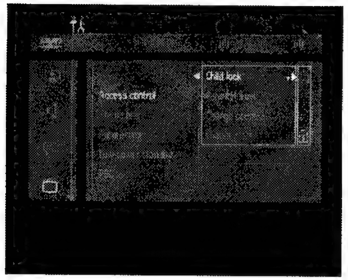
Child Lock (DVD and VCD)

When activating Child lock, only discs that are authorised can be played without PIN code.
The recorder memory maintains a list of 50 authorized ('Child safe') disc titles. A disc will be placed in the list when 'Play Always' is selected in the 'Child protect' dialog. Each time a 'Child safe' disc is played it will be placed on top of the list. When the list is full and a new disc is added, the least recently used disc will be removed from the list.

Activating/deactivating the child lock



- Select **Access control** in the features menu using ▽ △ (down up cursor) and press ▷ (right cursor).
- Enter a 4-digit PIN code of your own choice using the digit keys **0-9**.
- Enter the code a second time.
- Move to **Child lock** using ▽ △ (down up cursor).
- Move to 🔒 / 🔓 using the ▷ (right cursor) key.



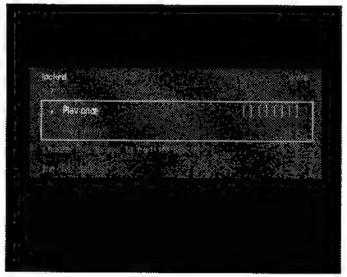
- Select 🔒 using ▽ △ (down up cursor).
- Press **OK** or ◁ (left cursor) to confirm and press **SYSTEM MENU** to exit the menu.
  ➤ Now unauthorized discs will not be played unless the 4-digit code is entered.
- Select 🔓 to deactivate the Child Lock.

Note: Reconfirmation of the 4-digit PIN code is necessary when: The code is entered for the very first time (see above); The code is changed (see 'Changing the 4-digit code'); The code is cancelled (see 'Changing the 4-digit code'); Both Child Lock and Parental Control are switched Off and the code is requested.

Authorizing discs when Child Lock is activated

- Insert the disc.
  ➤ The 'Child protect' dialog will appear. You will be asked to enter your secret code for '**Play once**' or '**Play always**.' If you select '**Play once**', the disc can be played as long as it is in the recorder and the recorder is in the On position. If you select '**Play always**', the disc will become Child safe (authorized) and can always be played even if the Child lock is set to **On**.

Note: Double sided DVD discs may have a different ID for each side. In order to make the disc 'Child safe', each side has to be authorized.
Multi volume VCD disc may have a different ID for each volume. In order to make the complete set 'Child safe', each volume has to be authorized.



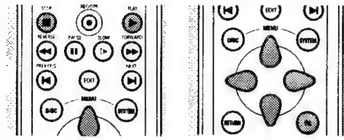
Securing discs

- Insert the disc.
  ➤ Playback starts automatically.
- Press **■ STOP** while ☺ is visible.
  ➤ ☹ will appear and the disc is now banned i.e. it is not Child safe any longer.

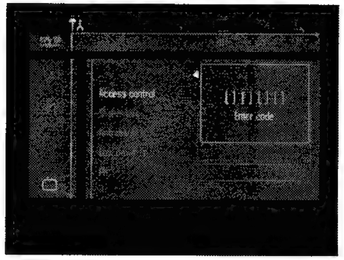
Parental Level (DVD-Video only)

Movies on pre-recorded DVD discs may contain scenes not suitable for children. Therefore discs may contain 'Parental Control' information which applies to the complete disc or to certain scenes on the disc.
These scenes are rated from 1 to 8 and alternative, more suitable scenes are available on the disc. Ratings are country dependent. The 'Parental Control' feature allows you to prevent discs from being played by your children or to have certain discs played with alternative scenes.

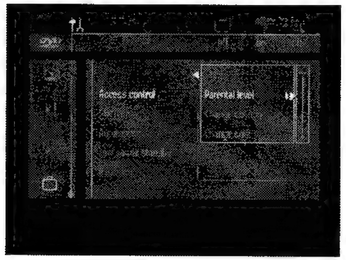
Activating/Deactivating Parental Control



- Select **Access control** in the features menu using ▽ △ (down up cursor) and press ▷ (right cursor).



- Enter your 4-digit PIN code using the digit keys **0-9**. If necessary enter the code a second time.
- Move to **Parental level** using ▽ △ (down up cursor).
- Move to the Value Adjustment bar using ▷ (right cursor).



- Use the ▽ △ (down up cursor) keys or the numerical keys **0-9** on the remote control to select a rating from 1 to 8 for the disc inserted.

Rating 0 (displayed as '– –'):
Parental Control is not activated. The disc will be played in full.
Ratings 1 to 8 (1 = childsafe - 8 = adults only):
The disc contains scenes not suitable for children. If you set a rating for the recorder, all scenes with the same rating or lower will be played. Higher rated scenes will not be played unless an alternative is available on the disc. The alternative must have the same rating or a lower one. If no suitable alternative is found, play will stop and the 4-digit code has to be entered.

- Press **OK** or ◁ (left cursor) to confirm and press **SYSTEM MENU** to exit the menu.

Country

- Select **Access control** in the features menu using ▽ △ (down up cursor) and press ▷ (right cursor).
- Enter the four digit PIN code.
- Move to **Change country** using ▽ (down cursor).
- Press ▷ (right cursor).
- Select a country using ▽ △ (down up cursor).
- Press **OK** or ◁ (left cursor) to confirm and press **SYSTEM MENU** to exit the menu.

Changing the 4-digit code

- Select **Access control** in the features menu using ▽ △ (down up cursor) and press ▷ (right cursor).
- Enter the old code.
- Move to **Change code** using ▽ (down cursor).
- Press ▷ (right cursor).
- Enter the new 4-digit PIN code.
- Enter the code a second time and reconfirm with **OK**.
- Press **SYSTEM MENU** to exit the menu.

Note: If you forgot your code, press **■ STOP** *four times while in the access control PIN code box and exit with* **OK**. *Access control is now switched off. You can then enter a new code as described above.*

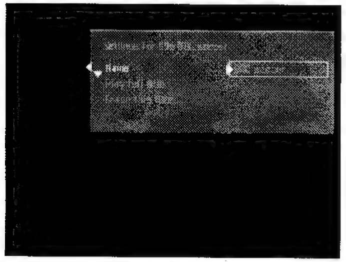
Managing disc content

Title settings

For each title on the discs the default settings can be changed to your personal preference in the title settings menu.

Changing the title name

- In the Index Picture Screen, select the required title with ▽ △ (down up cursor).
- Press ▷ (right cursor) to enter the title settings menu.



- Enter the new name. A name may contain a maximum of 64 characters.
- Use ◁ ▷ (left right cursor) for the position of the characters. Use ▽ △ (down up cursor) to change characters.
- Use **SELECT** to toggle between capitals and lower case characters.
- Confirm by pressing **OK**.

Play full title

- In the Index Picture Screen, select the required title with ▽ △ (down up cursor).
- Press ▷ (right cursor) to enter the title settings menu.
- Select 'Play full title'.

When this item is selected the title will be played in full, including hidden chapters. Follow the instructions on the screen. (See 'Operation - managing disc content - Current chapter')

Erasing a title

You may simply erase a title by recording over it, but if you want to erase the whole title instantly, do the following:

- In the Index Picture Screen, select the required title with ▽ △ (down up cursor).
- Press ▷ (right cursor) to enter the title settings menu.
- Select 'Erase this title'.
  ➤ The message 'This will completely erase this title', 'Press OK to confirm' is shown.
- Press **OK** to confirm.
  ➤ 'Erasing title...' is shown until the action is completed.
  ➤ After the title has been erased, the Index Picture Screen will show an empty space instead. If there was an empty space in front of or behind this title, then these are combined into one empty space. Empty spaces of less then one minute will not be shown.

Disc Info Screen

- When on the Index Picture Screen, press ■ **STOP** or keep ⏮ **PREVIOUS** pressed for about two seconds.
  ➤ You are now on Title 1.
- Press △ (up cursor).
  ➤ You enter the Disc Info Screen.
- Press ▽ (down cursor) to exit the Disc Info Screen.

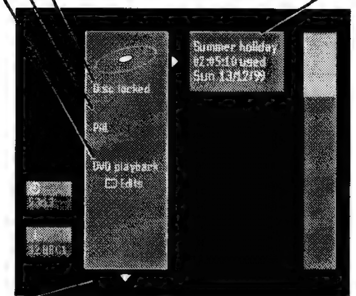
The Disc Info Screen contains the following information:

Compatibility status
- indicates compatibility of any edits with DVD players

Video system
- PAL or SECAM
- NTSC

Disc lock status
- Indicates whether the disc is write-protected

Disc description
- disc name
- total recording duration
- date of last recording



Cue to go back to the Index Picture Screen

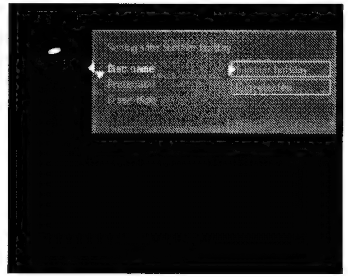
Disc Settings

For each disc the settings can be changed to your personal preference in the disc settings menu.

- In the Disc Info Screen press ▷ (right cursor).
  ➤ You will now enter the 'disc settings' menu.

Changing the Disc Name

- In the Disc Info Screen press ▷ (right cursor).
  ➤ You will now enter the 'disc settings' menu.



- Enter the new name. A name may contain a maximum of 64 characters.
- Use ◁ ▷ (left right cursor) for the position of the characters. Use the ▽ △ (down up cursor) keys to change characters.
- Use **SELECT** to toggle between capitals and lower case characters.
- Confirm by pressing **OK**.

Protection of recordings

- In the Disc Info Screen press ▷ (right cursor).
  ➤ You will now enter the 'disc settings' menu.
- Select 'Protection' and press ▷ (right cursor).
- Select 'Protected' with ▽ △ (down up cursor).
- Press **OK** on the remote control to confirm.
  ➤ No further changes can be made to the disc. It will also disable most title/disc manipulation screen entries, as well as the complete edit menu.
  ➤ Future editing is only possible after resetting the Protection feature to 'Unprotected' again.

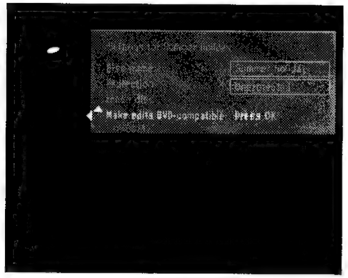
Erasing a disc

- In the Disc Info Screen press ▷ (right cursor).
  ➤ You will now enter the 'disc settings' menu.
- Select 'Erase disc' and press **OK**.
  ➤ The message 'This will erase all titles' is displayed.
- Press **OK** to confirm or ◁ (left cursor) to cancel.
  ➤ 'Erasing disc' is shown until the action is completed.
  ➤ After the disc has been erased the Index Picture Screen will show the free space on the disc.

Making your edits DVD-compatible

If one or more titles have been edited (see 'Favourite Scene Selection'), then the edits will play on your DVD recorder, but a DVD player may show the original versions instead of the edits. You can prepare your discs so that also a DVD player will show the edited version.

- If the Disc Settings menu shows the option 'Make edits DVD-compatible', select this option. If the menu does not show this option, then your disc is already compatible, and no conversion is needed.



- Press **OK** on the remote control to confirm.
  ➤ The messages 'This will take ...' and 'Press OK to confirm' will appear to indicate how long the action will take.
- Press **OK** on the remote control to confirm.
  ➤ 'Processing...' and a progress bar are shown until the action is completed.

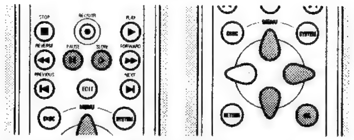
Favourite Scene Selection

With the **EDIT** key on the remote control the Favourite Scene Selection (FSS menu) for editing functionality can be called up. The basic function of any edit operations is to improve accessibility and handling of your recordings. For instance: scenes you do not want to see during playback (e.g. commercials during a movie) can be marked as chapters and made hidden. During playback you will see your recording without the hidden chapters as one sequence.

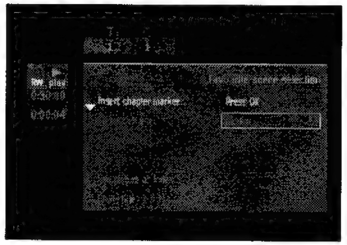
Note: In between the scenes the picture may freeze for a short moment.

Each title consists of chapters. With the FSS menu any chapter can be made hidden or made visible again. Normally, during recording, chapter markers are inserted automatically every five to six minutes (this setting can be changed in the record settings menu). After the recording is finished, you can manually add and remove chapter markers via the FSS menu. Both automatically generated and manually inserted chapter markers can be removed.

Edit in playback mode



- Press the **EDIT** key on the remote control.
  ➤ The video image is overlayed with a transparant edit menu. Title and chapter information appear in an information box at the top of the screen.



- Use ▽ or △ (down up cursor) to toggle through the menu's functions:

Insert chapter marker

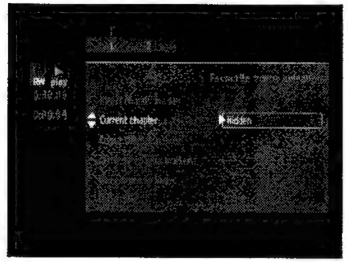
To insert a chapter marker on the current position of the title that is playing.

- Press **OK** on the remote control to insert a marker.

The maximum number of chapter markers per title is 99. Per disc the maximum number of chapter markers is 254. When this maximum is reached the on-screen message 'Too many chapters' appears. You have to delete some, before inserting new chapter markers.

Hide chapters

Initially all chapters are visible. You can hide chapters or make them visible again on playback. In edit mode however hidden chapters are displayed in a dimmed mode.



- Select Visible or Hidden with the ▷ (right cursor) keys.
- Press **OK** on the remote control to confirm.

Delete chapter marker

To delete the chapter marker at the beginning of the current chapter.

- Press **OK** on the remote control to confirm.
  ➤ 'Deleting markers' will appear.

Delete all markers in title

To delete all chapter markers (manually and automatically generated) for this title.

- Press **OK** on the remote control to confirm.
  ➤ 'Deleting markers' will appear.

Use picture as index

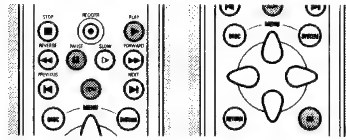
To define the current video frame as a miniature picture to be used for this title's entry in the Index Picture Screen.

- You can use **II PAUSE** and/or ▷ **SLOW** to accurately choose the desired picture.
- Press **OK** on the remote control to confirm.
  ➤ 'Updating menu'.

After editing, the modified version of a title is the default playback version. The original can be accessed via the 'Play full title' option in the title settings menu. Other DVD players may still play the original. To guarantee that the edited version will play on these DVD players, choose 'Make edits DVD-compatible' in the disc settings menu.

Divide a title

If you want to divide one title into two seperate titles, do the following:



- On the Index Picture Screen, select the title you want to divide.
- Press ▶ **PLAY**.
- Go to the point where you want to divide the title and press **II PAUSE**.
- Press **EDIT**.
  ➤ The Favourite Scene Selection menu is shown.
- Select 'Divide title'.

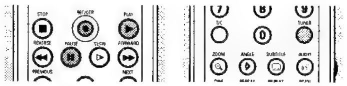
- Press **OK** on the remote control to confirm.
  ➤ 'Dividing title...' is shown until the action is completed. This divide operation cannot be undone.

The Index Picture Screen will show two titles instead of one. Both will have the same name. If you want to change the name, you can do so in the title settings menu. For one of the two resulting titles, a new index picture is created.

If you want to divide one title into more than two titles, use the above procedure several times.

English

Append recording



If you want to append a video recording to an earlier recorded title, do the following.

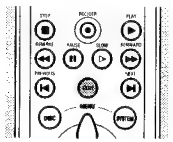
- On the Index Picture Screen, select the title to which you want to add a video recording.
- Press ▶ **PLAY**.
- At the point where you want to append the title press **II PAUSE**.
- To monitor the video input you may press **TUNER**.
- Press **RECORD** (on the recorder) or **REC/OTR** (on the remote control).

The video recording will now be appended from this point. Video material beyond this point is overwritten. This may include titles following the current title.

Any remaining video material that is not overwritten, which may include the last part of the original title, is maintained. You can access these titles from the Index Picture Screen.

Edit in record mode

- Press the **EDIT** key on the remote control during recording.
  ➤ A chapter marker is inserted at the current position. 'Inserting marker' appears in the status box at the top of the screen. The maximum number of chapter markers per title is 99. Per disc the maximum number of chapter markers is 254. When this maximum is reached the on-screen message 'Too many chapters' appears. You have to delete some, before inserting new chapter markers.



Troubleshooting

English

If it appears that the DVD recorder is faulty, first consult this checklist. It may be that something has been overlooked. Under no circumstances attempt to repair the system yourself; this will invalidate the warranty. Look for the specific symptom(s). Then perform only the actions listed to remedy the specific symptom(s).

Symptom	Remedy
The recorder does not respond to the remote control	The remote control may be configured for a second DVD recorder. Hold **SELECT+1** pressed simultaneously to revert to DVD recorder 1. Aim the remote control directly at the sensor on the front of the recorder. Avoid all obstacles which may interfere with the signal path. Inspect or replace the batteries.
No power	Check if both plugs of the mains cord are properly connected. Check if there is power at the AC outlet by plugging in another appliance.
No picture	Check if the TV set is switched on. Check the video connection.
Distorted picture distorted sound	Check the disc for fingerprints and clean with a soft cloth, wiping from centre to edge. Sometimes a small amount of picture distortion may appear. This is not a malfunction.
Recorder does not play disc	Ensure the disc label is upwards and that the right disc type is inserted. Clean the disc. Check if the disc is defective by trying another disc. Check if the region code of the disc matches the region code of the recorder. (pre-recorded DVD discs only). See 'playing a pre-recorded DVD-Video disc'. Check if Child Lock is activated.
No sound	Check audio connections. If using a HiFi amplifier, try another sound source.
Distorted sound from HiFi amplifier	Check to make sure that no audio connections are made to amplifier phono input. Check to make sure that analogue input of the amplifier is not connected to the digital output of DVD the recorder.
Distorted or black and white picture with DVD or Video CD disc	The disc format is not according to the TV set used (PAL/NTSC).
No audio at digital output	Check the digital connections. Check the settings menu to make sure that the digital output is set to on. Check if the audio format of the selected audio language matches your receiver capabilities.
Keys on the DVD recorder do not work	Disconnect and reconnect the DVD recorder from the mains. If this does not solve the problem. Check if the remote control still works. If so, the recorder is probably in trade mode. Disconnect the recorder from the mains and reconnect it while holding ▲ **OPEN/CLOSE** and ■ **STOP** pressed.
Recorder does not respond to all operating commands during playback	Some operations are not permitted by the disc. Refer to the instructions in the disc inlay.

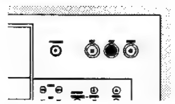
No new title can be recorded	Check if the maximum number of titles has been reached (message: 'too many titles' on screen). If so, delete a title next to a free space. Check if the disc is write protected. If so, unlock the disc in the disc settings menu (message: 'Disc locked' on screen).
Two languages are 'mixed' when recording from a stereo VCR	When the TV set does not automatically detect the dual-language signal, use left/right audio balance on the TV set to amplify the one or the other language.
The disc cannot be erased because the Index Picture Screen does not appear	Open the tray while leaving the disc in. Hold **CLEAR** pressed for around 5 seconds. The tray closes and the disc will be erased.
The Index Picture Screen does not appear but the titles on the disc can still be played	Take out the disc. Clear the disc. Insert the disc. Choose 'Adapt to own disc format' (See 'User Preferences - Features').
A DVD player shows the Index Picture Screen but does not react to the ▶ PLAY key	Press ■ **STOP** to exit the Index Picture Screen, then press ▶ **PLAY**.

Diagnosis programme

If the recorder is still faulty you can start the Diagnosis Programme in the recorder.

You can operate the Diagnosis Programme by following the instructions step by step.

Instructions



- Unplug the power cord of the recorder.
- Press the ▶ **PLAY** key and keep them pressed while you plug the recorder.
  ➤ On the display the message BUSY appears together with a counter. This counter indicates the termination of the test when zero is reached.
  ➤ After a few minutes the message on the local display changes over from BUSY to FAIL or to PASS.
  ➤ If the message FAIL appears on the display, there is apparently a failure in your recorder and your recorder should be repaired.
- Consult your dealer or the Philips Customer Care Centre for the nearest Service Repair Shop in your country. The phone number is given in your warranty booklet.
- If the message PASS appears on the display, there is apparently no failure in your recorder. In this case the failure can be caused by incorrect interpretation of the operating instructions or a wrong disc is used or your recorder is not correctly connected. In this case you should consult your dealer or the Philips Customer Care Centre for further assistance in solving the problem.
- If the problem remains, then consult your Philips Customer Care Centre.

System limitations

A DVD+RW disc may not play on certain DVD Video players.

A DVD+RW video disc that has been recorded on a different type or brand of recorder can be played, but may not provide all features commonly available to DVD+RW discs, such as the on-screen disc bar, the disc settings menu, the title settings menu, and editing. Refer to 'Adapt disc format'. If the disc is write-protected, the status cannot be changed.

When using manual recording, the DVD recorder will warn before adapting the format of the disc or removing non-video data. When using timer recording however, the DVD recorder will always start to record, unless the disc is write-protected. Menus, edits and other data recorded on a different device (e.g. a PC) may be lost.

Because of the Variable Bit Rate, a title map take up less or more space than the overwritten title, even though the duration is the same. As a result, a part of the next title may be lost. The maximum deviation is five minutes.

After a power interruption during recording, the Index Picture Screen will may not match with the actual video content on the disc. The last recorded title may be lost.

Glossary

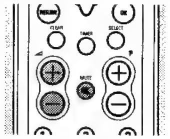
This section explains most important terms, abbreviations, and acronyms used in this document.

Term	Explanation
AC-3	Audio Coding 3, also known as Dolby Digital. Multi-channel digital audio compression system from Dolby Labs.
A/V	Audio/Video
Chapter	A part of a title.
Disc Bar	A graphical representation of the contents of a (DVD+RW) disc.
Disc Pointer	An arrow indicating the current playback/recording position on the DVD+RW disc, displayed on the 'disc bar'.
DTS	Digital Theater System. A high-end Multi-channel audio compression format.
DV	Digital Video. A camcorder format for high-quality video, different from MPEG. It is converted into MPEG 2 Video when recorded on DVD+RW
DVD	Digital Versatile Disc
DVD+RW	DVD+ReWritable. The disc standard used by the DVD recorder.
EasyLink	If your TV set and your video recorder are equipped with this feature, they can exchange information to adjust certain settings to each other, such as the TV channel order and other user preferences.
I.LINK	Also known as 'FireWire' and 'IEEE 1394'. A cable for transfer of high-bandwidth digital signals, as used by Digital Video camcorders.
Index Picture Screen	A screen that gives an overview of a DVD+RW disc, wih 'index pictures' that each represent a recording.
MPEG	Motion Picture Experts Group. A collection of compression systems for digital audio and video.
NEXTVIEW Link	A system that enables easy programming of a video recorder via a TV set. Also see EasyLink.
NICAM	System for reception of digital stereo TV sound.
NTSC	See TV system.
OSD	On-screen Display. The 'user interface' by which you can control the DVD recorder via the TV screen.
OTR	One-Touch Recording. With this feature you can easily start a recording (by pushing just one button) and select the switch-off time in intervals of 30 minutes.
PAL	See TV system.
PBC	Playback Control. A special feature on a VCD 2.0 or Super VCD disc that enables interactive use.
PCM	Pulse Code Modulation. A digital audio encoding system.
PDC	Program Delivery Control
RGB	Red-Green-Blue. A top-quality video connection where red, green and blue components of a video signal are carried through separate wires.
SCART cable	Also known as Euro-AV cable. This standard cable is an easy way to connect various AV devices and televisions. In addition to audio and video it can carry control signals.
SECAM	See TV system.
ShowView	A system by which you can easily program the Timer of your DVD-recorder by entering a code of maximum nine digits, which is printed in TV guides. 'ShowView' is a trademark of Gemstar Development Group.
S-video	Sometimes also called S-VHS or Super-VHS. A high-quality video connection standard.
Title	It is the name given to the unit of recording on the disc. A title, typically, represents one recording.
TruSurround	A system for simulating Multi-channel sound reproduction via a two-channel set-up, by SRS Labs, Inc.
TV system	There are various systems for transmitting television signals, for example PAL, PAL-I, PAL-BG, SECAM, SECAM-DK, NTSC, etc. The TV system is country dependant.
VCD	Video Compact Disc
VCR	Video Cassette Recorder
VPS	Video Programming System

Appendix

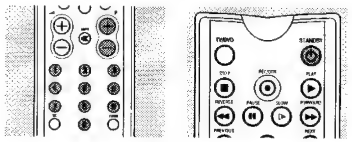
Using your DVD recorder remote control with your TV set

Your DVD recorder remote control can transmit several commands to TV sets of different brands. The following keys will always operate the TV set:



- + increase TV volume
- − decrease TV volume
- mute TV

Some other keys normally operate the DVD recorder, but will operate the TV set when you keep the button on the side of the remote control pressed:

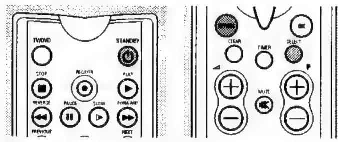


- **P +** next TV programme number
- **P -** previous TV programme number
- **0 - 9** choose TV channel
- ⏻ switch TV to standby

If your TV set does not respond to the remote control, you can re-programme your remote control. Below you will find a list of all available remote control codes for various TV brands. The following procedure re-programmes your remote control:

- Look up the set-up code for your TV set in the code list below.
- Press and hold the **RETURN** and **SELECT** key simultaneously for at least 3 seconds.
- Release both keys.
- Enter, within 30 seconds, the correct three-digit code with the digit keys **0-9**.
- If the selected code does not work with your TV set, or if the brand of your TV set is not in the list, try out the codes one after the other.

Alternative procedure:



- Switch on your television set.
- Press and hold the **RETURN** and **SELECT** key simultaneously for at least 3 seconds.
- Release both keys.
- Point the remote control to your TV set.
- Press and hold the ⏻ **STANDBY** key.
  ➤ Your TV set switches off when the right code is found.
- When your TV set switches off, immediately release the ⏻ **STANDBY** key.
  ➤ Your remote control is now re-programmed.
- This complete procedure may take up to 2 minutes.

Remote control set-up codes for television

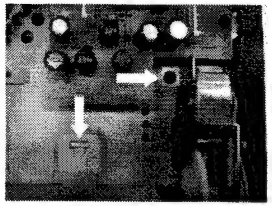
AOC 046, 057
Acura 036
Admiral 120, 490
Adyson 244
Aiko 119
Akai 057
Akura 245, 291
Alaron 206, 243
Alba ... 064, 036, 245, 063, 398
Allorgan 321
America Action 207
Amplivision 244
Amstrad 198, 398, 036, 064
Anam 207, 036
Anitech 036
Arcam 243, 244
Asuka 245
Atlantic 233
Audiosonic 064, 136
Audiovox 119, 207, 478
Autovox 233
BPL 309
BSR 321
BTC 245
Bang & Olufsen 592
Basic Line 036, 245
Baur 064, 037, 581
Baysonic 207
Beaumark 205
Beko 397
Belcor 046
Bell & Howell 181
Beon 064
Binatone 244
Blaupunkt 581
Blue Sky 245
Blue Star 309
Boots 244
Bradford 207
Brandt 136
Britannia 243
Brockwood 046
Broksonic 263, 490
Bush .. 064, 398, 245, 036, 063, 309, 321, 401
CCE 064, 244
CS Electronics 243
CXC 207
Candle 057, 083
Carnivale 057
Carrefour 063
Carver 081
Cascade 036
Cathay 064
Celebrity 027
Centurion 064
Cimline 036
Cineral 478, 119
Citizen 083, 057, 066, 087, 119
Clarivox 064
Clatronic 397
Concerto 083
Condor 347, 397
Contec 036, 063, 207, 243
Craig 207
Crosley 081
Crown 397, 036, 064, 066, 207, 445
Crystal 458
Curtis Mathes ... 087, 057, 066, 074, 078, 081, 083, 120, 172, 181, 193, 478
Cybertron 245
Daewoo ... 119, 046, 401, 478, 036, 064, 066
Dainichi 245
Dansai 064
Dayton 036
Daytron 046
Decca 064, 099
Denon 172
Dixi 036, 064
Dual Tec 244
Dumont 044, 046, 097
Electroband 027
Elin 064
Elite 245, 347
Elta 036
Emerson ... 263, 207, 205, 206, 490, 309, 066, 046, 181
Envision 057
Erres 039, 064
Expert 233
Ferguson 136, 064
Fidelity 243
Finlux .. 064, 132, 097, 099, 206

Firstline 348, 036, 243, 244, 321
Fisher 244, 181, 397
Flint 482
Formenti 347, 064
Frontech 458, 291
Fujitsu 206, 099, 233
Funai .. 321, 198, 206, 207, 291
Futuretech 207
GE 048, 074, 078, 205, 478, 120, 309
GEC 099, 064, 244
GPM 245
Geloso 036
Genexxa 245
Gibralter 044, 046, 057
GoldStar ... 064, 046, 057, 205, 244, 083, 136
Goodmans 064, 099, 206, 398, 063, 244, 401
Gorenje 397
Gradiente 083, 080
Granada 064, 099, 244
Grandin 309
Grundig 097, 581, 064
Grunpy 206, 207
HCM 036, 309
Hallmark 205
Hanseatic 064, 347
Harley Davidson 206
Harman/Kardon 081
Harvard 207
Hinari 036, 063, 064, 245, 206
Hisawa 309, 482
Hitachi 136, 071, 172, 244, 063, 083, 132
Huanyu 243, 401
Hypson 291, 064, 309
ICE 244, 291, 398
ICeS 245
ITS 398
Imperial 445, 397
Indiana 064
Infinity 081
Inno Hit 099
Innova 064
Inteq 044
Interfunk 064
Intervision .. 064, 129, 244, 291
Isukai 245
JBL 081
JCB 027
JVC 080, 063, 398, 680
KEC 207
KTV 207, 244, 057, 066
Kaisui .. 245, 244, 036, 243, 309
Kamp 243
Kapsch 233
Kawasho 243
Kendo 064
Kenwood 057, 046
Kingsley 243
Korpel 064
Koyoda 036
LG 083
LXI 181, 074, 081, 183, 205
Leyco 099, 064, 291, 321
Liesenk & Tter 064
Luma 233
Luxman 083
M Electronic 132, 244, 036, 064, 136, 401
MGA 177, 046, 057, 205
MTC ... 087, 057, 046, 083, 243
Magnadyne 129
Magnafon 129
Magnavox ... 081, 057, 063, 206
Manesth 347, 244, 291
Marantz 064, 081, 057
Mark 064
Matsui . 036, 064, 244, 398, 062, 063, 099, 321
Matsushita 277, 677
Mediator 039, 064
Megatron 172, 205
Memorex .. 205, 036, 083, 177, 181, 277, 490
Midland 044, 066, 074, 078
Minerva 097, 581
Minutz 048
Mitsubishi .. 063, 135, 177, 205, 046, 120
Mivar 243
Motorola 120
Multitech ... 036, 129, 207, 243, 244
NAD 183, 193, 205
NEC ... 057, 063, 046, 083, 482
NEI 064, 458
NTC 119
Neckermann 064, 581
Nesco 206
Netsat 064
Nikkai . 064, 062, 245, 099, 243, 291
Nikko 205, 057, 119
Nobliko 129
Nordmende 136
Onwa 207
Optimus 277, 193, 181, 677
Optonica 120, 192
Orion . 321, 490, 064, 206, 263, 347, 348
Osaki 099, 244, 245, 291
Oso 245
Osume 099
Otto Versand ... 064, 037, 063, 244, 347, 581
Palladium 397, 445
Panama 244, 291
Panasonic 078, 277, 677
Pathe Cinema 347, 243
Pausa 036
Penney 074, 087, 057, 048, 205, 078, 066, 046, 083, 183
Perdio 347
Philco .. 172, 046, 057, 081, 490
Philips .. 064, 039, 081, 401, 581
Phonola 064, 039
Pilot 046, 057, 066
Pioneer 136, 193
Portland 046, 066, 119
Prism 078
Profex 036
Proline 348
Proscan 074
Protech 064, 129, 036, 458, 244, 291, 445
Proton 205
Pulsar 044, 046
Pye 039
Quasar 078, 277, 192, 677
Quelle 064, 097, 037, 581
Questa 063
R-Line 064
RBM 097
RCA ... 074, 046, 078, 117, 120
Radio Shack 192, 207, 057, 205, 066, 181, 046, 074, 083
Radiola 064, 039
Rank Arena 063
Realistic 192, 207, 181, 057, 066, 205, 046, 083
Revox 064
Rex 233, 291
Rhapsody 243
Roadstar ... 036, 291, 245, 445
Runco 044, 057
SBR 039, 064
SEG 244, 063, 291
SEI 129, 037, 321
SKY 064
SSS 046, 207
Saba 136
Saisho 036, 291, 458
Sambers 129
Sampo 057, 066
Samsung ... 064, 046, 205, 244, 291, 397, 036, 057, 066, 083, 087, 117
Samsux 066
Sandra 243
Sansei 478
Sansui 490
Sanyo 181, 063, 099
Schneider 064, 245, 398
Scimitsu 046
Scotch 205
Scott .. 263, 046, 205, 206, 207
Sears .. 181, 083, 183, 074, 081, 198, 205, 206
Seleco 233
Semivox 207
Semp 183
Sentra 062
Sharp 120, 192, 063, 066
Shogun 046
Shorai 321
Siarem 129
Siemens 581, 064
Silver 063
Sinudyne 129, 037, 321
Sonoko 036, 064
Sontec 064
Sony 037, 063, 027
Soundesign 205, 206, 207
Soundwave 064, 445
Squareview 198
Standard 244, 245, 036
Starlite 207
Stern 233
Sunkai 321, 348
Supra 083
Supreme 027
Susumu 245
Sylvania 081, 057
Symphonic 198
Sysline 064
TMK 083, 205
Tandy 245, 099, 244, 120
Tashiko 063, 244
Tatung 099, 244, 064
Tec 244
Technema 347
Technics 078, 277, 677
Technol Ace 206
Techwood 078, 083
Teknika 081, 206, 207, 046, 066, 119, 083, 087, 177
Telefunken 136, 083
Telemeister 347
Teletech 036
Teleton 233, 063, 244
Tensai 245, 321, 347
Texet 243, 245
Thomson 136
Thorn 064, 062, 099
Tomashi 309
Toshiba 062, 183, 063, 097, 087, 181
Totevision 066
Uher 233, 347
Ultravox 129
Universum .. 132, 064, 291, 397
Vector Research 057
Vestel 064
Victor 080
Videotechnic 244
Vidikron 081
Vidtech 046, 063, 205
Vision 347
Waltham 244
Wards 081, 192, 205, 046, 048, 057, 083, 206
Watson 347, 064
Watt Radio 129
Wega 063
White Westinghouse 347, 064, 243, 490
Yamaha 046, 057
Yoko 244, 064, 291, 458
Zanussi 233
Zenith 044, 119, 490

4. Mechanical Instructions

4.1 Dismantling Instrutions

DISMANTLING INSTRUCTIONS
See exploded view for item numbers



mounting ↑ ↓ demounting

Cover 151
⇒ Remove 9 screws
171→174 at both sides
175→179 at the rearside
⇒ Lift the cover at the rearside to remove

Front assy
⇒ open the tray and remove the tray front 65
⇒ remove 4 screws 75→ 78 (front assy → frame 181)
⇒ remove screw 72 (flap motor assy →frame 181)
⇒ remove the feet (251→ 254) and the bottomplate (231)
⇒ unlock the front from the frame by releasing successively 6 snaps (1 on the left, 2 in the middle, 1 on the right and 2 in the bottom of the frame. The snaps in the bottom can be released inside the set via the holes in the bottom.

FRONT DV Board 1006
⇒ Remove screw 17 (board → front)
⇒ demount the board

Display board 1004
⇒ Remove 6 screws 33→38 (board → front)
⇒ demount the board

IR/STBY Board 1004
⇒ remove screw 30 (board → front)
⇒ demount the board

FRONT AV Board1004
⇒ remove screws 31+32 (board → front)
⇒ demount the board

Analog board 1003
⇒ remove the connections
⇒ remove 1 screw(206) (board →frame)
⇒ remove screws (cinches → backplate)
⇒ release the snaps of 4 spacers (board →frame)
⇒ demount the board

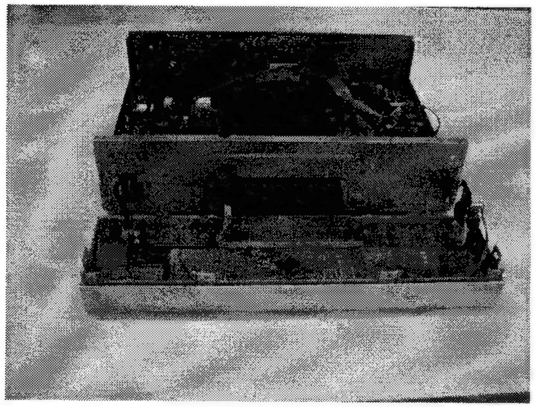
Progressive Scan board 1007 (Only for DVDR1000/171)
⇒ release snaps of 3 spacers
⇒ demount the board

DVIO board 1005
⇒ Remove 2 screws 217 and 218 (DVIO board→ frame 181)
⇒ Release the snaps of 2 spacers (DVIO board → Digital board)
⇒ demount carefully the board. (board to board connection to the Digital board)

Digital board 1001
⇒ Remove the connections
⇒ Remove 4 screws 207 → 210 (Digital board → frame 181)
⇒ demount the board.

DVDR LOADER 81
⇒ Remove the connections
⇒ Remove 4 screws (192→194) (air filter 191 → loader 81)
⇒ Remove screw 196 (air filter inlet 198→ frame 181)
⇒ Remove air filter assy
⇒ Open the tray and remove the tray front 65
⇒ Remove 4 screws 200 → 203 (loader 81→frame 181)
⇒ Demount the DVDR loader

Switched Operating Power supply 1002
⇒ Remove the connections
⇒ Remove screws 204 → 205 (board → frame)
⇒ Remove screw 268 (mains inlet →backplate)
⇒ Release the snaps of 2 spacers 183 and 184 (board →frame)
⇒ Demount the board



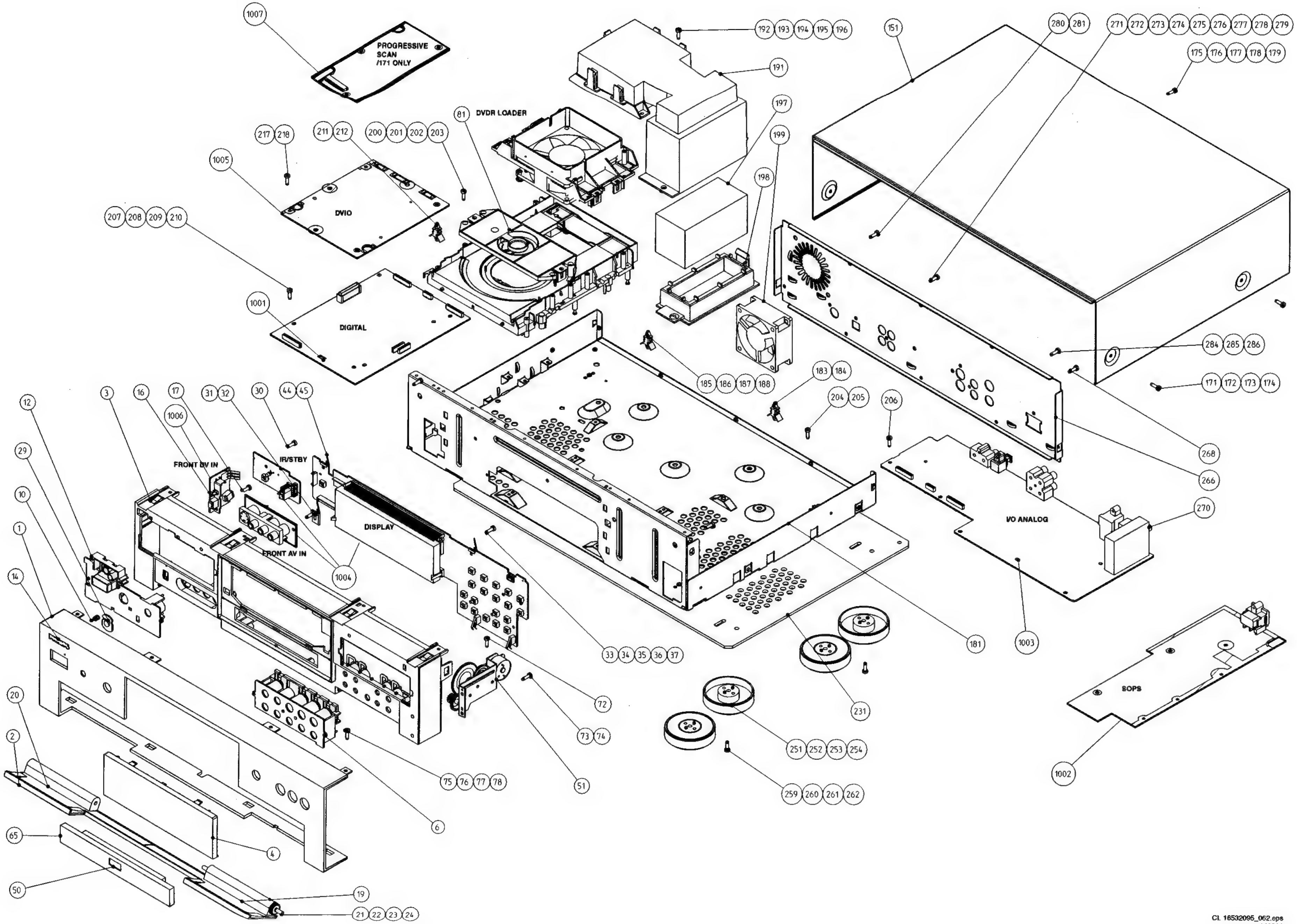
Manually removal of tray front 65

In case the loader is defective and cannot be opened electrically, you can open the tray after demounting the loader as follows:

⇒ Remove the connections to the loader
⇒ Remove 4 screws (192→194) (air filter 191 → loader 81)
⇒ Remove screw 196 (air filter inlet 198→ frame 181)
⇒ Remove air filter assy
⇒ Remove 4 screws 200 → 203 (loader 81→frame 181)
⇒ Lift the loader a the rear side. The tray front jumps off from the loader.
⇒ demount the loader
⇒ Push the white pin of the slider at the bottom side of the loader in the direction indicated by the arrow. Open the unlocked tray.

CL 16532095_061.eps
140801

4.2 Exploded View



CL 16532095_062.eps
140801

4.3 Service Hints

4.3.1 DVDR Module VAE8010/01

This module, item 81 in exploded view, must be exchanged completely in case of failure. A new unit can be ordered with codenumber 9305 025 81001.

4.3.2 Service Positions

Front

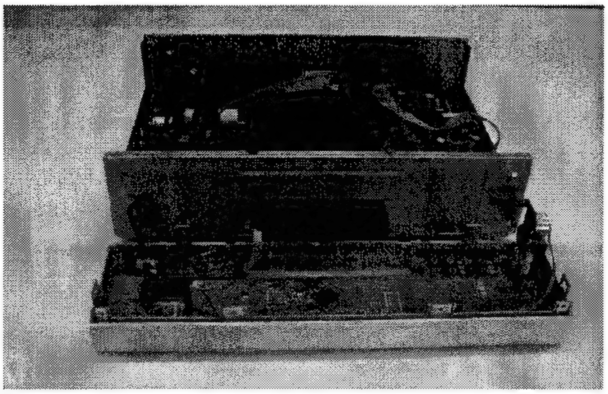


Figure 4-1

DVIO Board
To put the DVIO board in a service position, an extender board must be used. This extender board can be ordered with codenumber 3104 128 07770.

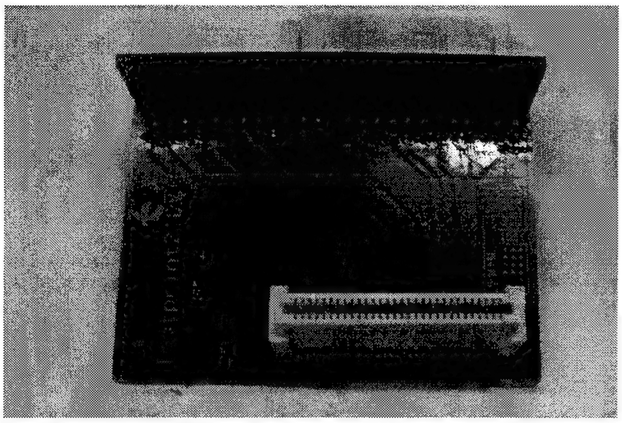


Figure 4-2

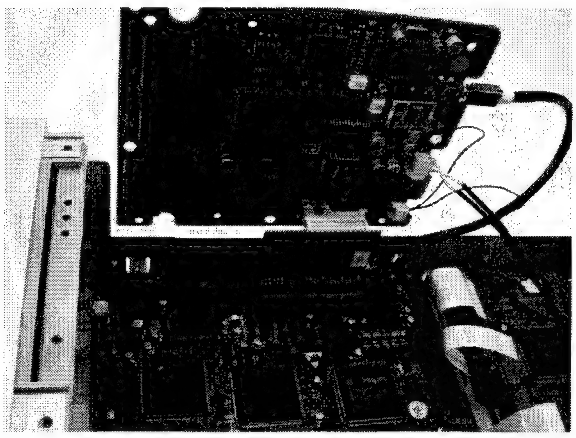


Figure 4-3

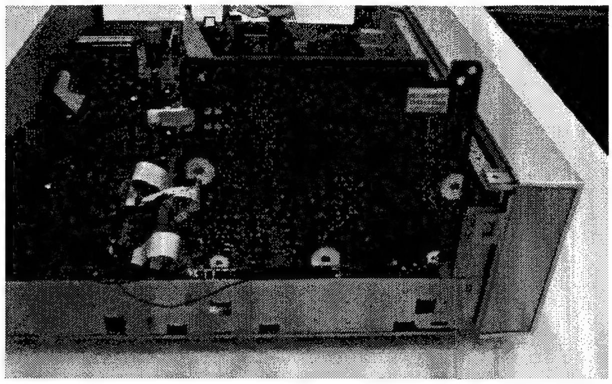


Figure 4-4

Digital Board
After demounting of DVIO board, the top side of the digital board is in reach. To reach the bottom side of the digital board, the DVDR module must be demounted together with the digital board. Connected to each other, the assembly can be set in a service position. In this position, the bottom side of the digital board and the servo board are in reach to be serviced.

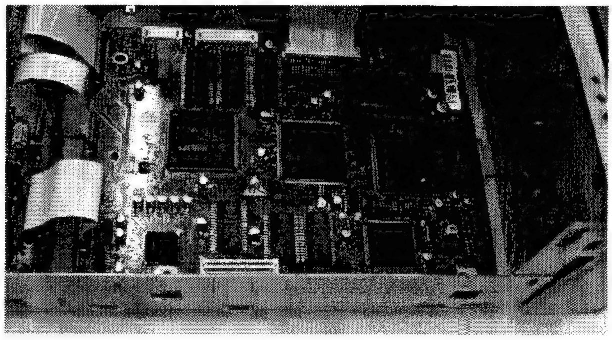


Figure 4-5

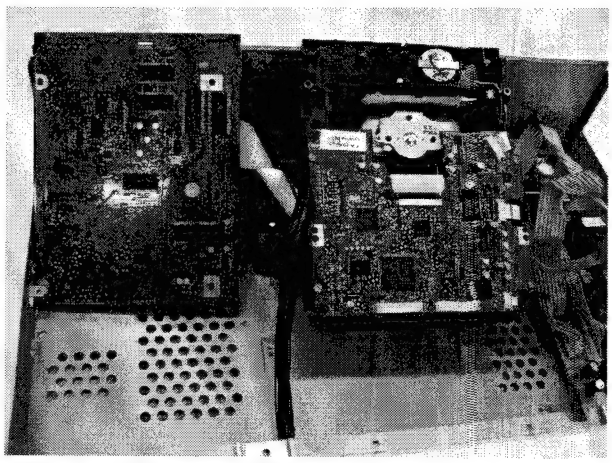


Figure 4-6

Analog Board
To put the analog board in service position, demount the assembly of analog board and backplate as follows:

1. Remove 3 screws from the backplate to the frame
2. Remove the screw from the backplate to the mains inlet of the power supply
3. Remove the screw of the analog board to the frame

4. Release the snaps of the 4 spacers of the analog board to the frame.

Turn the assembly of the backplate and the analog board against the loader.

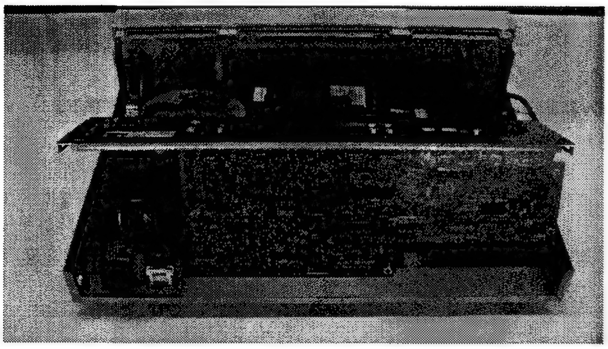


Figure 4-7

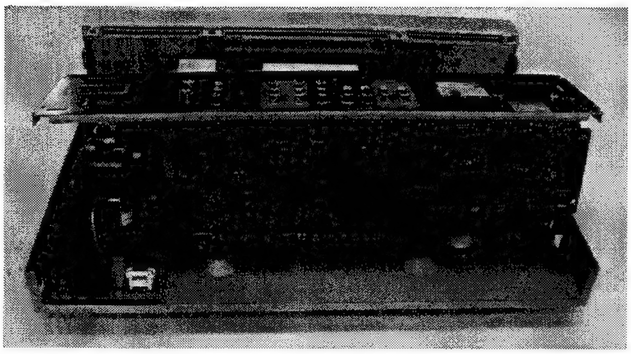


Figure 4-8

5. Diagnostic Software and Faultfinding Trees

Due to the complexity of the DVD recorder, the time to find a defect in the recorder can become long. To reduce this time, the recorder has been equipped with Diagnostic and Service software (DS). The DS offers functionality to diagnose the DVDR hardware and tests the following:

- Interconnections between components
- Accessibility of components
- Functionality of the audio and video paths

This functionality can be accessed via several interfaces:

1. End user/Dealer script interface
2. Player script interface
3. Menu and command interface

5.1 End User/Dealer Script Interface

5.1.1 Description

The End user/Dealer script interface gives a diagnosis on a stand alone DVD recorder; no other equipment is needed. During this mode, a number of hardware tests (nuclei) are automatically executed to check if the recorder is faulty. The diagnosis is simply a "fail" or "pass" message. If the message "FAIL" appears on the display, there is apparently a failure in the recorder. If the message "PASS" appears, the nuclei in this mode have been executed successfully. There can be still a failure in the recorder because the nuclei in this mode don't cover the complete functionality of the recorder.

5.1.2 Contents

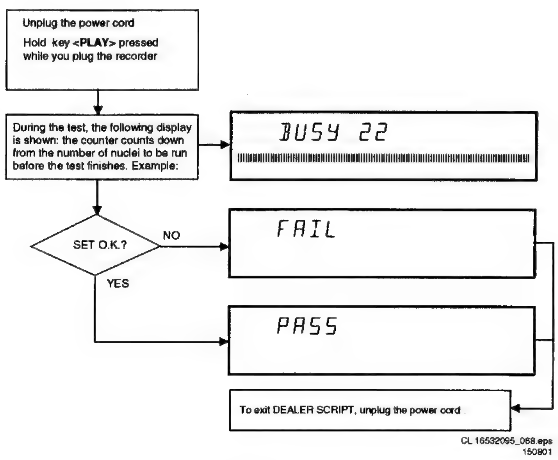


Figure 5-1

The End use/Dealer script executes all diagnostic nuclei that do not need any user interaction and are meaningful on a standalone DVD recorder. The nuclei called in the End user/ Dealer script are the following:

22	HostdSdramWrR	check of all memory locations of the 4MB SDRAMS
21	HostdDramWrR	check of all the DRAMS
20	HostdI2cNvram	check of the data line and the clock line of the I2C bus between the host decoder and NVRAM
19	SAA711XI2c	checks the interface between the host I2C controller and the Video Input Processor SAA7118
18	VideoEncI2c	checks the interface between the host I2C controller and the Video Encoder SAA6750
17	AudioEncI2c	checks the I2C connection between the host decoder and the audio encoder
16	AudioEncAccess	this nucleus tests the HIO8 interface lines between the host decoder and the audio encoder
15	AudioEncS-ramAccess	check of the access of the SRAM by the audio encoder (address and data lines)
14	AudioEncS-ramWrR	tests the SRAM connected to the audio encoder
13	AudioEncInter-rupt	tests the interrupt line between the host decoder and the audio encoder
12	VsmAccess	checks the data and address bus and the interrupt register of the VSM
11	VsmInterrupt	checks both interrupt lines between the VSM and the host decoder
10	VsmSdramWrR	tests the entire SDRAM of the VSM
9	Clock11_289MHz	switches the A_CLK of the micro clock to 11.2896 MHz
8	Clock12_288MHz	switches the A_CLK of the micro clock to 12.288 MHz
7	BeS2Bengine	checks the S2B interface with the Basic Engine by sending an echo command
6	DisplayEcho	checks the interface between the host processor and the slave processor on the display board
5	AnalogueEcho	checks the interface between the host processor and the microprocessor on the analogue board
4	AnalogueNvram	checks the NVRAM on the analogue board
3	AnalogueTuner	checks whether the tuner on the analogue board is accessible
2	LoopAudioUser-Dealer	tests the components on the audio signal path Host decoder Analogue board Audio encoder VSM
1	LoopVideoUser-Dealer	tests the components on the video signal path VIP VSM Host decoder

5.2 Player Script Interface

5.2.1 Description

The Player script will give the opportunity to perform a test that will determine which of the DVD recorder's modules are faulty, to read the error log and to perform an endurance loop test. To successfully perform the tests, the DVD recorder must be connected to a TV set.
To be able to check results of certain nuclei, the player script expects some interaction of the user (i.e. to approve a test picture or a test sound). Some nuclei (e.g. nuclei that test functionality of the DVDR module) require that a DVD+RW disc is inserted.
Only tests within the scope of the diagnostic software will be executed hence only faults within this scope can be detected.

5.2.2 Structure of the Player Script

The player script consists of a set of nuclei testing the hardware modules in the DVD recorder: the Display PWB, the Digital PWB, the Analogue In/Out PWB and the DVDR module.
Nuclei run by the player test need some user interaction; in the next table this interaction is described. The player test is done in two phases:

- Interactive tests: this part of the player test depends strongly on user interaction and input to determine nucleus results and to progress through the full test. Reading the error log information can be useful to determine any errors that occurred recently during normal operation of the DVD player.
- The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely.

STEP	DESCRIPTION	NUCLEUS
1	Press **OPEN/CLOSE** and **STOP** at the same time and **POWER ON** the recorder to start the playerscript	2
2	The local display shows **FPSEGMENTS**. Press **PLAY** to start the test. First the *starburst pattern* is lit, then the *horizontal segments* are lit, followed by the *vertical segments* and the last test is *light all segments* test. After each of the 4 tests the user has to confirm that the correct pattern was lit. Press **PLAY** to confirm that the correct pattern was lit (four times if the FPSEGMENTS test was successful). Press **RECORD** to indicate that the correct pattern was not successfully lit. Press **STOP** to skip this nucleus.	502
3	The local display shows **FPLABELS**. Press **PLAY** to start the test. Press **PLAY** to confirm that all labels are lit. Press **RECORD** to indicate that not all labels are lit. Press **STOP** to skip this nucleus.	503
4	The local display shows **FPLIGHT ALL**. Press **PLAY** to start the test. Press **PLAY** to confirm that everything was lit. Press **RECORD** to indicate that not all patterns are lit. Press **STOP** to skip this nucleus.	520
5	The local display shows **FPLED**. Press **PLAY** to start the test. Press **PLAY** to confirm that the led is lit. Press **RECORD** to indicate that the led is not lit. Press **STOP** to skip this nucleus.	504
6	The local display shows **FPFLAP OPEN**. Press **PLAY** to start the test. Press **PLAY** to confirm that the flap has opened. Press **RECORD** to indicate that the flap did not open. Press **STOP** to skip this nucleus.	522
7	The local display shows **FPKEYBOARD**. Press **PLAY** to start the test. Attention all keys have to be pressed to get a positive result! Press **PLAY** for more than one second to confirm that all the keys were pressed and shown on the local display. If not all the keys were pressed, a FAIL message will appear on the local display. Press **RECORD** for more than one second to indicate that not all keys were pressed and shown on the local display. Press **STOP** for more than one second to skip this nucleus.	505
8	The local display shows **FPREMOTE CONTROL**. Press **PLAY** to start the test. Press **PLAY** to confirm that a key on the remote control was pressed and shown on the local display. Only one key has to be pressed to get a successful result. Press **RECORD** to indicate that the key on the remote control was pressed but not shown on the local display. Press **STOP** to skip this nucleus.	506
9	The local display shows **FPDIMMER**. Press **PLAY** to start the test. Press **PLAY** to confirm that the text on the local display was dimmed. Press **RECORD** to indicate that the text on the local display was not dimmed. Press **STOP** to skip this nucleus.	518
10	The local display shows **FPBEEPER**. Press **PLAY** to start the test. Press **PLAY** to confirm that the beeper on the front panel sounded. Press **RECORD** to indicate that the beeper on the front panel did not sound. Press **STOP** to skip this nucleus.	514
11	The local display shows **FPFLAP CLOSE**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	523
12	The local display shows **ROUTE VIDEO**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	712
13	The local display shows **ROUTE AUDIO**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	713
14	The local display shows **COLOUR-BAR ON**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	120
15	The local display shows **PINK NOISE ON**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	115
16	The local display shows **PINK NOISE OFF**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	116
17	The local display shows **SINE ON**. Press **PLAY** to start the test. Press **STOP** to stop the sine. Press **STOP** to skip this nucleus.	117
18	The local display shows **COLOUR-BAR OFF**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	121
19	The local display shows **BERESET**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	603
20	The local display shows **BETRAY OPEN**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	616
21	The local display shows **BETRAY CLOSE**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	615
22	The local display shows **BEWRITE READ**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	617
23	The local display shows **BETRAY OPEN**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	616
24	The local display shows **BETRAY CLOSE**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	615
25	The local display shows **READ ERRORLOG**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus. If the player test succeeded, the **user/dealer script** will start in an endless loop. If the player test failed, the local display will display **FAIL** and the **error code**	633

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Remark

In case of failure, the display shows " FAIL 00000 ". The description of the shown error code can be retrieved in the survey of Nuclei Error Codes (paragraph 5.4). Once an error occurs, it is not possible to continue the player script. Unplug the set and restart the player script. By pressing the STOP key, it is possible to jump over the failure and to continue the player script.

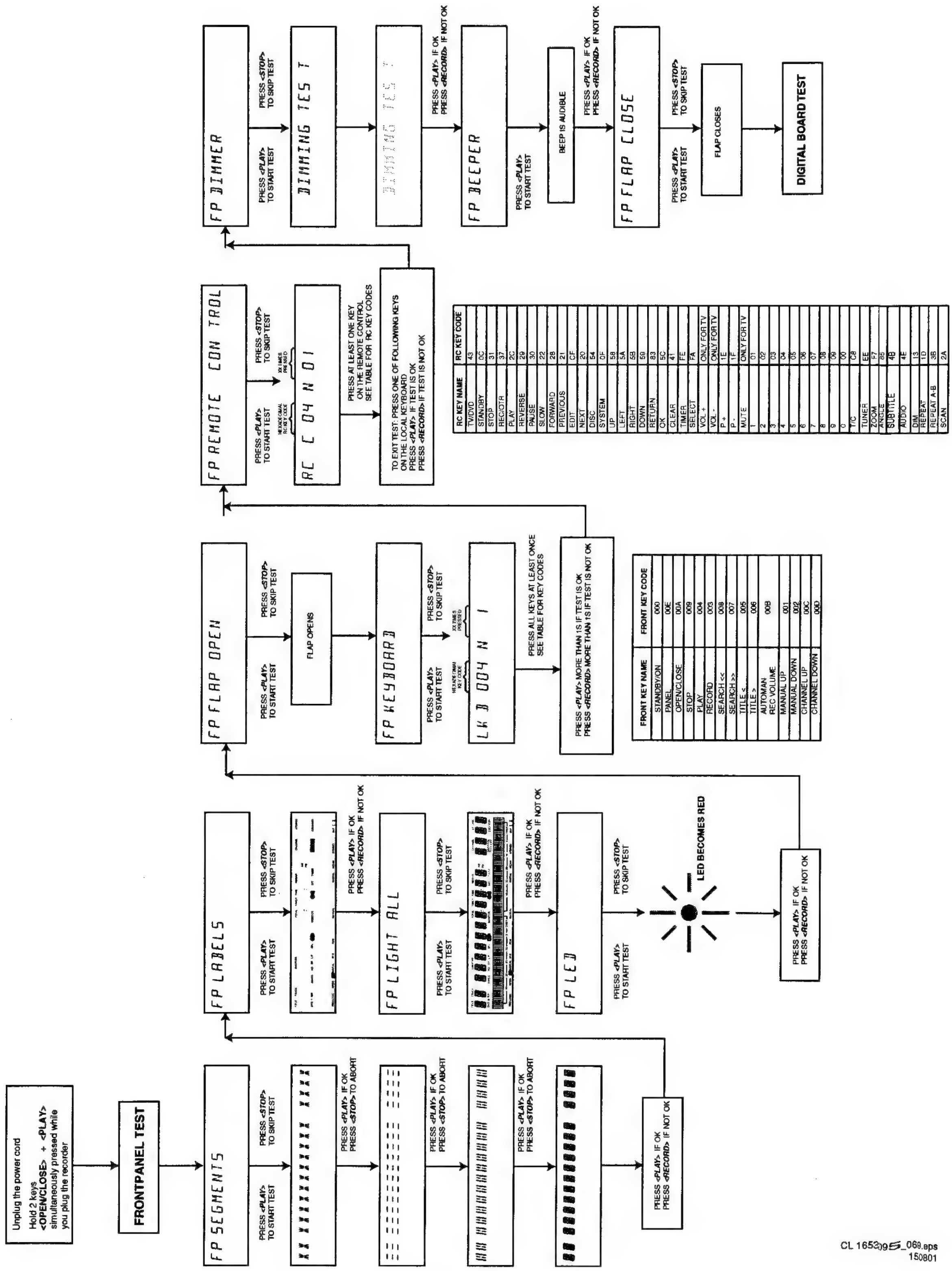

Figure 5-2

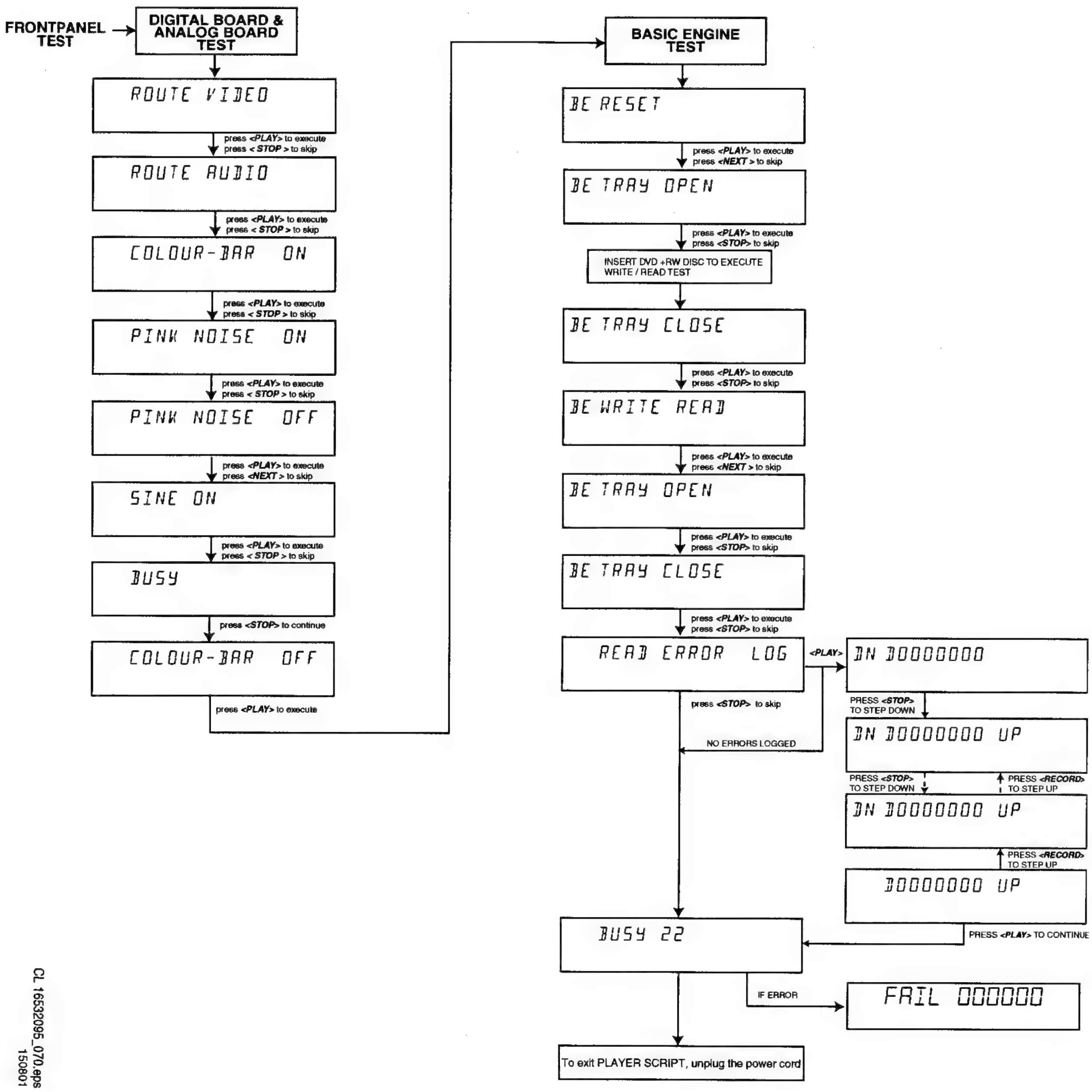

Figure 5-3

5.2.3 ErrorLog

Explanation:
The application errors will be logged in the NVRAM. The maximum number of error bytes that will be visible is 19. The last reported error is shown as DN D0000000, the oldest visible error as D0000000 UP and the errors in between as DN D0000000 UP. DN stands for DOWN, UP stands for UPWARDS. The shown error codes are identical to the Nuclei Error Codes (paragraph 5.4).

5.2.4 Trade Mode

TRADE MODE
When the recorder is in Trade Mode, the recorder cannot be controlled by means of the front key buttons, but only by means of the remote control.

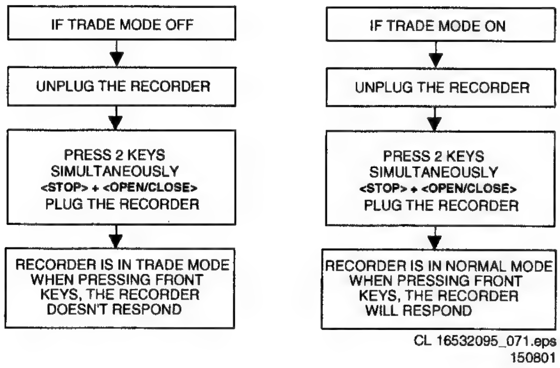

Figure 5-4

5.3 Menu and Command Mode Interface

5.3.1 Nuclei Numeration

Each nucleus has a unique number of four digits. This number is the input of the command mode.

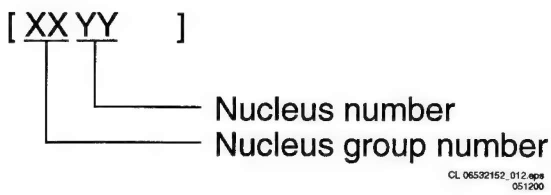

Figure 5-5

The following groups are defined:

Group number	Group name
0	Basic / Scripts
1	Host decoder (Sti5505 and memory)
2	Audio / video encoder (DVDR only)
3	VSM (DVDR only)
4	NVRAM
5	Front Panel
6	Basic Engine
7	Analogue board (DVDR only)
8	DVIO (DVDR only)
9	Loop nuclei (DVDR only)
10	Library sub nuclei (I2C nuclei)
11	User interface
12	Furore (SACD only)
13	DAC (SACD only)
14	Miscellaneous

5.3.2 Error Handling

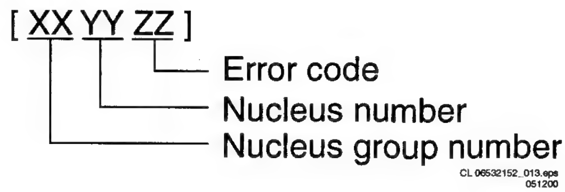

Figure 5-6

The nucleus group numbers and nucleus numbers are the same as above.

5.3.3 Command Mode Interface

Set-Up Physical Interface Components
Hardware required:
- Service PC
- one free COM port on the Service PC
- special cable to connect DVD recorder to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD recorder. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin). Code number of PC interface cable: 3122 785 90017

Activation
Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):

```
DVD Video Recorder Diagnostic Software version 48
Basic SDRAM Data bus test passed
Basic SDRAM Address bus test passed
Basic SDRAM Device test passed

(M) enu, (C) ommand or (S) 2B-interface?      [M] : @ C ↵
DD:>
```

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Figure 5-7

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing C has made a choice for Command Interface, the prompt ("DD>") will appear. The diagnostic software is now ready to receive commands. The commands that can be given are the numbers of the nuclei.

Command Overview
We provide an overview of the nuclei and their numbers. This overview is preliminary and subject to modifications.

Host Decoder [01]

[xx yy] Number	Nuclei
100	Checksum Flash
101	Flash Write Access 1
102	Flash Write Access 2
103	Flash Write Read
104	SdRam Write Read
105	SdRam Write Read Fast
106	Dram Write Read
107	Dram Write Read Fast
108	Hardware Version
109	Mute On
110	Mute Off
115	Pink Noise On
116	Pink Noise Off
117	Sine On
118	Sine Burst 1kHz
119	Sine Burst 12kHz
120	Colour-bar On
121	Colour-bar Off
122	NvramWrR
123	NvramI2c
130	Boot Version
131	Application Version
132	Diagnostics Version
133	Download Version
134	Write / read I2C message to / from digital board

Audio Video Encoder [02]

[xx yy] Number	Nuclei
200	Video Encoder I2C
202	SAA711x I2C
203	Audio Encoder SRAM Access
204	Audio Encoder Access
205	Audio Encoder SRAM Write Read
206	Audio Encoder Interrupts
207	Audio Encoder I2C
208	SAA7118 select input

VSM [03]

[xx yy] Number	Nuclei
300	Register Access
301	SDRAM Access
302	SDRAM Write Read
303	Interrupt lines
304	VSM Interconnection
305	UART

NVRAM [04]

[xx yy] Number	Nuclei
400	Reset
401	Read
402	Modify
403	UniqueNr Read
404	Read Error Log
407	Reset Error Log
409	Line2 Region-Code Reset
410	UniqueNr Store

Front Panel [05]

[xx yy] Number	Nuclei
500	Echo
501	Version
502	Segment
503	Label
504	Led
505	Keyboard
506	Remote-Control
507	Segment Starburst
508	Segment Vertical
509	Segment Horizontal
514	Beeper
515	Discbar
516	Discbar Dots
517	Vu / Grid
518	Dimmer
519	Blinking
520	Light All Segments
522	Flap Open
523	Flap Close

Basic Engine [06]

[xx yy] Number	Nuclei
600	S2B Pass
601	S2B Echo
602	Version
603	Reset
604	Focus On
605	Focus Off
606	Disc Motor On
607	Disc Motor Off
608	Radial On
609	Radial Off
615	Tray In
616	Tray Out
617	Write Read
618	Write Read Endless Loop
619	Selftest
620	BE Test
621	Laser Test
622	Spindle (Disc) Motor Test
623	Focus Test
624	Sledge Motor Test
625	Sledge Motor Slow
626	Tilt
627	EEPROM Read
628	EEPROM Write
629	Optimise Jitter
630	Radial ATLS Calibration
631	Get Statistics Information
632	Reset Statistics Information
633	BE Read Error Log
634	BE Reset Error Log
638	Get Self Test Result
639	Radial Initialisation

Analogue Board [07]

[xx yy] Number	Nuclei
700	Echo
703	Boot Version
704	Hardware Version
705	Clock Adjust
706	Tuner
707	Frequency Download
708	Data Slicer
709	Sound Processor
710	AV Selector
711	Nvram
712	Route Video
713	Route Audio
714	Validate CVBS
715	Set Slash Version
716	Application Version
717	Diagnostics Version
718	Download Version
719	Initiate Output Of Clock Reference
720	Adjust Clock reference
721	Adjust Bargraph Level
723	Revirginize Recorder
724	Flash Checksum
726	Tuner frequency selection

[xx yy] Number	Nuclei
727	Set virgin bit
728	Clear Virgin Bit
729	Write / read I2C message to / from analogue board
730	Store external presets

DVIO [08]

[xx yy] Number	Nuclei
800	Check DVIO board presence
801	Reset DVIO
802	DVIO Access
803	Get DVIO error codes
804	Get DVIO module Ids

Loop Nuclei [09]

[xx yy] Number	Nuclei
900	Digital Audio Loop
901	Audio User Dealer Loop
902	Digital Video Loop
903	Digital Video VBI Loop
904	System Video Loop
905	System Video VBI Loop
906	Video User Dealer Loop
907	Video VBI User Dealer Loop
908	System Audio Loop SCART
909	System Audio Loop CINCH
910	Digital DVIO Video Loop

Miscellaneous [14]

[xx yy] Number	Nuclei
1400	Clock 11.289 MHz
1401	Clock 12.288 MHz
1412	Progressive Scan I2C
1413	Progressive Scan test image on
1414	Progressive Scan test image off

Scripts [00]

[xx yy] Number	Nuclei
1	UserDealer Script
2	Player Script

5.3.4 Menu Mode Interface

Activation

Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):

```
DVD Video Recorer Diagnostic Software version 48
Basic SDRAM Data bus test passed
Basic SDRAM Address bus test passed
Basic SDRAM Device test passed

(M) enu, (C) ommand or (S) 2B-interface?      [M] : @ M

Main Menu

1.    Digital Board          ->
2.    Analogue Board         ->
3.    Front Panel            ->
4.    Basic Engine           ->
5.    DVIO                   ->
6.    Progressive Scan Board ->
7.    Loop tests             ->
8.    Log                    ->
9.    Scripts                ->

Select>
```

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Figure 5-8

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing M has made a choice for Menu Interface, the Main Menu will appear.

Menu Structure

The following menu structure is given after starting up the DVD recorder in menu mode. The symbol → indicates that the current menu choice will invoke the display of a submenu.

Main Menu
1. Digital Board →
2. Analogue Board →
3. Front Panel →
4. Basic Engine →
5. DVIO →
6. Progressive Scan Board →
7. Loop Tests →
8. Log →
9. Scripts →

Digital Board Menu
1. Host Decoder →
2. VSM →
3. AVENC →
4. NVRAM →

Host Decoder Menu
1. Flash Checksum
2. Flash1 Write Access
3. Flash2 Write Access
4. Flash Write/Read
5. Host SDRAM Write/Read
6. Host SDRAM Fast Write/Read
7. Host DRAM Write/Read
8. Host DRAM Fast Write/Read
9. I2C NVRAM
10. NVRAM Write/Read
11. Engine S2B Echo
12. Versions →
13. Audio Mute →
14. Colourbar →
15. Pink Noise →
16. Sine Generate →

Digital Board Versions Menu
1. Hardware Version
2. Bootcode version
3. Applications Version
4. Diagnostics Version
5. Download Version

Audio Mute Menu
1. Audio Mute On
2. Audio Mute Off

Colourbar Menu
1. Colourbar On
2. Colourbar Off

Pink Noise Menu
1. Pink Noise On
2. Pink Noise Off

Sine Generate Menu
1. Sine On
2. Sine Burst 1kHz
3. Sine Burst 12kHz

VSM Menu
1. Register Access
2. SDRAM Access
3. VSM SDRAM Write/Read
4. Interrupt Lines
5. VSM Interconnection
6. UART

AVENC Menu
1. Video Encoder →
2. Audio Encoder →
3. Video Input Processors →

Video Encoder Menu
1. I2C Access

Audio Encoder Menu
1. I2C Access
2. Interrupt Line
3. Encoder Register Access
4. SRAM Write/Read
5. SRAM Access

Video Input Processors Menu
1. SAA711X I2C Access

NVRAM Menu
1. Read Error Log
2. Reset Error Log
3. Read DVIO Unique ID

Analogue Board Menu
1. Echo
2. Show Guide Channels
3. Video Routing
4. Audio Routing
5. Flash Checksum
6. Versions →
7. Components →
8. Re-virginize Recorder →

Analogue Board Versions Menu
1. Hardware Version
2. Bootcode version
3. Application version
4. Diagnostics version
5. Download version

Analogue Components Menu
1. Tuner
2. Data Slicer
3. Sound Processor
4. AV Selector

5. NVRAM

Analogue Board Re-virginize Menu
1. Re-virginize Recorder
2. Set Virgin-bit
3. Clear Virgin-bit
4. Store external presets

Front Panel Menu
1. Echo
2. Version
3. Flap Control →
4. Segment Test →
5. Light Labels
6. Led test
7. Keyboard test
8. Remote Control
9. Beep
10. Disc Bar
11. Disc Bar Dots
12. Vu Grid
13. Dimmer
14. Blink
15. Light All Segments

Flap Control Menu
1. Open Flap
2. Close Flap

Segment Test Menu
1. Starburst
2. Light Horizontal Segments
3. Light Vertical Segments
4. Light All Segments

Basic Engine Menu
1. Reset
2. S2B Pass
3. S2B Echo
4. Version
5. Self Test
6. Get Self Test Result
7. Basic Engine Test
8. Laser Test
9. Focus Test
10. Tilt Test
11. Optimise Jitter
12. Statistics Info
13. Log →
14. Spindle Motor →
15. Radial →
16. Sledge →
17. Tray →

Basic Engine Error Log
1. Read Error Log
2. Reset Error Log

Basic Engine Spindle Motor Menu
1. Spindle Motor On
2. Spindle Motor Off
3. Spindle Motor Test

Basic Engine Radial Menu
1. Radial On
2. Radial Off
3. Radial Initialisation
4. Radial ATLS Calibration

Basic Engine Sledge Menu
1. Sledge test
2. Sledge test slow

Basic Engine Tray Menu
1. Tray In
2. Tray Out

DVIO Menu
1. Check Presence
2. Reset
3. Access
4. Error Codes
5. Module Identifiers

Progressive Scan Board Menu
1. I2C Access
2. Test Image On
3. Test Image Off

Loop Tests Menu
1. Digital Board Loops →
2. User/Dealer Loops →
3. System Loops →
4. Basic Engine Loops →

Digital Board Loops Menu
1. Digital Audio Loop
2. Digital Video Loop
3. Digital Video Loop VBI

User/Dealer Loops Menu
1. User/Dealer Audio Loop
2. User/Dealer Video Loop
3. User/Dealer Video Loop VBI

System Loops Menu
1. System Video Loop
2. System Video Loop VBI
3. System Audio Loop SCART
4. System Audio Loop SCART

Basic Engine Loops Menu
1. Basic Engine write read
2. Basic Engine write read endless loop

Log Menu
1. Read Error Log
2. Reset Error Log

Script Menu
1. User/Dealer Script
2. Player Script

5.4 Nuclei Error Codes

In the following table the error codes will be described.

Error Nr	Error String
10000	"Checksum is OK"
10001	"segment name Checksum doesn't match" or "segment name segment not found"
10100	""
10101	"FLASH 1 Write access test failed"
10200	""
10201	"FLASH 2 Write access test failed"
10300	""
10301	"FLASH write test failed"
10302	"FLASH write command failed"
10303	"FLASH write test done max. number of times"
10400	""
10401	"HostDec SDRAM Memory data bus test goes wrong."

Error Nr	Error String
10402	" HostDec SDRAM Memory address bus test goes wrong."
10403	" HostDec SDRAM Physical memory device test goes wrong."
10500	""
10501	" HostDec SDRAM Memory data bus test goes wrong."
10502	" HostDec SDRAM Memory address bus test goes wrong."
10503	" HostDec SDRAM Physical memory device test goes wrong."
10600	""
10601	"HostDec DRAM Memory data bus test goes wrong."
10602	"HostDec DRAM Memory address bus test goes wrong."
10603	"HostDec DRAM Physical memory device test goes wrong."
10700	""
10701	"HostDec DRAM Memory data bus test goes wrong."
10702	"HostDec DRAM Memory address bus test goes wrong."
10703	"HostDec DRAM Physical memory device test goes wrong."
10800	"Host Decoder version(cut) number: version number" "Digital hardware version"
10801	"Can not find version in FLASH."
10900	""
10901	"Error muting audio"
11000	""
11001	"Error demuting audio"
11500	""
11501	"Init of I2C failed"
11502	"The selection of the clock source failed"
11504	"The demute of the audio failed"
11600	""
11601	"Init of I2C failed"
11602	"The mute of the audio failed"
11700	""
11701	"Init of I2C failed"
11702	"The muting of the audio failed"
11703	"The demute of the audio failed"
11704	"The selection of the clock source failed"
11707	"Setup of Front panel failed"
11708	"Sine on Front panel keyboard failed"
11800	""
11801	"Init of I2C failed"
11802	"The muting of the audio failed"
11803	"The demute of the audio failed"
11804	"The selection of the clock source failed"
11805	"Error cannot start VSM audio in port"
11900	""
11901	"Init of I2C failed"
11902	"The muting of the audio failed"
11903	"The demute of the audio failed"
11904	"The selection of the clock source failed"
11905	"Error cannot start VSM audio in port"
12000	""
12100	""
12200	""
12201	"I2C bus busy before start"
12202	"NVRAM access time-out"

Error Nr	Error String
12203	"No NVRAM acknowledge"
12204	"NVRAM time-out"
12205	"NVRAM Write/Read back failed"
12300	""
12301	"I2C bus busy before start"
12302	"NVRAM read access time-out"
12303	"No NVRAM read acknowledge"
12304	"NVRAM read failed"
13000	"Bootcode application version : bootversion"
13001	"Can not find version in FLASH."
13100	"Recorder application version : recorderversion"
13101	"Can not find version in FLASH."
13200	"Diagnostics application version : diagversion"
13201	"Can not find version in FLASH."
13300	"Download application version : downloadversion"
13301	"Can not find version in FLASH."
20000	""
20001	"I2C bus busy before start"
20002	"Video Encoder access time-out"
20003	"No acknowledge from Video Encoder"
20004	"No data send/received to or from Video Encoder"
20005	"SAA711x VIP can not be initialised"
20200	""
20201	"I2C bus busy before start"
20202	"SAA711X VIP access time-out"
20203	"No acknowledge from SAA711X VIP"
20204	"No data received from SAA711X VIP"
20300	""
20301	"Error audio encoder SRAM access cannot initialise I2C"
20302	"Error audio encoder SRAM access cannot reset DSP through I2C"
20303	"Error audio encoder SRAM access cannot download boot"
20304	"Error audio encoder cannot download test code"
20305	"Error audio encoder cannot obtain result of test"
20306	"Error audio encoder SRAM access stuck-at-zero data line "
20307	"Error audio encoder SRAM access stuck-at-one data line "
20308	"Error audio encoder SRAM access stuck-at-one address line "
20309	"Error audio encoder SRAM access address line address line x is connected to data line data line y"
20310	"Error audio encoder SRAM access address lines address line x and address line y are connected "
20311	"Error audio encoder SRAM access data lines data line x and data line y are connected "
20312	"Error audio encoder SRAM access illegal data received"
20400	""
20401	"Error audio encoder access cannot initialise I2C"
20402	"Error audio encoder access cannot reset DSP through I2C"
20403	"Error audio encoder accessing ICR register"
20404	"Error audio encoder access stuck-at-zero of data line "
20405	"Error audio encoder access stuck-at-one of data line "
20406	"Audio encoder access data lines data line x and data line y are interconnected "
20500	""

Error Nr	Error String
20501	"Error audio encoder SRAM WRR cannot initialise I2C"
20502	"Error audio encoder SRAM WRR cannot reset DSP through I2C"
20503	"Error audio encoder WRR cannot download boot"
20504	"Error audio encoder cannot download test code"
20505	"Error audio encoder SRAM WRR cannot obtain result of test"
20506	"Error audio encoder WRR SRAM stuck-at-zero data bit "
20507	"Error audio encoder WRR SRAM stuck-at-one data bit "
20508	"Error audio encoder WRR SRAM data lines data line x and data line y are connected"
20509	"Error audio encoder WRR SRAM illegal data received"
20600	""
20601	"Error audio encoder interrupt cannot initialise I2C"
20602	"Error audio encoder interrupt cannot reset DSP through I2C"
20603	"Error audio encoder cannot download test code"
20604	"Error audio encoder interrupt cannot download boot"
20605	"Error occurred accessing VSM"
20606	"Audio encoder interrupt not received"
20700	""
20701	"Error audio encoder I2C cannot reset DSP through I2C"
20702	"Error audio encoder cannot download boot"
20703	"Error audio encoder cannot download TEST code"
20704	"Error audio encoder I2C bus busy"
20705	"Error audio encoder I2C cannot write slave address"
20706	"Error audio encoder I2C no acknowledge received"
20707	"Error audio encoder I2C cannot send/receive data"
20708	"Error audio encoder received data through I2C was invalid"
20800	""
20801	"I2C access failed."
20802	"SAA7118 VIP can not be initialised."
20803	"Invalid input"
30000	""
30001	"VSM SDRAM Bank1 Memory databus test goes wrong."
30002	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30003	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30004	" VSM SDRAM Bank2 Memory databus test goes wrong."
30005	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30006	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30007	"VSM SDRAM Bank1 VSM interrupt register A has a -stuck at- error for value:"
30008	"VSM SDRAM Bank2 VSM interrupt register A has a -stuck at- error for value:"
30100	""
30101	"VSM SDRAM Bank1 Memory databus test goes wrong."
30102	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30103	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30104	" VSM SDRAM Bank2 Memory databus test goes wrong."
30105	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30106	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30200	""
30201	"VSM SDRAM Bank1 Memory databus test goes wrong."
30202	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30203	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30204	" VSM SDRAM Bank2 Memory databus test goes wrong."
30205	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30206	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30300	""
30301	"VSM interrupt register A has a -stuck at- error for value:"
30302	"VSM interrupt register B has a -stuck at- error for value:"
30303	"Interrupt A wasn't raised."
30304	"Interrupt B wasn't raised."
30305	"Interrupts A and B were raised.'
30400	""
30401	"VSM SDRAM Bank1 Memory databus test goes wrong."
30402	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30403	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30404	" VSM SDRAM Bank2 Memory databus test goes wrong."
30405	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30406	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30500	""
30501	"Communication with the analogue board fails."
30502	"Echo test to analogue board returned wrong string."
40000	""
40001	"NVRAM Reset; I2C failed"
40100	"NVRAM address = 0xaddress -> Byte value = 0xvalue"
40101	"NVRAM Read; I2C failed"
40102	"NVRAM Read; Invalid input"
40200	""
40201	"NVRAM Modify; I2C failed"
40202	"NVRAM Modify; Invalid input"
40300	"DV Unique ID = id"
40301	"NVRAM Read DV Unique ID; I2C failed"
40400	"\r\n Error log:\r\n errorString \r\n"
40401	"NVRAM error log; I2C failed"
40402	"NVRAM error log is invalid"
40403	"Front panel failed"
40700	""
40701	"NVRAM error log reset; I2C failed"

Error Nr	Error String
40900	"Region code Change counter is reset"
40901	"NVRAM region code reset; I2C failed"
41000	""
41001	"NVRAM Store DV Unique ID; I2C failed"
41002	"NVRAM Store DV Unique ID; Invalid input"
50000	""
50007	"Execution of the command on the analogue board failed."
50008	"The frontpanel could not be accessed by the analogue board."
50009	"The echo from the frontpanel processor was not correct."
50100	" Front panel version: FPversion "
50102	"Execution of the command on the analogue board failed."
50103	"The frontpanel could not be accessed by the analogue board."
50200	""
50204	"Execution of the command on the analogue board failed."
50205	"The frontpanel could not be accessed by the analogue board."
50206	"The frontpanel did not show a starburst."
50207	"The user skipped the FP-which pattern test."
50208	"The user returned an unknown confirmation: confirmation "
50209	"The frontpanel did not show horizontal segments."
50210	"The frontpanel did not show vertical segments."
50300	""
50304	"Execution of the command on the analogue board failed."
50305	"The frontpanel could not be accessed by the analogue board."
50306	"The frontpanel did not light all labels."
50307	"The user skipped the rest of the FP-label test."
50308	"The user returned an unknown confirmation: confirmation"
50400	""
50404	"Execution of the command on the analogue board failed."
50405	"The frontpanel could not be accessed by the analogue board."
50406	"The LED's could not be turned on."
50407	"The user skipped the rest of the FP-LED test."
50408	"The user returned an unknown confirmation: confirmation"
50500	""
50502	"Front panel Keyboard; test failed"
50503	"Front panel Keyboard; test aborted"
50504	"Front panel Keyboard; not all keys were pressed"
50505	"Front panel keyboard I2C connection failed"
50600	""
50602	"Front panel Remote control; test failed"
50603	"Front panel Remote control; test aborted"
50604	"Front panel remote control; can not access FP"
50605	"Front panel remote control; no user input received"
50700	""
50701	"Execution of the command on the analogue board failed."
50702	"The frontpanel could not be accessed by the analogue board."
50703	"The frontpanel did not show a starburst."

Error Nr	Error String
50704	"The user skipped the FP-starburst test."
50705	"The user returned an unknown confirmation: confirmation "
50800	""
50801	"Execution of the command on the analogue board failed."
50802	"The frontpanel could not be accessed by the analogue board."
50803	"The frontpanel did not show vertical segments."
50804	"The user skipped the FP-vertical segments test."
50805	"The user returned an unknown confirmation: confirmation "
50900	""
50901	"Execution of the command on the analogue board failed."
50902	"The frontpanel could not be accessed by the analogue board."
50903	"The frontpanel did not show horizontal segments."
50904	"The user skipped the FP-horizontal segments test."
50905	"The user returned an unknown confirmation: confirmation "
51400	""
51401	"Execution of the command on the analogue board failed."
51402	"The frontpanel could not be accessed by the analogue board."
51403	"The beeper did not sound."
51404	"The user skipped the FP-Beep test."
51405	"The user returned an unknown confirmation: confirmation"
51500	""
51501	"Execution of the command on the analogue board failed."
51502	"The frontpanel could not be accessed by the analogue board."
51503	"The discbar did not display properly."
51504	"The user skipped the discbar test."
51505	"The user returned an unknown confirmation: confirmation"
51600	""
51601	"Execution of the command on the analogue board failed."
51602	"The frontpanel could not be accessed by the analogue board."
51603	"The discbar dots did not display properly."
51604	"The user skipped the discbar dots test."
51605	"The user returned an unknown confirmation: confirmation"
51700	""
51701	"Execution of the command on the analogue board failed."
51702	"The frontpanel could not be accessed by the analogue board."
51703	"The VU grid did not display properly."
51704	"The user skipped the VU gridtest."
51705	"The user returned an unknown confirmation: confirmation"
51800	""
51801	"Execution of the command on the analogue board failed."
51802	"The frontpanel could not be accessed by the analogue board."
51803	"The frontpanel could not be dimmed."

Error Nr	Error String
51804	"The user skipped the FP-Dim test."
51805	"The user returned an unknown confirmation: confirmation"
51900	""
51901	"Execution of the command on the analogue board failed."
51902	"The frontpanel could not be accessed by the analogue board."
51903	"The frontpanel did not show segments blinking."
51904	"The user skipped the FP-blinking test."
51905	"The user returned an unknown confirmation: confirmation"
52000	""
52001	"Execution of the command on the analogue board failed."
52002	"The frontpanel could not be accessed by the analogue board."
52003	"The frontpanel did not show all segments lit."
52004	"The user skipped the FP-light all segments test."
52005	"The user returned an unknown confirmation: confirmation"
52200	""
52201	"Communication with Analogue Board fails."
52202	"Frontpanel can not be accessed by the Analogue Board."
52300	""
52301	"Communication with Analogue Board fails."
52302	"Frontpanel can not be accessed by the Analogue Board."
60000	""
60100	""
60101	"Basic Engine returned error number 0xerrornumber"
60102	"Parity error from Basic Engine to Serial"
60103	"Communication time-out error"
60104	"Unexpected response from Basic Engine"
60105	"Echo loop could not be closed"
60106	"Wrong echo pattern received"
60200	"Version: nr1.nr2.nr3"
60201	"Basic Engine returned error number 0xerrornumber"
60202	"Parity error from Basic Engine to Serial"
60203	"Communication time-out error"
60204	"Unexpected response from Basic Engine"
60205	"Front Panel failed."
60300	""
60301	"Basic-Engine time-out error"
60400	""
60401	"Basic Engine returned error number 0xerrornumber"
60402	"Parity error from Basic Engine to Serial"
60403	"Communication time-out error"
60404	"Unexpected response from Basic Engine"
60405	"Focus loop could not be closed"
60500	""
60501	"Basic Engine returned error number 0xerrornumber"
60502	"Parity error from Basic Engine to Serial"
60503	"Communication time-out error"
60504	"Unexpected response from Basic Engine"
60600	""
60601	"Basic Engine returned error number 0xerrornumber"
60602	"Parity error from Basic Engine to Serial"
60603	"Communication time-out error"
60604	"Unexpected response from Basic Engine"
60700	""
60701	"Basic Engine returned error number 0xerrornumber"
60702	"Parity error from Basic Engine to Serial"
60703	"Communication time-out error"
60704	"Unexpected response from Basic Engine"
60800	""
60801	"Basic Engine returned error number 0xerrornumber"
60802	"Parity error from Basic Engine to Serial"
60803	"Communication time-out error"
60804	"Unexpected response from Basic Engine"
60805	"Radial loop could not be closed"
60900	""
60901	"Basic Engine returned error number 0xerrornumber"
60902	"Parity error from Basic Engine to Serial"
60903	"Communication time-out error"
60904	"Unexpected response from Basic Engine"
61500	""
61501	"Basic Engine returned error number 0xerrornumber"
61502	"Parity error from Basic Engine to Serial"
61503	"Communication time-out error"
61504	"Unexpected response from Basic Engine"
61600	""
61601	"Basic Engine returned error number 0xerrornumber"
61602	"Parity error from Basic Engine to Serial"
61603	"Communication time-out error"
61604	"Unexpected response from Basic Engine"
61700	""
61701	"BE tray-in command failed"
61702	"BE read-TOC command failed"
61703	"BE VSM interrupt initialisation failed"
61704	"BE set irq command failed"
61705	"BE no disc or wrong disc inserted"
61706	"BE rec-pause command failed"
61707	"BE VSM BE out DMA initialisation failed"
61708	"BE VSM BE out initialisation failed"
61709	"BE VSM BE out DMA start failed"
61710	"BE VSM BE out start failed"
61711	"BE rec command failed"
61712	"BE VSM out underrun error occurred"
61713	"BE record complete interrupt not raised"
61714	"BE get irq command failed"
61715	"BE no interrupt was raised by BE"
61716	"BE VSM DMA out not finished"
61717	"BE stop command after writing failed"
61718	"BE VSM Sector processor initialisation failed"
61719	"BE VSM sector processor DMA initialisation failed"
61720	"BE VSM sector processor DMA start failed"
61721	"BE VSM sector processor start failed"
61722	"BE seek command failed"
61723	"BE VSM sector processor error occurred"
61724	"BE read timeout occurred"
61725	"BE stop command after reading failed"

Error Nr	Error String
61726	"BE difference found in data at disc sector 0xdiscsector"
61727	"This nucleus cannot be executed because the Self-Test failed"
61800	""
61801	"BE i2c initialisation failed"
61802	"This nucleus cannot be executed because the Self-Test failed"
61900	""
61901	"The SelfTest failed with result: 0xnr1 0xnr2 0xnr3"
61902	"Basic Engine returned error number 0xerrornumber"
61903	"Parity error from Basic Engine to Serial"
61904	"Communication time-out error"
61905	"Unexpected response from Basic Engine"
62000	""
62001	"Self-Test : errorstring1 Laser-Test : errorstring2 SpindleM-Test: errorstring3 SledgeM-Test : errorstring4 Focus-Test : errorstring5"
62100	"The forward sense level is 0xlevel"
62101	"Basic Engine returned error number 0xerrornumber"
62102	"Parity error from Basic Engine to Serial"
62103	"Communication time-out error"
62104	"Unexpected response from Basic Engine"
62200	""
62201	"The BE-self-diagnostic-spindle-motor-test failed"
62202	"Basic Engine returned error number 0xerrornumber"
62203	"Parity error from Basic Engine to Serial"
62204	"Communication time-out error"
62205	"Unexpected response from Basic Engine"
62300	""
62301	"The BE-focus-test failed"
62302	"Basic Engine returned error number 0xerrornumber"
62303	"Parity error from Basic Engine to Serial"
62304	"Communication time-out error"
62305	"Unexpected response from Basic Engine"
62400	""
62401	"The BE-self-diagnostic-sledge-motor-test failed"
62402	"Basic Engine returned error number 0xerrornumber"
62403	"Parity error from Basic Engine to Serial"
62404	"Communication time-out error"
62405	"Unexpected response from Basic Engine"
62500	""
62600	""
62700	"BE EEPROM address = address -> Byte value = 0xvalue"
62701	"Basic Engine returned error number 0xerrornumber"
62702	"Parity error from Basic Engine to Serial"
62703	"Communication time-out error"
62704	"Unexpected response from Basic Engine"
62705	"BE read EEPROM; invalid input"
62800	""
62801	"Basic Engine returned error number 0xerrornumber"
62802	"Parity error from Basic Engine to Serial"
62803	"Communication time-out error"

Error Nr	Error String
62804	"Unexpected response from Basic Engine"
62805	"BE write EEPROM; invalid input"
62900	""
62901	"Basic Engine returned error number 0xerrornumber"
62902	"Parity error from Basic Engine to Serial"
62903	"Communication time-out error"
62904	"Unexpected response from Basic Engine"
62905	"Radial loop could not be closed"
63000	""
63001	"Basic Engine returned error number 0xerrornumber"
63002	"Parity error from Basic Engine to Serial"
63003	"Communication time-out error"
63004	"Unexpected response from Basic Engine"
63100	" Number of times Tray went Open/Closed : nr1" " Total hours the CD laser was on : nr2" " Total hours the DVD laser was on : nr3" " Total hours the write laser was on : nr4"
63101	"Basic Engine returned error number 0xerrornumber"
63102	"Parity error from Basic Engine to Serial"
63103	"Communication time-out error"
63104	"Unexpected response from Basic Engine"
63200	""
63201	"Basic Engine returned error number 0xerrornumber"
63202	"Parity error from Basic Engine to Serial"
63203	"Communication time-out error"
63204	"Unexpected response from Basic Engine"
63300	Momentary errors (Byte 1 - Byte 7) : 0xb1 0xb2 0xb3 0xb4 0xb5 0xb6 0xb7 Cumulative errors (Byte 1 - Byte 7): : 0xb1 0xb2 0xb3 0xb4 0xb5 0xb6 0xb7 Fatal errors (Oldest - Youngest) : : 0xb1 0xb2 0xb3 0xb4 0xb5
63301	"Basic Engine returned error number 0xerrornumber"
63302	"Parity error from Basic Engine to Serial"
63303	"Communication time-out error"
63304	"Unexpected response from Basic Engine"
63400	""
63401	"Basic Engine returned error number 0xerrornumber"
63402	"Parity error from Basic Engine to Serial"
63403	"Communication time-out error"
63404	"Unexpected response from Basic Engine"
63500	""
63501	"Basic Engine returned error number 0xerrornumber"
63502	"Parity error from Basic Engine to Serial"
63503	"Communication time-out error"
63504	"Unexpected response from Basic Engine"
63505	"errorstring The basic engine will reject all player commands"
63900	""
63901	"Basic Engine returned error number 0xerrornumber"
63902	"Parity error from Basic Engine to Serial"
63903	"Communication time-out error"
63904	"Unexpected response from Basic Engine"
70000	"Echo test OK"
70001	"Echo test returned wrong string."
70002	"Communication with Analogue Board fails"

Error Nr	Error String
70300	"SoftwareVersion"
70301	"Can not find segment in FLASH ROM on the Analogue Board"
70302	"Communication with Analogue Board fails"
70400	"HardwareVersion"
70401	"Can not find segment in FLASH ROM on the Analogue Board"
70402	"Communication with Analogue Board fails"
70500	"Clock adjusted OK"
70501	"Can not adjust the clock on the Analogue Board."
70502	"Wrong date/time text size."
70503	"Communication with Analogue Board fails"
70600	"Tuner accessibility test OK"
70601	"Can not access tuner on the Analogue Board."
70602	"Communication with Analogue Board fails"
70700	"Frequency download OK"
70701	"Wrong frequency table size."
70702	"Can not download the frequency table into the analogue NVRAM."
70703	"Can not download the frequency table into the analogue NVRAM."
70704	"Communication with Analogue Board fails"
70800	"Data slicer test OK"
70801	"Test of the Data slicer on the Analogue Board fails."
70802	"Communication with Analogue Board fails"
70900	"Sound Processor test OK"
70901	"Test of the Sound Processor on the Analogue Board fails."
70902	"Communication with Analogue Board fails"
71000	"AV Selector test OK"
71001	"Test of the AV Selector on the Analogue Board fails."
71002	"Communication with Analogue Board fails"
71100	"NVRAM test OK"
71101	"Test of the NVRAM on the Analogue Board fails."
71102	"Communication with Analogue Board fails"
71200	"Video routing on the Analogue Board OK"
71201	"Routing the video on the Analogue Board fails."
71202	"Invalid input."
71203	"Communication with Analogue Board fails"
71300	"Audio routing on the Analogue Board OK"
71301	"Routing the audio on the Analogue Board fails."
71302	"Invalid input."
71303	"Communication with Analogue Board fails"
71400	"Audio routing on the Analogue Board OK"
71401	"Can not access switching matrix."
71402	"CVBS signal is invalid."
71403	"Communication with Analogue Board fails"
71500	""
71501	"Invalid slash version, default slash version is set."
71502	"Setting the slash version on the Analogue Board fails."
71503	"Communication with Analogue Board fails"
71600	"ApplicationVersion"
71601	"Can not find segment in FLASH ROM on the Analogue Board"
71602	"Communication with Analogue Board fails"
71700	"DiagnosticsVersion"
71701	"Can not find segment in FLASH ROM on the Analogue Board"
71702	"Communication with Analogue Board fails"
71800	"DownloadVersion"

Error Nr	Error String
71801	"Can not find segment in FLASH ROM on the Analogue Board"
71802	"Communication with Analogue Board fails"
72300	""
72301	"Clearing the NVRAM on the Analogue Board fails"
72302	"Communication with Analogue Board fails"
72400	"segment checksum is : checksum which is correct" for every segment
72401	"segment could not be found" or "segment checksum is : checksumC ,however it should be : checksumE" for every segment
72402	"Communication with Analogue Board fails"
73000	""
73001	"Storing the external presets on the Analogue Board fails"
73002	"Communication with Analogue Board fails"
80000	"The DVIO module is present in the system."
80001	"The DVIO module is not present in the system."
80100	"The DVIO module has been reset OK."
80101	"The DVIO module is not present in the system."
80102	"The DVIO module could not be reset."
80103	"Could not initialise I2C before Reset."
80200	"The accessibility of the DVIO module is OK."
80201	"The DVIO board is not present in this DVDR."
80202	"Could not initialise I2C."
80203	"Unable to reset the DVIO module."
80204	"Unable to receive the reset indication from the DVIO module."
80205	"Unable to send the configuration to the DVIO module."
80206	"Unable to download the chip ID to the DVIO module."
80207	"Unable to set the mode of the DVIO module to IDLE."
80208	"Software Error in function HandleStateAwaitingReply !!"
80209	"Maximal number of retries reached by HandleStateSending !!"
80210	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80211	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80212	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80213	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80214	"VSM UART error timeout transmitting command"
80215	"VSM UART error timeout receiving reply"
80216	"VSM UART frame error occurred receiving from DVIO board"
80217	"VSM UART parity error occurred receiving from DVIO board"
80218	"The confirmation/indication from the DVIO module is invalid."
80300	"The accessibility of the DVIO module is OK."
80301	"The DVIO board is not present in this DVDR."
80302	"Could not initialise I2C."
80303	"Unable to reset the DVIO module."
80304	"Unable to receive the reset indication from the DVIO module."
80305	"Unable to send the configuration to the DVIO module."
80306	"Unable to download the chip ID to the DVIO module."

Error Nr	Error String
80307	"Unable to set the mode of the DVIO module to IDLE."
80308	"Software Error in function HandleStateAwaitingReply !!"
80309	"Maximal number of retries reached by HandleStateSending !!"
80310	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80311	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80312	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80313	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80314	"VSM UART error timeout transmitting command"
80315	"VSM UART error timeout receiving reply"
80316	"VSM UART frame error occurred receiving from DVIO board"
80317	"VSM UART parity error occurred receiving from DVIO board"
80318	"The confirmation/indication from the DVIO module is invalid."
80400	"The accessibility of the DVIO module is OK."
80401	"The DVIO board is not present in this DVDR."
80402	"Could not initialise I2C."
80403	"Unable to reset the DVIO module."
80404	"Unable to receive the reset indication from the DVIO module."
80405	"Unable to send the configuration to the DVIO module."
80406	"Unable to download the chip ID to the DVIO module."
80407	"Unable to set the mode of the DVIO module to IDLE."
80408	"Software Error in function HandleStateAwaitingReply !!"
80409	"Maximal number of retries reached by HandleStateSending !!"
80410	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80411	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80412	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80413	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80414	"VSM UART error timeout transmitting command"
80415	"VSM UART error timeout receiving reply"
80416	"VSM UART frame error occurred receiving from DVIO board"
80417	"VSM UART parity error occurred receiving from DVIO board"
80418	"The confirmation/indication from the DVIO module is invalid."
90000	""
90001	"Error cannot initialise I2C"
90002	"Error cannot initialise VIP"
90003	"Error cannot clear ADC enable pin"
90004	"Error cannot set VSM audio clock"
90005	"Error cannot initialise audio encoder"
90006	"Error cannot initialise VSM audio in port"
90007	"Error cannot initialise VSM audio in DMA port"
90008	"Error cannot initialise VSM audio out DMA port"
90009	"Error cannot initialise host decoder audio in"
90010	"Error cannot initialise audio VSM out port"

Error Nr	Error String
90011	"Error digital loop audio cannot start audio encoder"
90012	"Error cannot start VSM audio in DMA port"
90013	"Error cannot start VSM audio in port"
90014	"Error transfer data from audio encoder to VSM"
90015	"Error cannot start VSM AV out DMA port"
90016	"Error cannot start VSM AV out port"
90017	"Error transfer data from VSM to host decoder"
90018	"Error digital loop audio data in host memory and VSM memory differ"
90019	"Error digital loop audio data is not a valid MPEG stream"
90020	"Error digital loop audio data is not a digital silence"
90100	""
90101	"Error routing the audio back to the digital board."
90102	"Error cannot initialise I2C"
90103	"Error cannot initialise VIP"
90104	"Error cannot set ADC enable pin"
90105	"Error cannot set VSM audio clock"
90106	"Error preparing the 12kHz audio-sine"
90107	"Error cannot initialise audio encoder"
90108	"Error cannot initialise VSM audio in port"
90109	"Error cannot initialise VSM audio in DMA port"
90110	"Error cannot initialise VSM audio out DMA port"
90111	"Error cannot initialise audio VSM out port"
90112	"Error cannot initialise host decoder audio in"
90113	"Error loop audio user/dealer cannot start audio encoder"
90114	"Error cannot start VSM audio in DMA port"
90115	"Error starting the 12kHz audio-sine"
90116	"Error transfer data from audio encoder to VSM"
90117	"Error cannot start VSM AV out DMA port"
90118	"Error cannot start VSM AV out port"
90119	"Error transfer data from VSM to host decoder"
90120	"Error: audio data in host memory and VSM memory differ"
90121	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90122	"Error: audio data in host memory contains silence!"
90123	"There is no correct audio frame in the buffer"
90124	"The audio frame has an illegal version bit"
90125	"The audio frame has an illegal bitrate-index"
90126	"The audio frame has an illegal sampling rate"
90127	"The CRC of the audio frame is wrong"
90128	"The audio frame is not MPEG-I layer II !"
90129	"Error cannot de-mute DAC on analogue board"
90200	""
90201	"Initialisation of I2C failed"
90202	"Initialisation of VIP and EMPIRE failed"
90203	"Initialisation of PLL / Link failed."
90204	"Next descriptor address set wrong."
90205	"Turning on the colourbar failed"
90206	"No I2C communication possible to start video encoder."
90207	"Starting the video encoder failed."
90208	"Transfer of data from video encoder to VSM failed."
90209	"Stopping the encoder failed."
90210	"Turning off the colourbar failed."
90211	"Cannot intialize hostdecoder parallel input"
90212	"Cannot initialise VSM AV-out DMA port"

Error Nr	Error String
90213	"Cannot initialise VSM AV-out port"
90214	"Cannot start VSM AV-out DMA port"
90215	"Cannot start VSM AV-out port"
90216	"Transfer of data from VSM to host decoder failed."
90217	"VSM and Hostdec memory do not match (compared after transfer)"
90218	"Decoding of the video data in the hostdecoder memory failed"
90219	"The data in the hostdecoder is not equal to a colourbar"
90220	"The video encoder did not return the Group Of Picture count."
90221	"The video encoder did not receive data from the VIP."
90223	"Initialisation of VIP and EMPRESS failed"
90224	"The video encoder did not return the current status."
90225	"The video encoder timed out in BUSY mode. (no VIP input)"
90226	"The video encoder did not return the current bitrate."
90227	"The video encoder did not switch to ENCODING mode."
90228	"The video encoder could not start from STOP/IDLE mode."
90229	"The video encoder did not switch from IDLE to STOP mode."
90300	""
90301	"Initialisation of I2C failed"
90302	"I2C communication to VIP failed"
90303	"Initialisation of VIP failed"
90304	"Generation of Close Caption data failed"
90305	"VIP not locked to video signal"
90306	"Initialisation of VBI Extractor failed
90307	"No CC data received"
90308	"Closed Caption data overrun"
90309	"Closed Caption data does not match"
90310	"Switch off ColourBar failed"
90400	""
90401	"Initialisation of I2C failed"
90402	"Initialisation of VIP and EMPIRE failed"
90403	"Initialisation of PLL / Link failed."
90404	"Next descriptor address set wrong."
90405	"Turning on the colourbar failed"
90406	"No I2C communication possible to start video encoder."
90407	"Starting the video encoder failed."
90408	"Transfer of data from video encoder to VSM failed."
90409	"Stopping the encoder failed."
90410	"Turning off the colourbar failed."
90411	"Cannot intialize hostdecoder parallel input"
90412	"Cannot initialise VSM AV-out DMA port"
90413	"Cannot initialise VSM AV-out port"
90414	"Cannot start VSM AV-out DMA port"
90415	"Cannot start VSM AV-out port"
90416	"Transfer of data from VSM to host decoder failed."
90417	"VSM and Hostdec memory do not match (compared after transfer)"
90418	"Decoding of the video data in the hostdecoder memory failed"
90419	"The data in the hostdecoder is not equal to a colourbar"
90420	"The video encoder did not return the Group Of Picture count."
90421	"The video encoder did not receive data from the VIP."
90422	"Execution of the command on the analogue board failed."
90423	"Initialisation of VIP and EMPRESS failed"
90424	"The video encoder did not return the current status."
90425	"The video encoder timed out in BUSY mode. (no VIP input)"
90426	"The video encoder did not return the current bitrate."
90427	"The video encoder did not switch to ENCODING mode."
90428	"The video encoder could not start from STOP/IDLE mode."
90429	"The video encoder did not switch from IDLE to STOP mode."
90500	""
90501	"Initialisation of I2C failed"
90502	"I2C communication to VIP failed"
90503	"Initialisation of VIP failed"
90504	"Generation of Close Caption data failed"
90505	"VIP not locked to video signal"
90506	"Initialisation of VBI Extractor failed
90507	"No CC data received"
90508	"Closed Caption data overrun"
90509	"Closed Caption data does not match"
90510	"Switch off ColourBar failed"
90511	"Execution of the command on the analogue board failed."
90600	""
90601	"Initialisation of I2C failed"
90602	"Initialisation of VIP and EMPIRE failed"
90603	"Initialisation of PLL / Link failed"
90604	"Next descriptor address set wrong."
90605	"Turning on the colourbar failed'
90606	"No I2C communication possible to start video encoder."
90607	"Starting the video encoder failed."
90608	"Transfer of data from video encoder to VSM failed."
90609	"Stopping the encoder failed."
90610	"Turning off the colourbar failed."
90611	"Cannot intialize hostdecoder parallel input"
90612	"Cannot initialise VSM AV-out DMA port"
90613	"Cannot initialise VSM AV-out port"
90614	"Cannot start VSM AV-out DMA port"
90615	"Cannot start VSM AV-out port"
90616	"Transfer of data from VSM to host decoder failed."
90617	"VSM and Hostdec memory do not match (compared after transfer)"
90618	"Decoding of the video data in the hostdecoder memory failed"
90619	"The data in the hostdecoder is not equal to a colourbar"
90620	"The video encoder did not return the Group Of Picture count."
90621	"The video encoder did not receive data from the VIP."

Error Nr	Error String
90622	"Execution of the command on the analogue board failed."
90623	"Initialisation of VIP and EMPRESS failed"
90624	"The video encoder did not return the current status."
90625	"The video encoder timed out in BUSY mode. (no VIP input)"
90626	"The video encoder did not return the current bitrate."
90627	"The video encoder did not switch to ENCODING mode."
90628	"The video encoder could not start from STOP/ IDLE mode."
90629	"The video encoder did not switch from IDLE to STOP mode."
90700	""
90701	"Initialisation of I2C failed"
90702	"I2C communication to VIP failed"
90703	"Initialisation of VIP failed"
90704	"Generation of Close Caption data failed"
90705	"VIP not locked to video signal"
90706	"Initialisation of VBI Extractor failed
90707	"No CC data received"
90708	"Closed Caption data overrun"
90709	"Closed Caption data does not match"
90710	"Switch off ColourBar failed"
90711	"Execution of the command on the analogue board failed."
90800	""
90801	"Error routing the audio back to the digital board."
90802	"Error cannot initialise I2C"
90803	"Error cannot initialise VIP"
90804	"Error cannot set ADC enable pin"
90805	"Error cannot set VSM audio clock"
90806	"Error preparing the 12kHz audio-sine"
90807	"Error cannot initialise audio encoder"
90808	"Error cannot initialise VSM audio in port"
90809	"Error cannot initialise VSM audio in DMA port"
90810	"Error cannot initialise VSM audio out DMA port"
90811	"Error cannot initialise audio VSM out port"
90812	"Error cannot initialise host decoder audio in"
90813	"Error loop audio user/dealer cannot start audio encoder"
90814	"Error cannot start VSM audio in DMA port"
90815	"Error starting the 12kHz audio-sine"
90816	"Error transfer data from audio encoder to VSM"
90817	"Error cannot start VSM AV out DMA port"
90818	"Error cannot start VSM AV out port"
90819	"Error transfer data from VSM to host decoder"
90820	"Error: audio data in host memory and VSM memory differ"
90821	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90822	"Error: audio data in host memory contains silence!"
90823	"There is no correct audio frame in the buffer"
90824	"The audio frame has an illegal version bit"
90825	"The audio frame has an illegal bitrate-index"
90826	"The audio frame has an illegal sampling rate"
90827	"The CRC of the audio frame is wrong"
90828	"The audio frame is not MPEG-I layer II !"
90829	"Error cannot de-mute DAC on analogue board"
90900	""
90901	"Error routing the audio back to the digital board."
90902	"Error cannot initialise I2C"
90903	"Error cannot initialise VIP"
90904	"Error cannot set ADC enable pin"
90905	"Error cannot set VSM audio clock"
90906	"Error preparing the 12kHz audio-sine"
90907	"Error cannot initialise audio encoder"
90908	"Error cannot initialise VSM audio in port"
90909	"Error cannot initialise VSM audio in DMA port"
90910	"Error cannot initialise VSM audio out DMA port"
90911	"Error cannot initialise audio VSM out port"
90912	"Error cannot initialise host decoder audio in"
90913	"Error loop audio user/dealer cannot start audio encoder"
90914	"Error cannot start VSM audio in DMA port"
90915	"Error starting the 12kHz audio-sine"
90916	"Error transfer data from audio encoder to VSM"
90917	"Error cannot start VSM AV out DMA port"
90918	"Error cannot start VSM AV out port"
90919	"Error transfer data from VSM to host decoder"
90920	"Error: audio data in host memory and VSM memory differ"
90921	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90922	"Error: audio data in host memory contains silence!"
90923	"There is no correct audio frame in the buffer"
90924	"The audio frame has an illegal version bit"
90925	"The audio frame has an illegal bitrate-index"
90926	"The audio frame has an illegal sampling rate"
90927	"The CRC of the audio frame is wrong"
90828	"The audio frame is not MPEG-I layer II !"
90929	"Error cannot de-mute DAC on analogue board"
140000	""
140001	"I2C to Clock failed" or "I2C initialisation failed"
140100	""
140101	"I2C to Clock failed" or "I2C initialisation failed"

5.5 Loop Tests

The following loops can be distinguished:

- Loops performed on the digital board only
- User Dealer loops performed on the digital and analogue board
- System loops performed via an external connection: outputs are looped back to the inputs.

5.5.1 Nucleus 900: Digital Audio Loop

This nucleus tests the audio path through the digital board

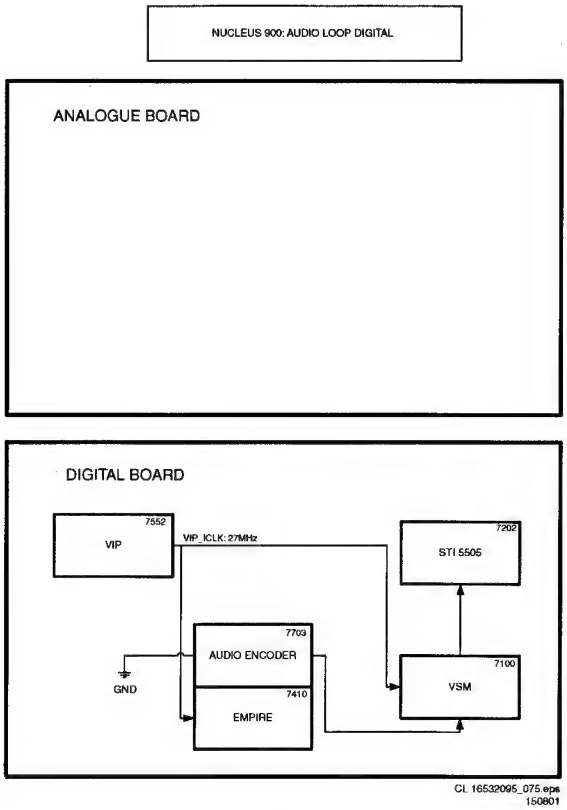


Figure 5-9

5.5.2 Nucleus 901: Audio User Dealer Loop

A PCM audio sine of 12kHz is generated in the Sti5505 for a while and sent to the analogue board. The signal coming from the analogue board is encoded again and sent to the memory of the host decoder for comparison. This nucleus tests the components on the audio signal path:

- Host decoder Sti5505
- Flex connection between connector 1602 (digital board) and connector 1900 (analogue board)
- DAC
- Op-amp
- Scart switch STV6410
- ADC
- Audio Encoder
- VIP
- VSM

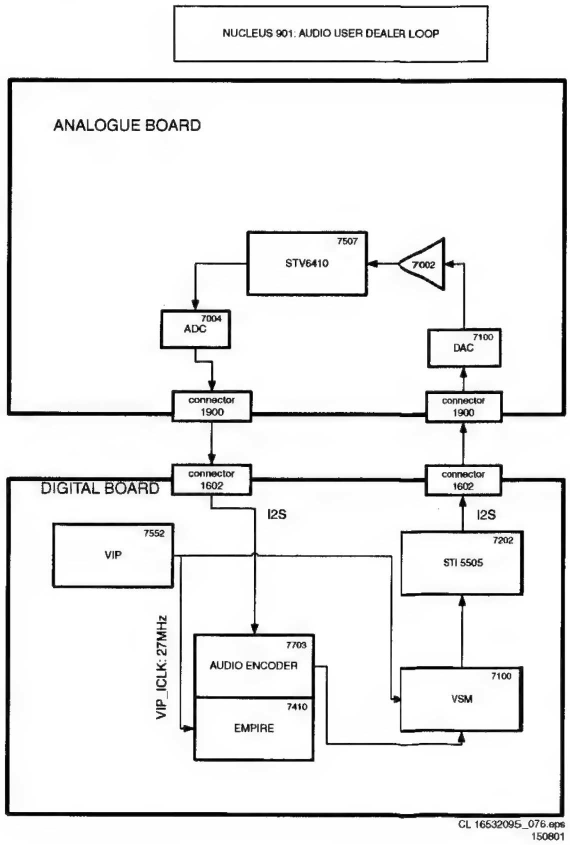


Figure 5-10

5.5.3 Nucleus 902: Digital Video Loop

A colourbar generated in the host decoder is looped through the VIP, Empire, and VSM and checked again in the host decoder. The following components are tested on the video signal path:

- VIP
- Empire
- VSM
- Host decoder

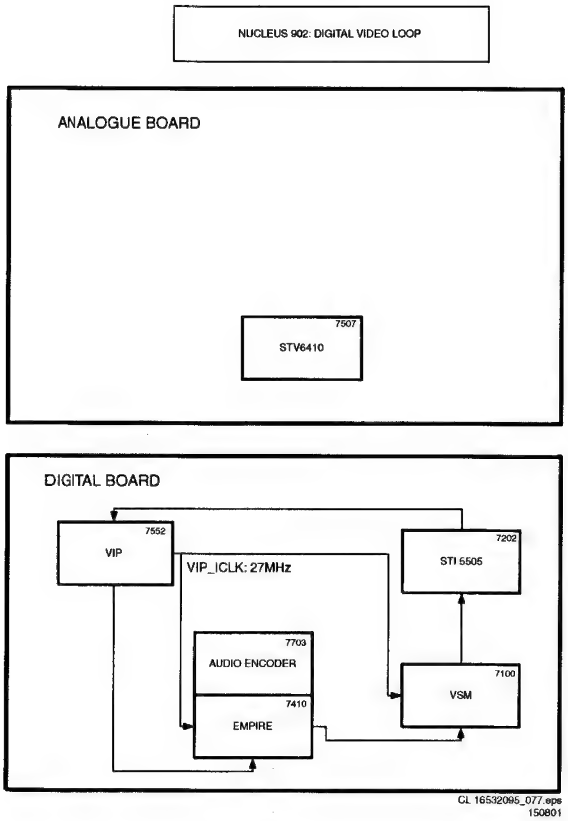


Figure 5-11

5.5.4 Nucleus 903: Digital Video VBI Loop

Nucleus for testing the components on the video VBI signal path:

- The VIP
- The VSM
- The Host Decoder

This is done by using the internal test signal source (digital board only)

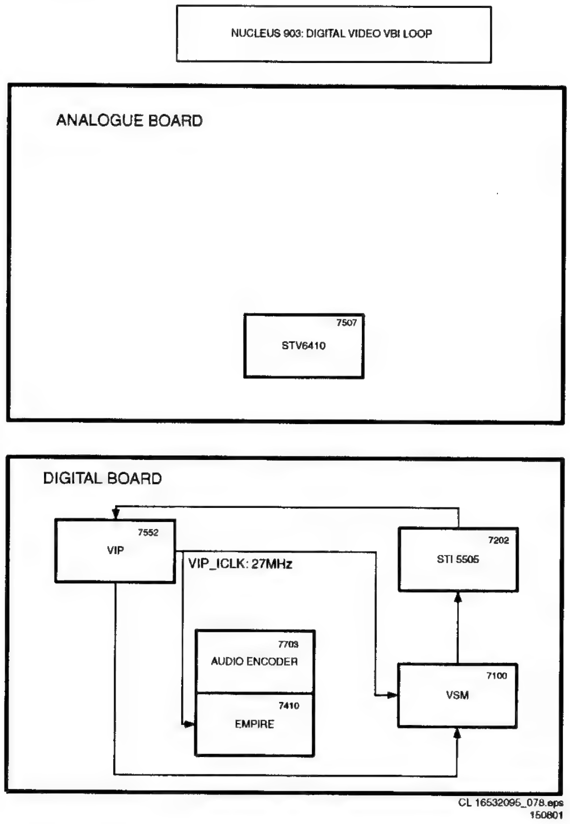


Figure 5-12

5.5.5 Nucleus 904: System Video Loop

Nucleus for testing the components on the video signal system path:

- The VIP
- The video encoder
- The VSM
- The host decoder
- The analogue board

On the analogue board the video signal will be routed to the SCART (EUROPE) or CINCH (NAFTA). There it will be looped back externally by means of the proper cable

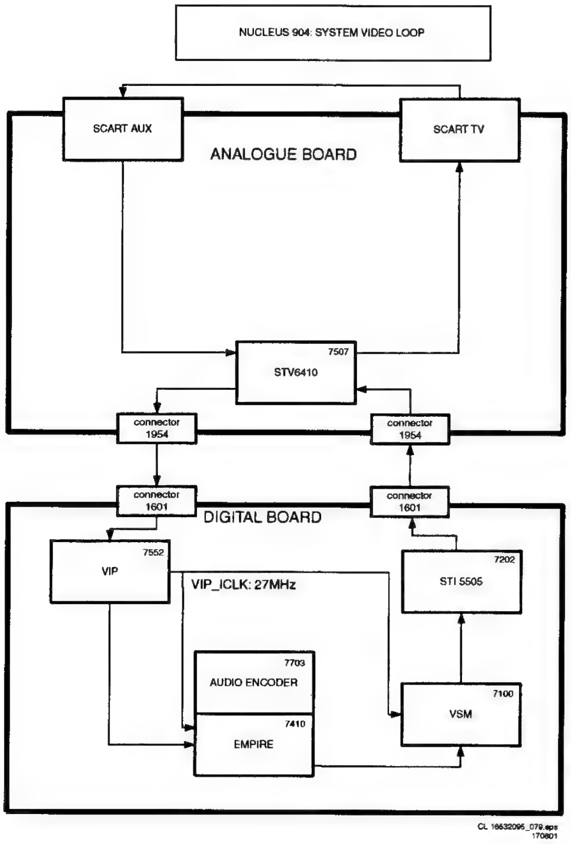


Figure 5-13

5.5.6 Nucleus 905: System Video VBI Loop

This nucleus tests the components on the video signal path:

- The VIP
- The VSM
- The Host Decoder

The video CVBS signal is routed to the output of the analogue board where it will be looped back by means of an external cable

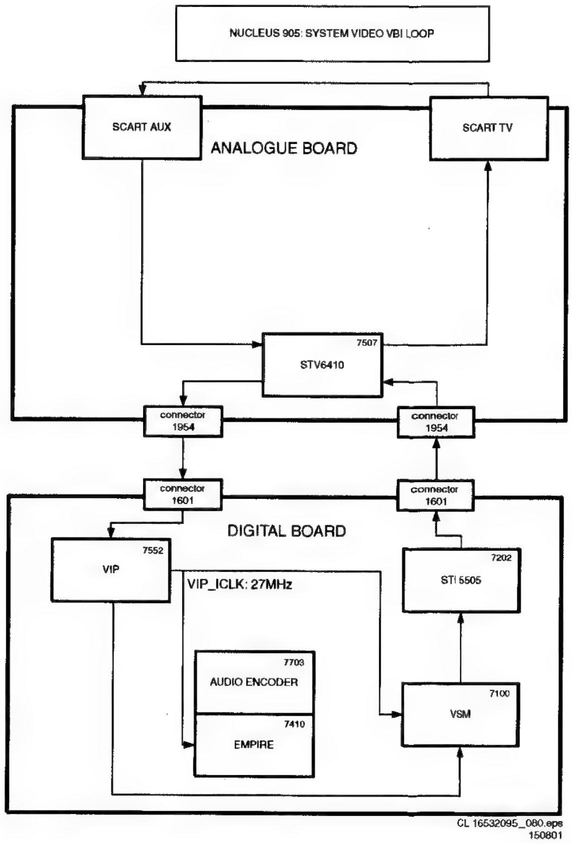


Figure 5-14

5.5.7 Nucleus 906: Video User Dealer Loop

Nucleus for testing the components on the video signal system path:

- The VIP
- The video encoder
- The VSM
- The host decoder
- The analogue board

On the analogue board, the video signal is internally routed back to the digital board.

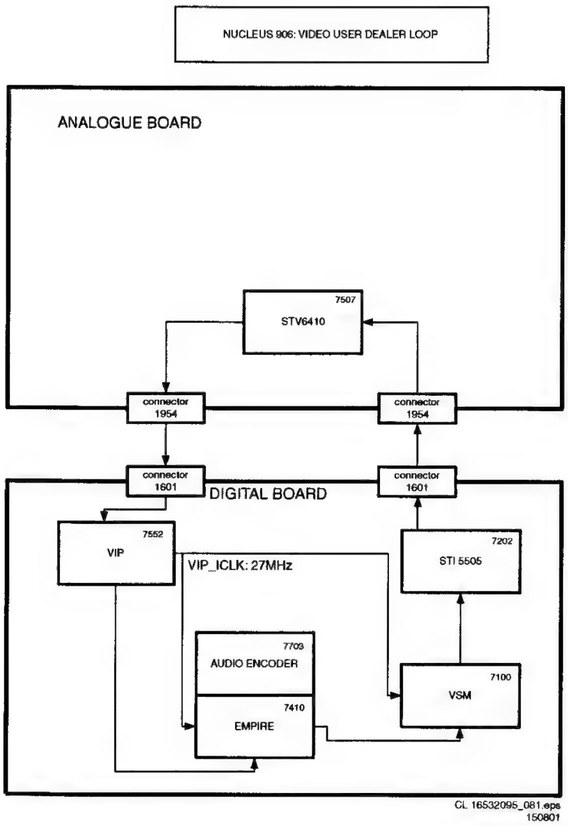


Figure 5-15

5.5.8 Nucleus 907: Video VBI User Dealer Loop

This nucleus tests the components on the video VBI signal path:

- The VIP
- The VSM
- The Host Decoder

The signal is routed back internally on the analogue board

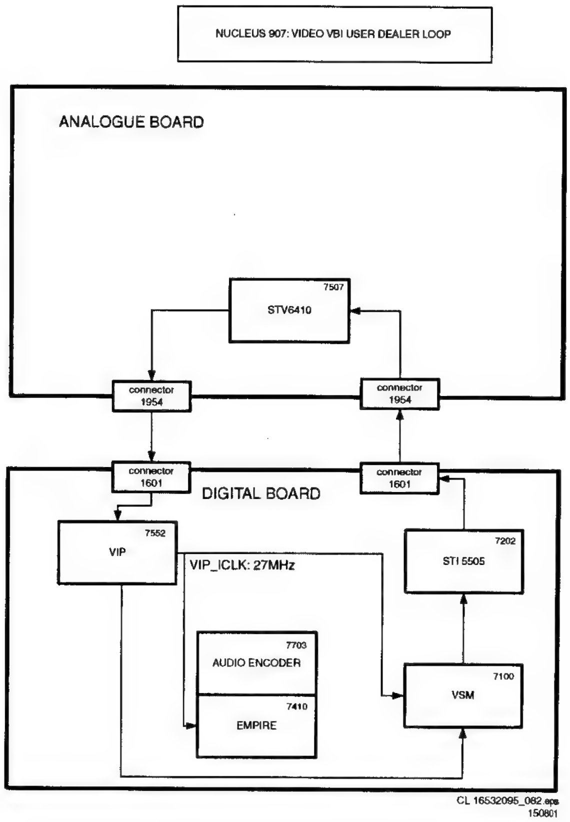


Figure 5-16

5.5.9 Nucleus 908: System Audio Loop Scart

Nucleus for testing the components on the audio signal path:

- The hostdecoder
- The analogue board
- The audio encoder
- The VSM

On the analogue board, audio is passed to the SCART connector, where a SCART cable needs to be used to loop back the audio signal to the digital board

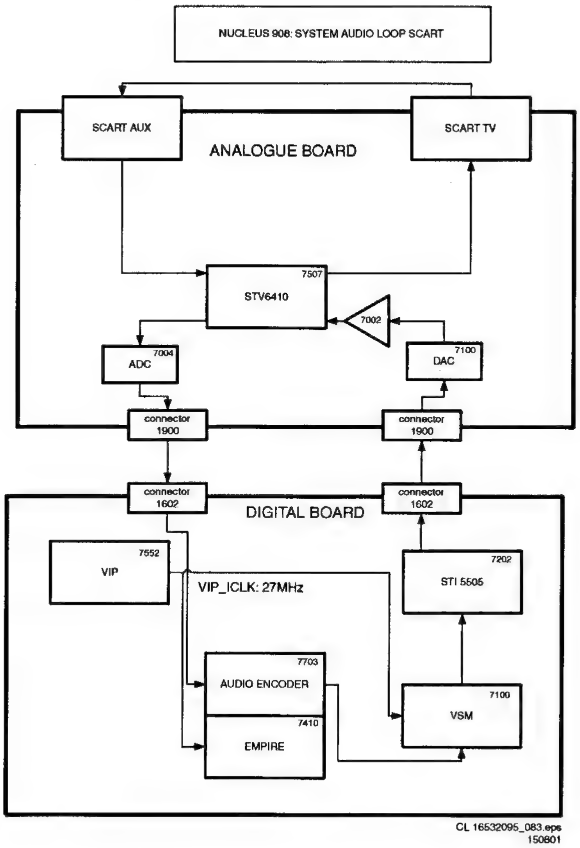


Figure 5-17

5.5.10 Nucleus 909: System Audio Loop CINCH

Nucleus for testing the components on the audio signal path:

- The hostdecoder
- The analogue board
- The audio encoder
- The VSM

On the analogue board the audio is passed to the CINCH connector, where a CINCH cable needs to be used to loop back the audio signal to the digital board

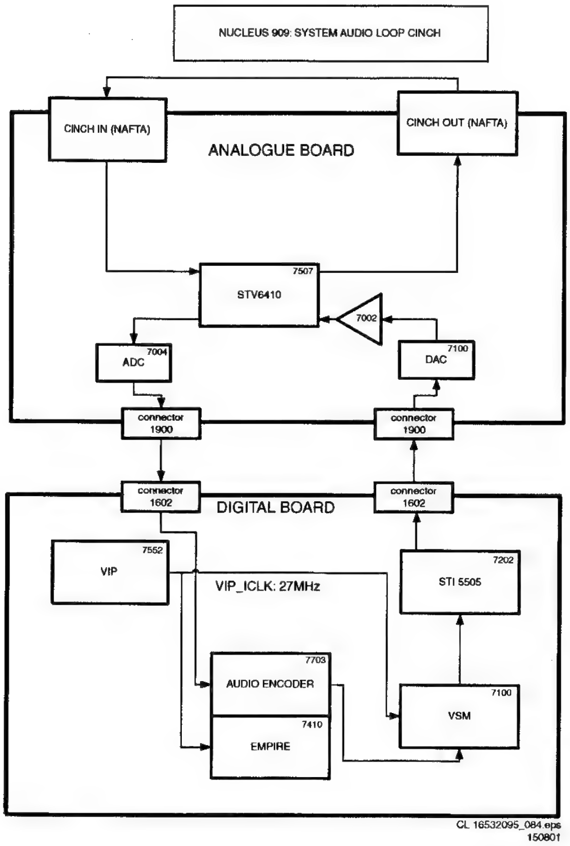
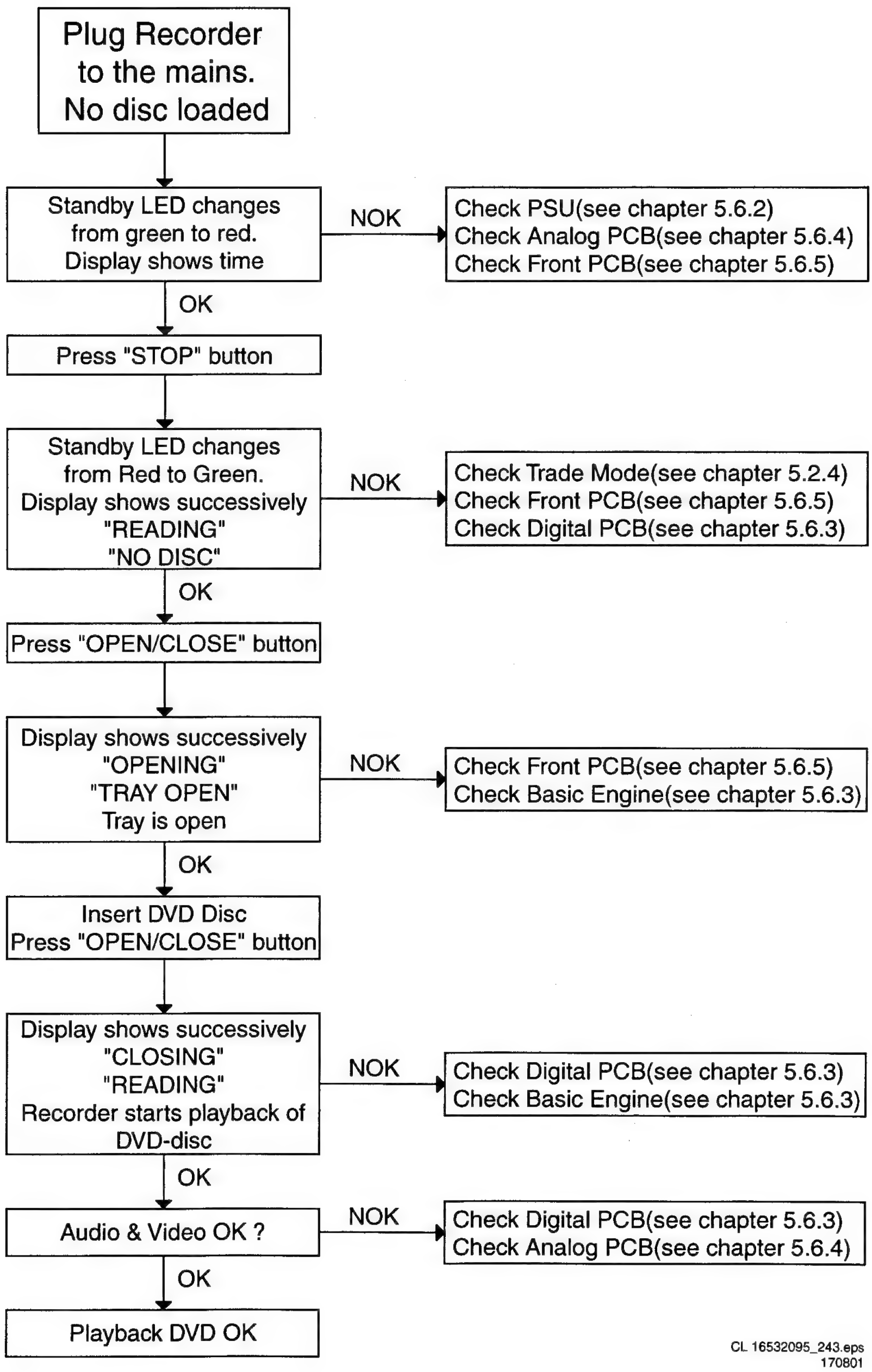


Figure 5-18

5.6 Faultfinding Trees

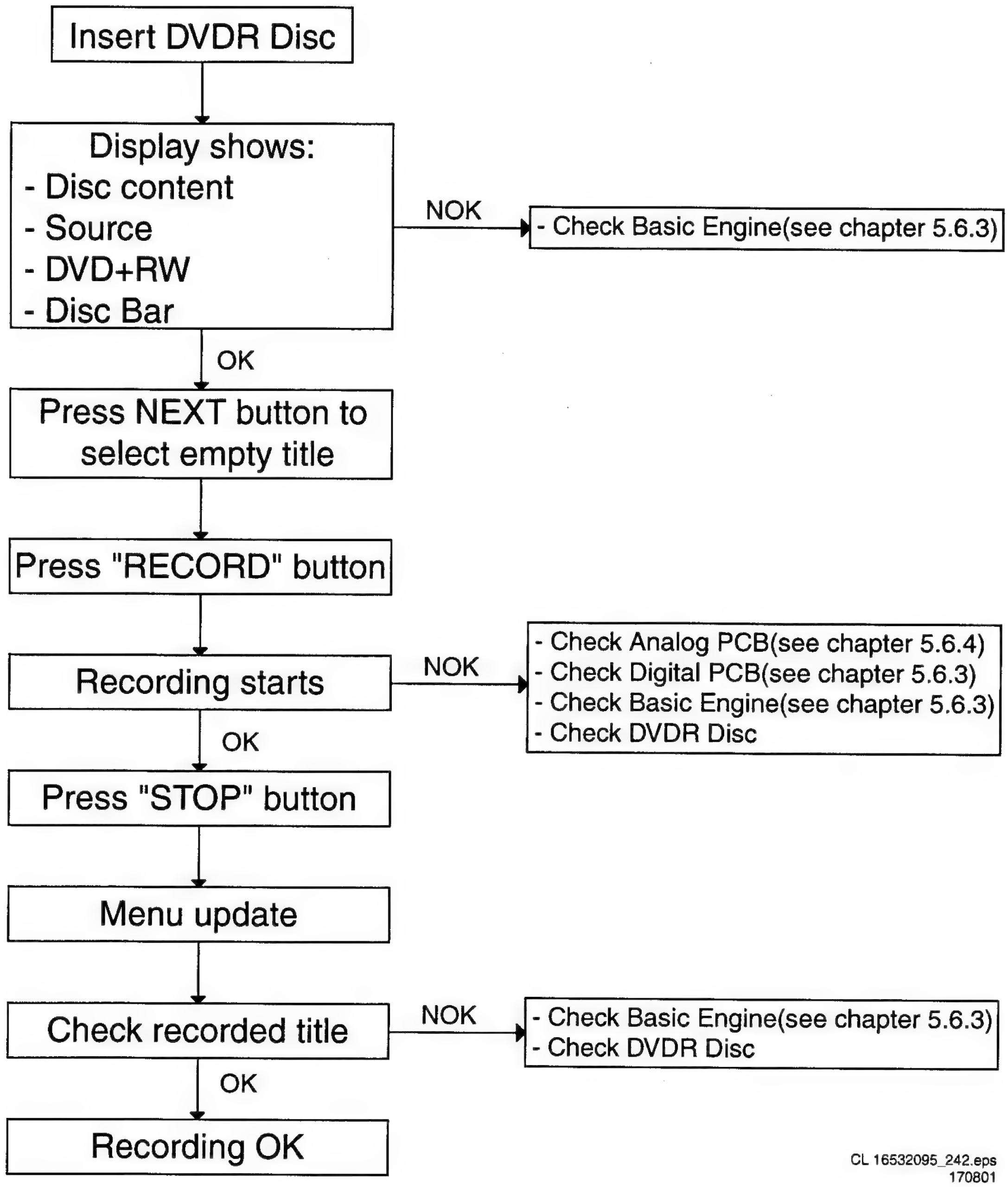
5.6.1 General

PLAYBACK MODE



CL 16532095_243.eps
170801

RECORD MODE



CL 16532095_242.eps
170801

5.6.2 Power Supply

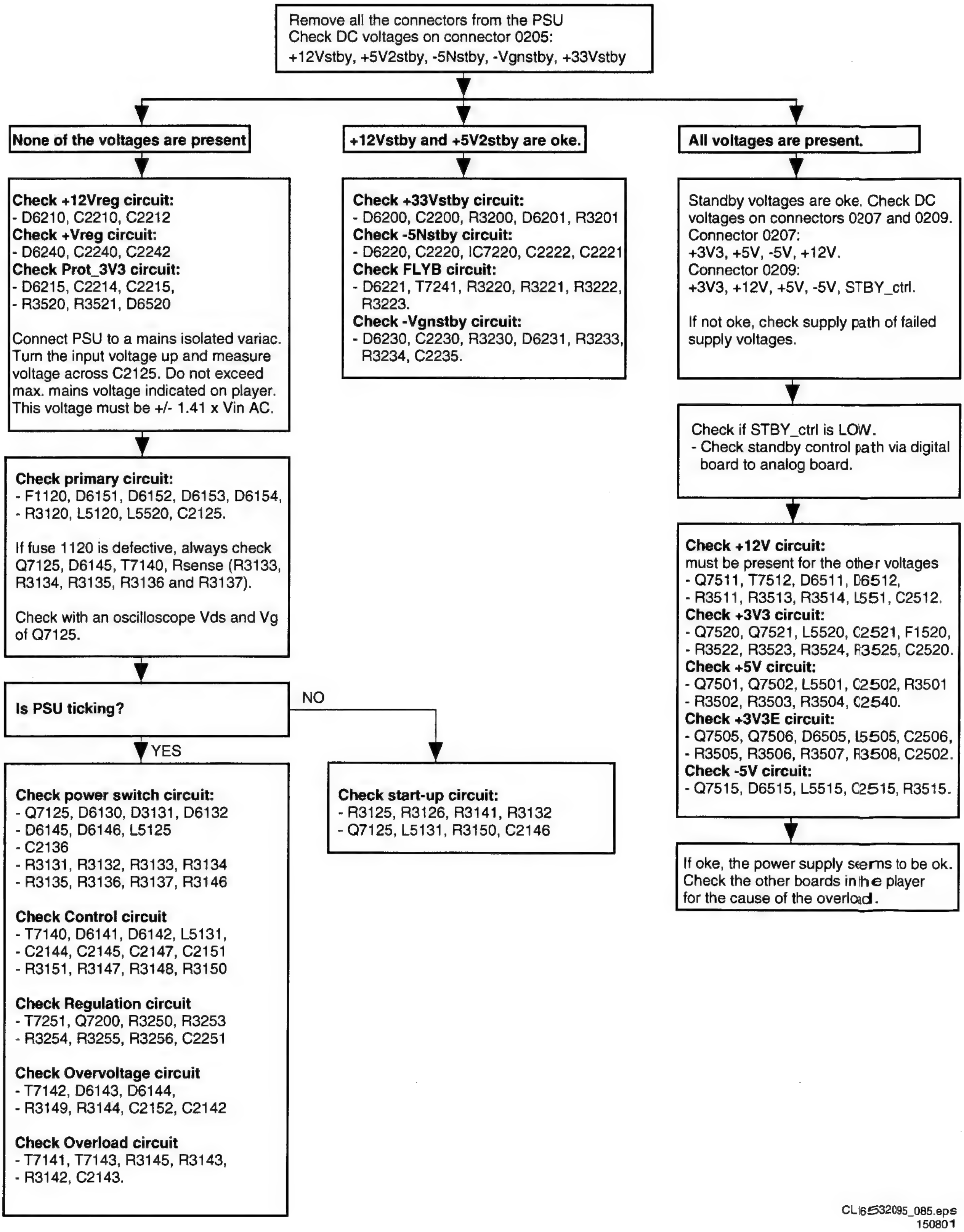
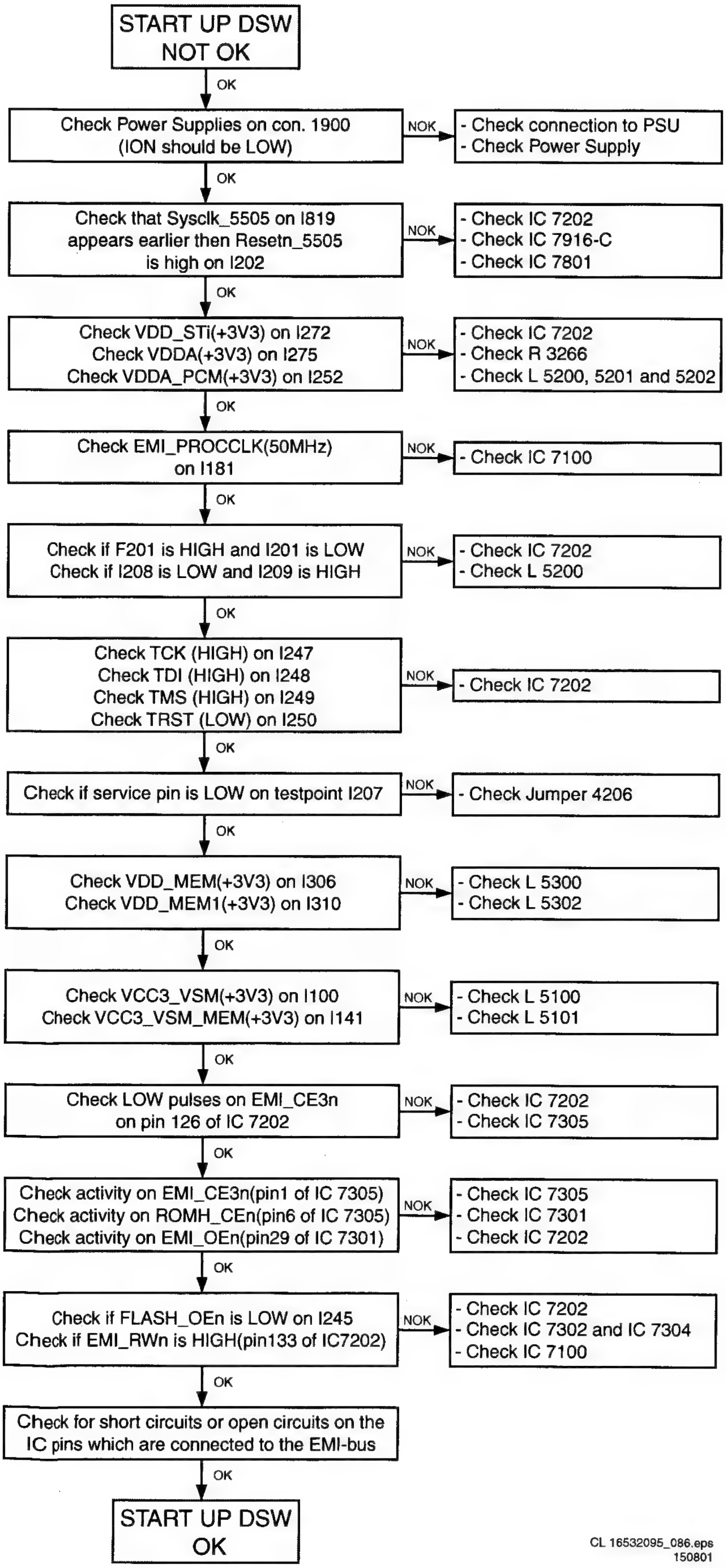


Figure 5-19

5.6.3 Digital Board

Start-Up DSW



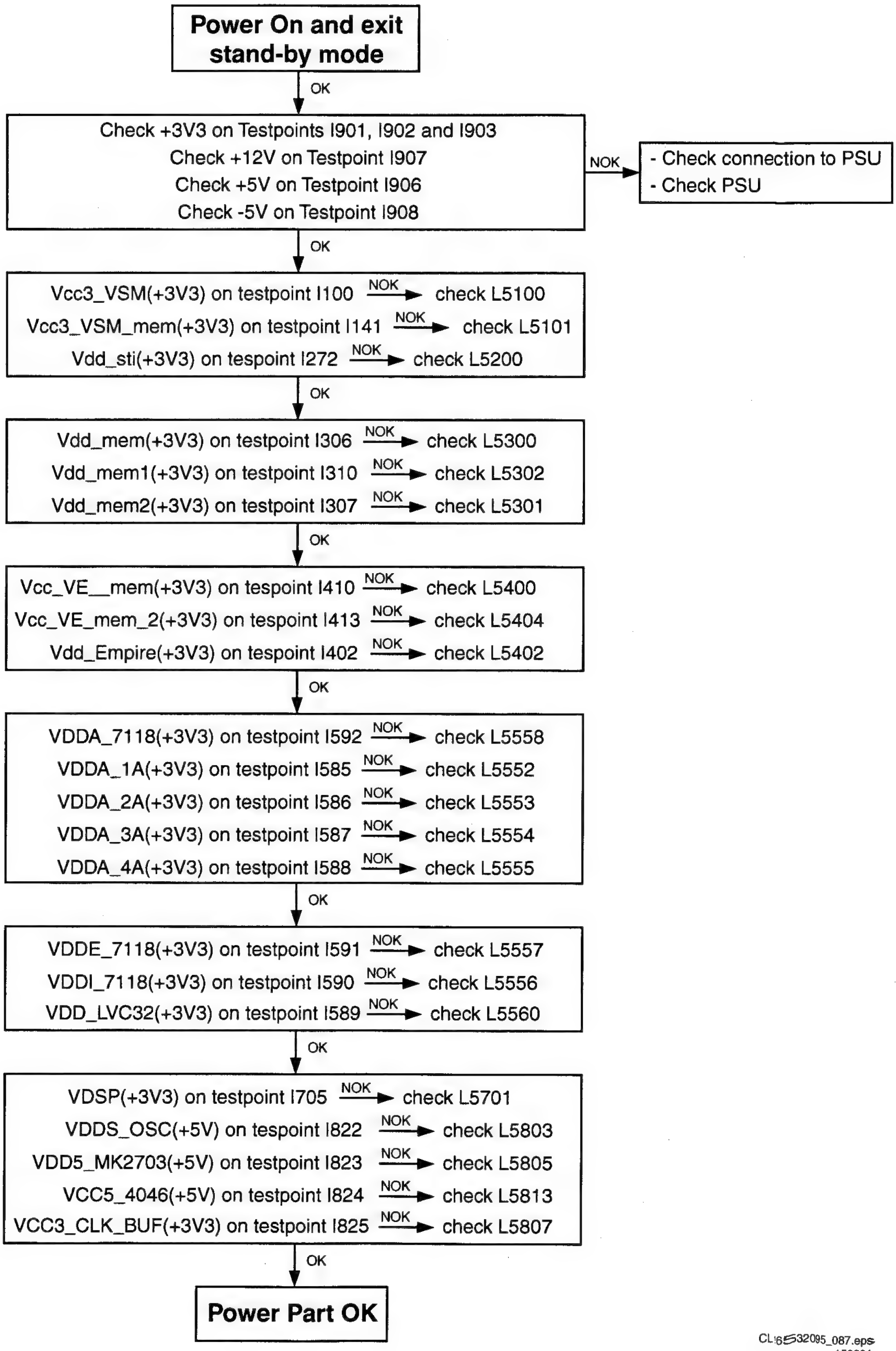
CL 16532095_086.eps
150801

Figure 5-20

Power Part Check

POWER PART CHECK DIGITAL BOARD

USE DIGITAL BOARD CIRCUIT DIAGRAMS 1 2, 3, 4, 5, 7 AND 8 AND DIGITAL BOARD BOTTOM VIEW TESTPOINTS



CL 16532095_087.eps
150801

Figure 5-21

Reset and Clock Check

RESET & CLOCK CHECK DIGITAL BOARD

USE DIGITAL BOARD CIRCUIT DIAGRAMS 1,2,7 AND 8 AND DIGITAL BOARD BOTTOM VIEW TESTPOINTS

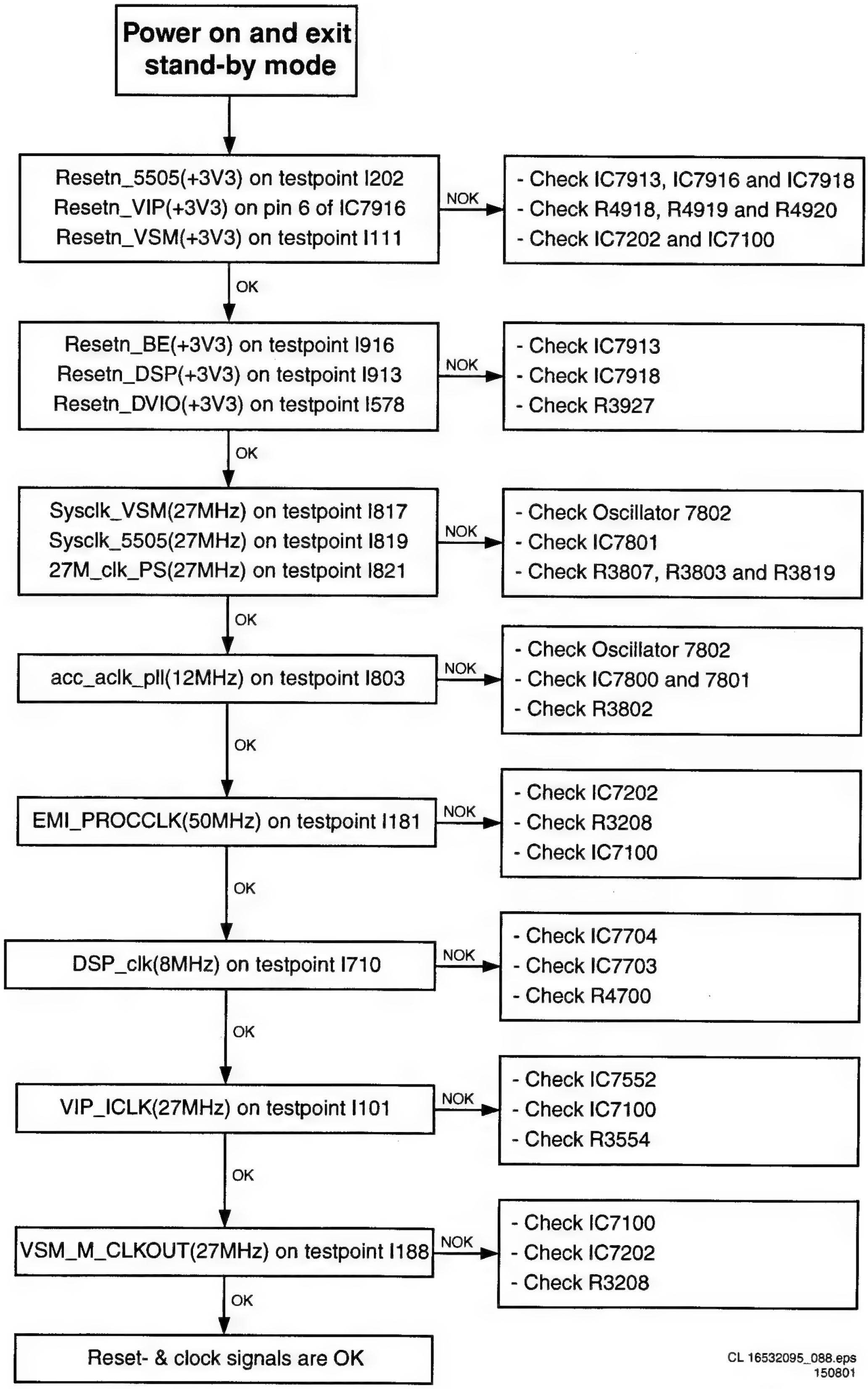


Figure 5-22

DSW Memory Tests

DSW MEMORY TESTS

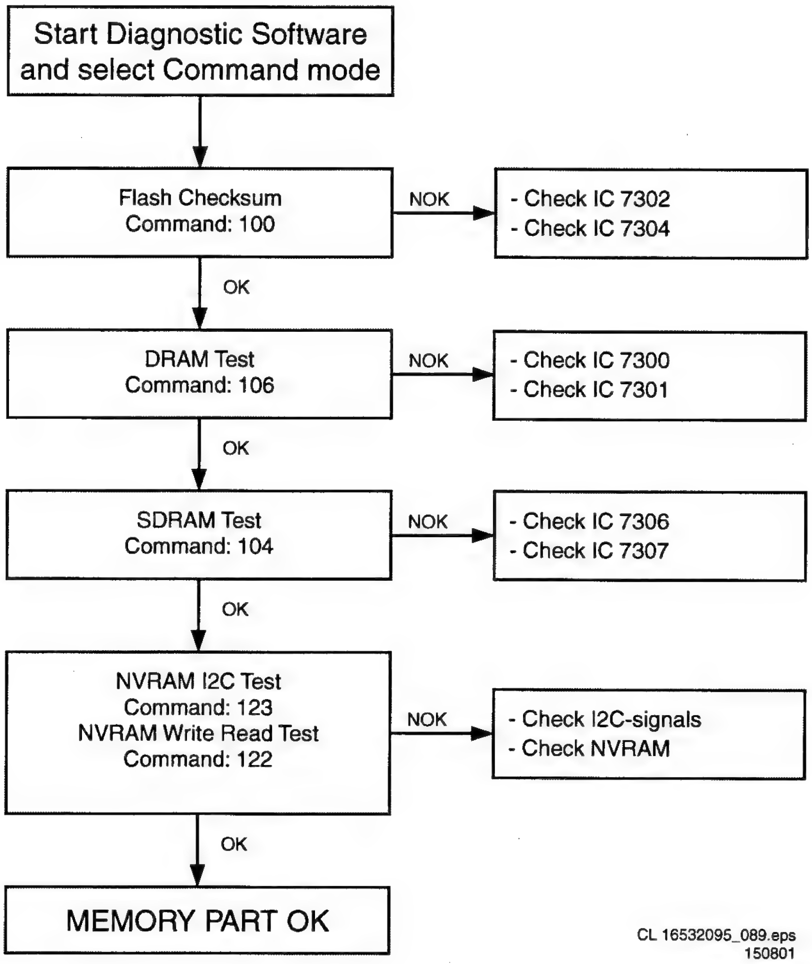


Figure 5-23

DSW VSM TESTS

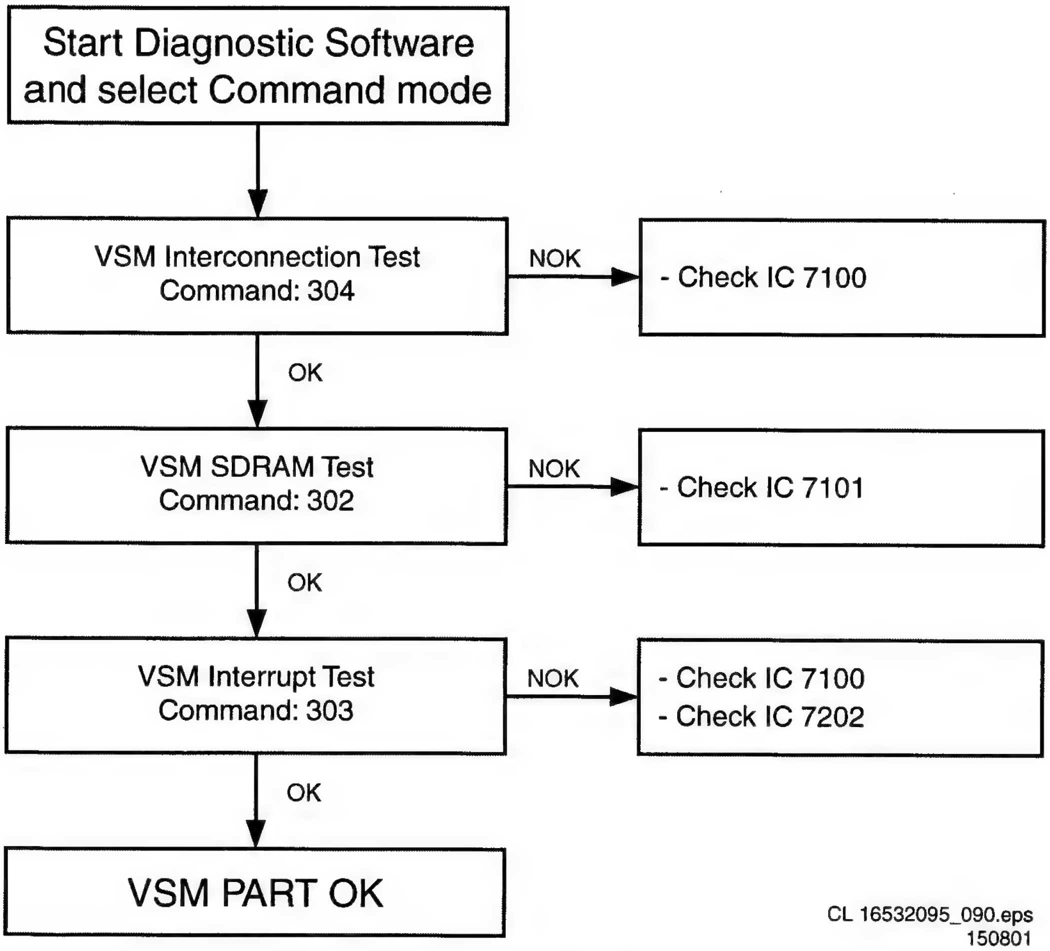


Figure 5-24

DSW Audio Video Encoder Tests

DSW AUDIO VIDEO ENCODER TESTS

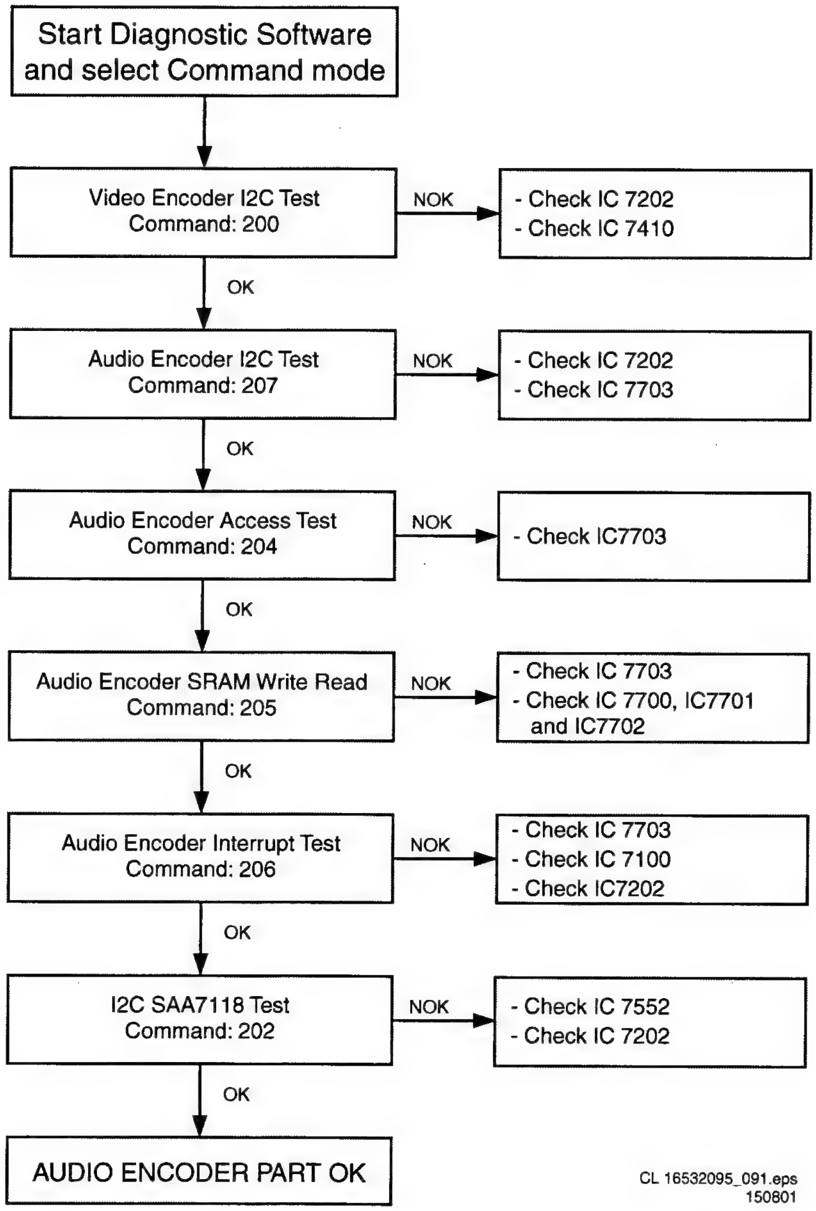


Figure 5-25

DSW Audio Part Check

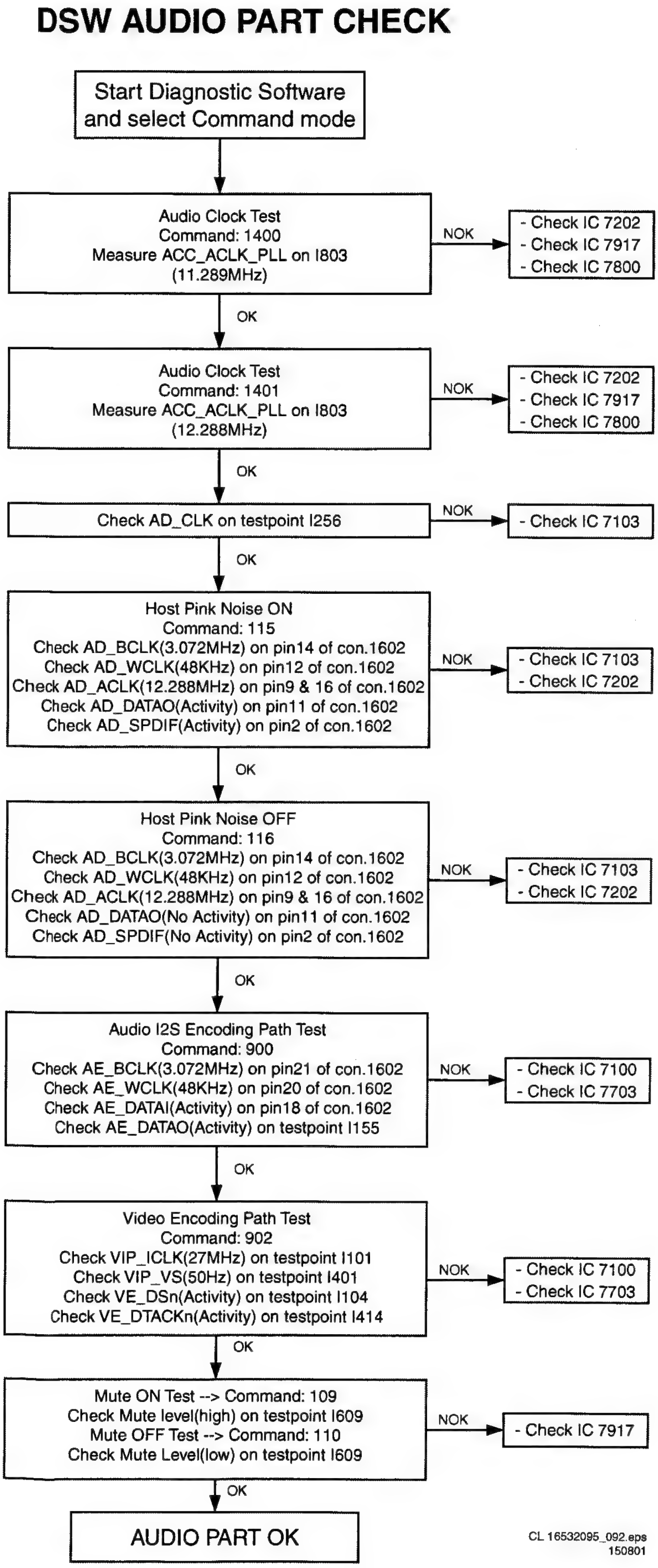
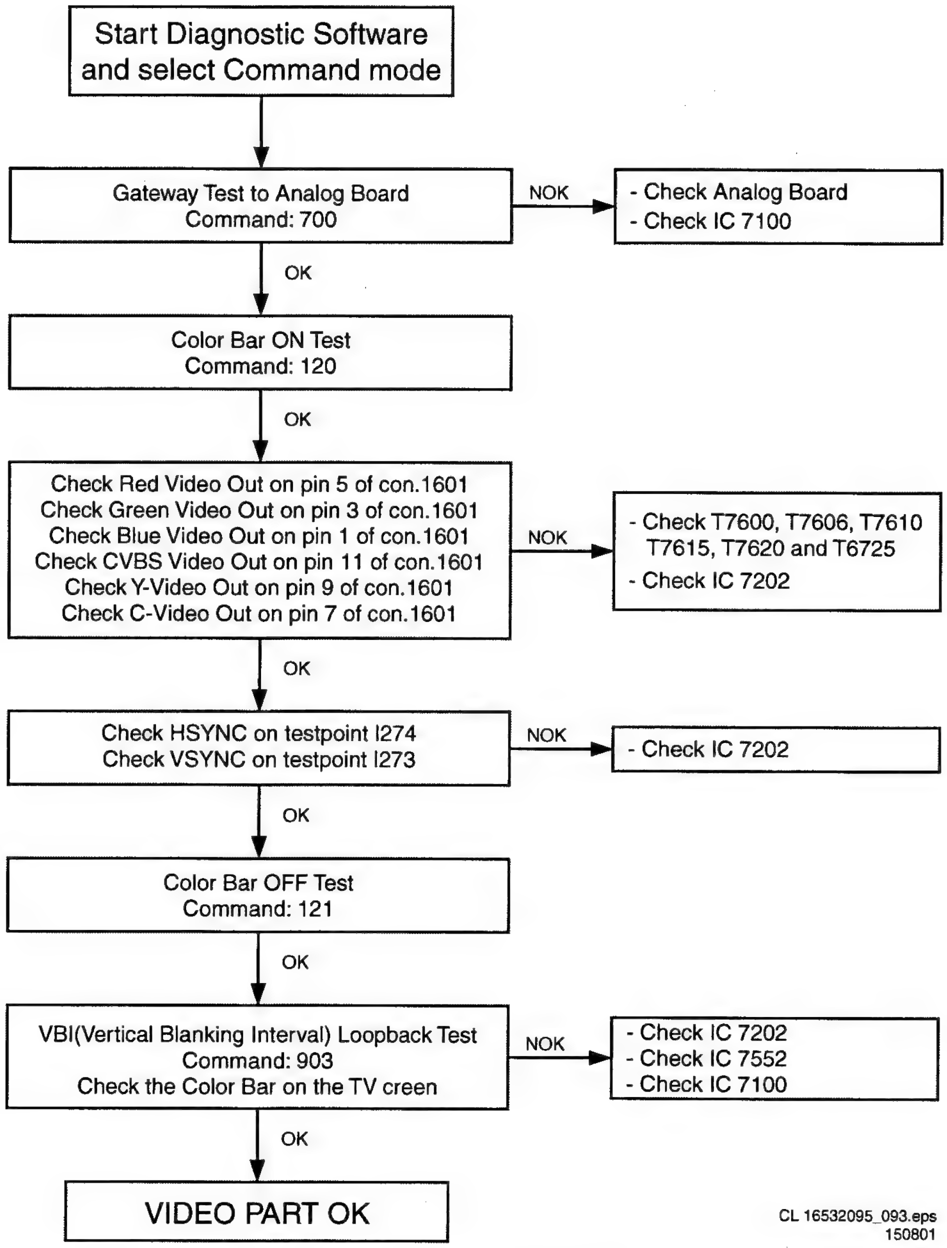


Figure 5-26

DSW Video Part Check

DSW VIDEO PART CHECK



CL 16532095_093.eps
150801

Figure 5-27

DSW Basic Engine Check

DSW BASIC ENGINE TESTS

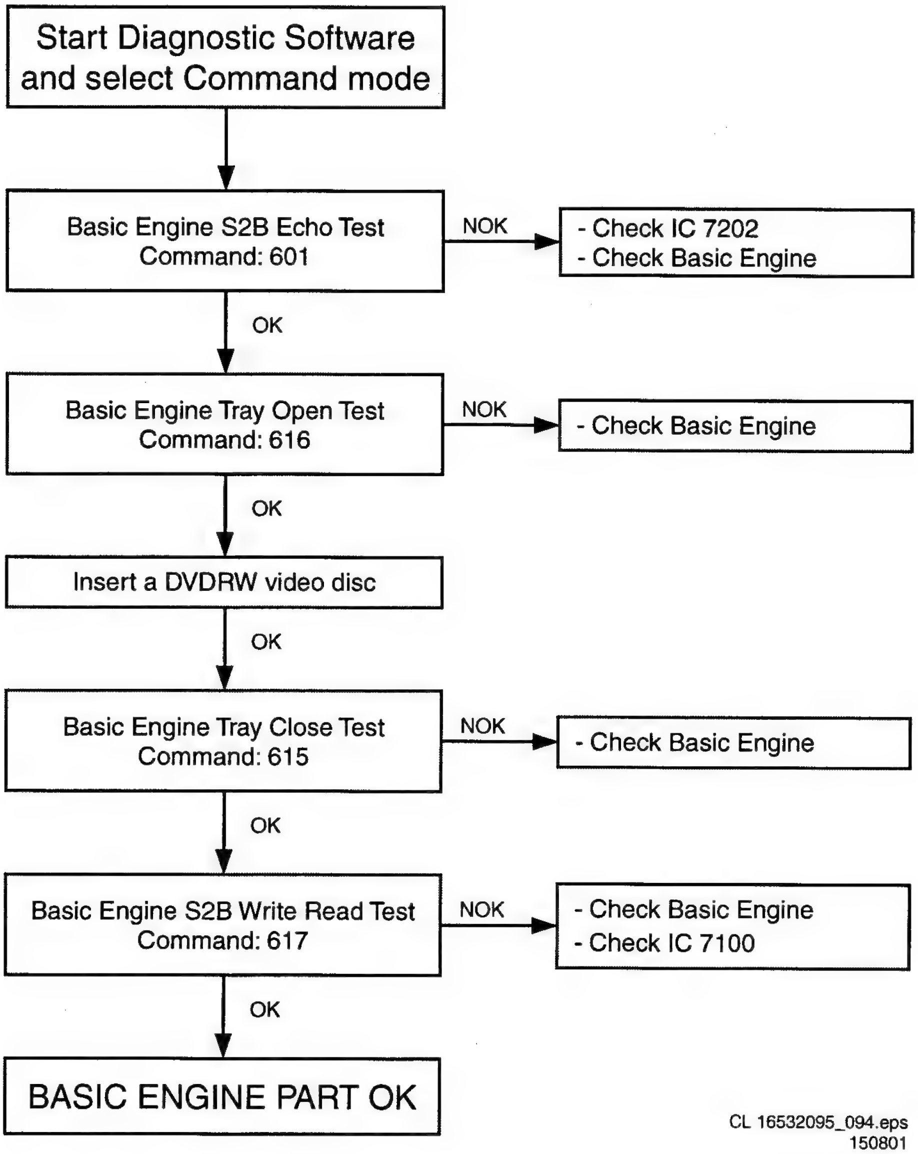


Figure 5-28

Waveforms

Waveforms Digital Board

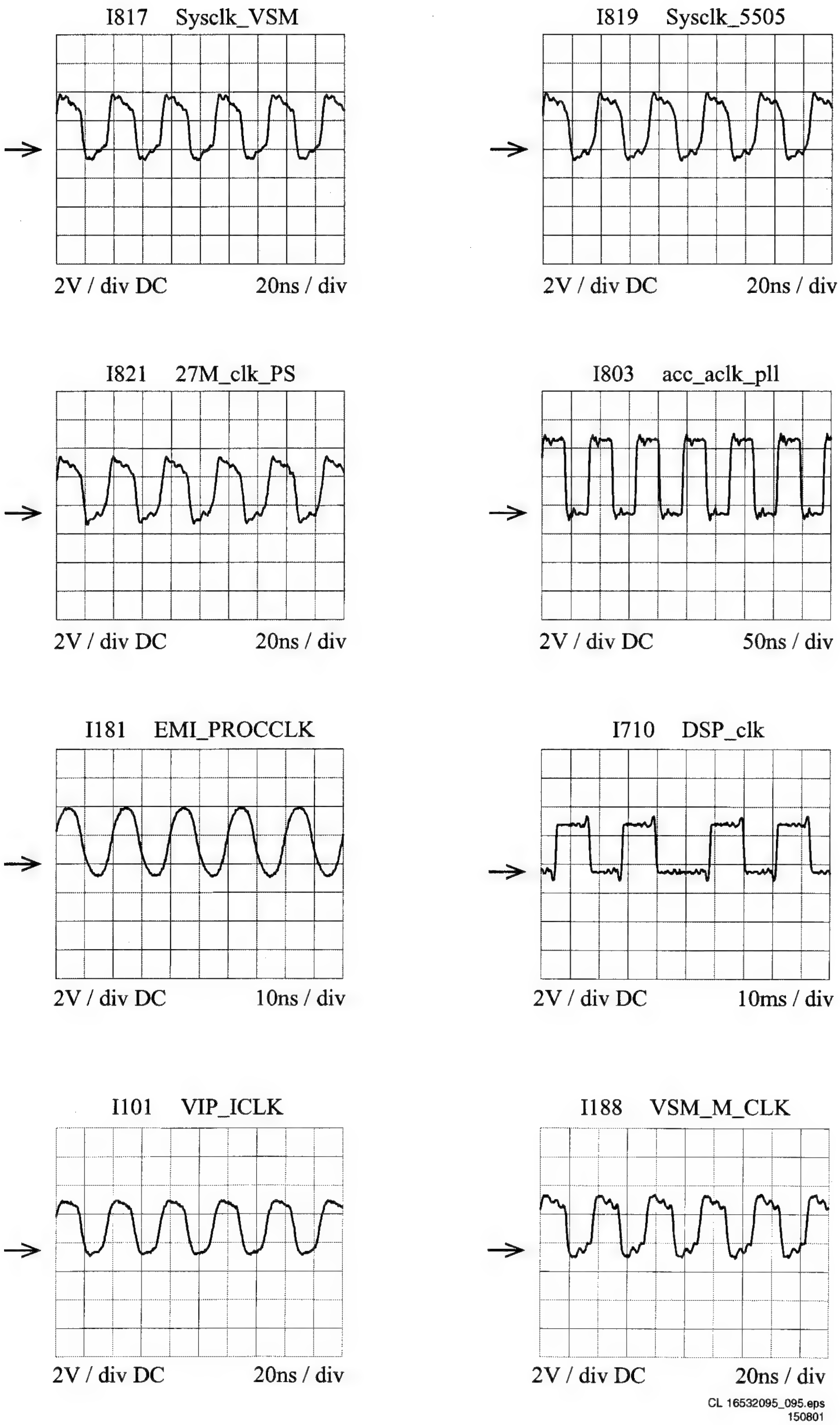


Figure 5-29

Waveforms Digital Board

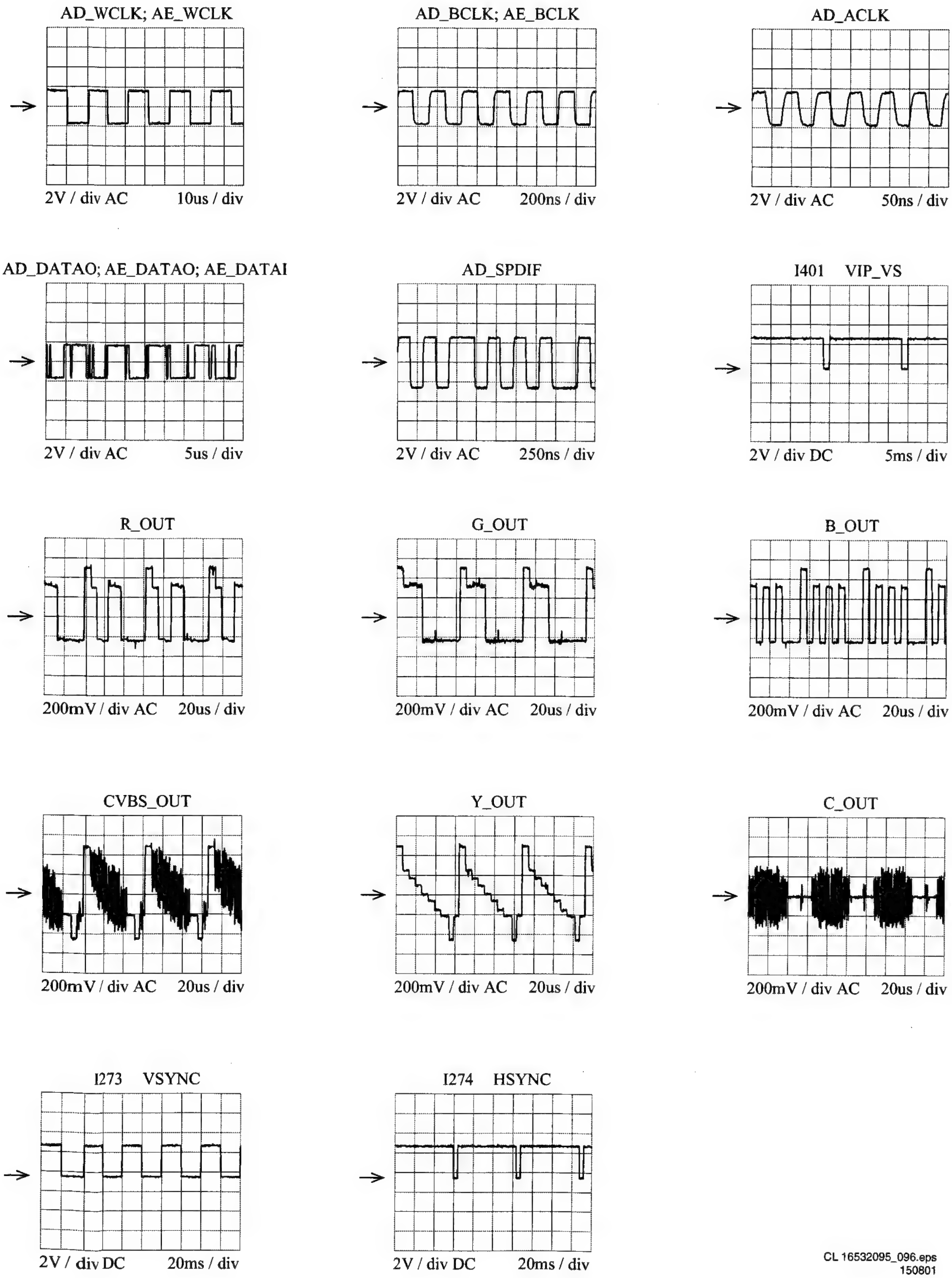


Figure 5-30

5.6.4 Analogue Board

Measurement Points Overview

Measurement Point Overview for EURO

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Schematics Coord.
F800			F_MODE	Fact. Mode	Condition	AIO1	AIO1	C10
F3201			12V	12 V Supply	PS IN	1932 1	PS	C1
F3202			5V	5 V Supply	PS IN	1932 2	PS	C1
F3203			5NSTBY	5 V Supply	PS IN	1932 3	PS	C1
F3204			VGNSTBY	Supply GND	PS IN	1932 4	PS	C1
F3205			33STBY	33 V Supply	PS IN	1932 5	PS	D1
F3206			FLYB	Controls PS	DC Gen	1932 6	PS	D1
F3207			GNDA	Ground Analogue	GND	1932 7	PS	D1
F0017			3VD	3V3 Supply	PS IN	1900 17	DAC	B1
F0001			GNDD	Ground Digital	GND	1900 01	DAC	E1
F803			INT Clock	Clock Adjust	Count Out	7811 7	AIO1	H5
F900			5STBY2	5V AIO	DC Out	7803 12	AIO2	D3
F902			IReset	Inverse Reset	DC Out *	7803 115	AIO2	D2
F8111			5M	5 V Motor	DC Out	1987 12	AIO1	F14
F303			5SW	5SW	DC Out	7703 21	TU	B10
F9336			8SW	8SW	DC Out	2321	PS	B6
F8105			SDA	IIC1	IIC IO	1981 6	AIO1	E13
F8107			SCL	IIC1	IIC IO	1981 8	AIO1	E13
F810			SCL1	IIC2	IIC IO	3804	AIO1	A9
F811			SDA1	IIC2	IIC IO	3805	AIO1	A9
F8104			IPOR1	IPOR to DC	DC OUT	1981 5	AIO1	E13
F8101			12STBY	12 V to DC	DC Out	1981 2	AIO1	D13
F8110			5STB	5 V to DC	DC Out	1981 11	AIO1	F13
F5306			8SW	8 SW to FRONT	DC Out	1953 6	IO1	I1
F8102			VGNSTBY	VGN to DC	GND	1981 3	AIO1	E13
F8202			A_DATA	To DIGI	DC IN	1982 2	AIO1	H13
F8203			D_DATA	To DIGI	DC IN	1982 3	AIO1	H13
F8204			A_RDY	To DIGI	DC IN	1982 4	AIO1	H13
F8205			D_RDY	To DIGI	DC IN	1982 5	AIO1	H13
F8108			INT	TO DC	DC IN	1981 9	AIO1	F13
F8109			RC	TO DC	DC IN	1981 10	AIO1	F13
F8201			IRESET_DIG	TO DIGI	DC IN	1982 1	AIO1	H13
F513			GNDA	SC1 GND A	DC IN	1950 4A	IO1	E14
F517			ARIn_SC1	SC1 A R IN	NF IN	1950 2A	IO1	E13
F519			ALIn_SC1	SC1 A L IN	NF IN	1950 6A	IO1	E14
F534			YCVBSIN_SC1	SC1 Y IN	V IN	1950 20A	IO1	I13
F525			GNDV	SC1 GND V	GND	1950 21A	IO1	H14
F5001			AROut_SC2	SC2 A R Out	NF Out	1950 1B	IO4	C9
F5003			ALOutSC2	SC2 A L Out	NF Out	1950 3B	IO4	C9
F5004			GNDA	SC2 GND A	GND	1950 4B	IO4	C9
F5019			YCVBSOut_SC2	SC2 Y Out	V Out	1950 19B	IO4	C9
F5021			GNDV	SC2 GND V	GND	1950 21B	IO4	C9
F019			AROut_SC1	SC1 A R Out	NF Out	1950 1A	IO1	E14
F518			ALOutSC1	SC1 A L Out	NF Out	1950 3A	IO1	E14
F531			YCVBSOut_SC1	SC1 Y Out	V Out	1950 19A	IO1	G13

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Schematics Coord.
F5002			ARIn_SC2	SC2 A R IN	NF IN	1950 2B	IO4	C9
F5006			ALIn_SC2	SC2 A L IN	NF IN	1950 6B	IO4	C9
F5020			YCVBSIN_SC2	SC2 Y IN	Sin IN	1950 20B	IO4	F9
F536			BC_SC1	SC1 BC	Sin Out*	1950 7A	IO1	E13
F521			8_SC1	SC1 Pin 8	DC Out	1950 8A	IO1	F13
F515			P50_SC1	SC1 P50	DC Out	1950 10A	IO1	F14
F524			Gout_SC1	SC1 G Out	Sin Out	1950 11A	IO1	F13
F527			RCOut_SC1	SC1 RC Out	Sin Out	1950 15A	IO1	G14
F530			FBOut_SC1	SC1 FB Out	DC Out	1950 16A	IO1	H13
F5007			BC_SC2	SC2 B IN C Out	Sin In*	1950 7B	IO4	D9
F5008			8_SC2	SC2 Pin 8	DC Out	1950 8B	IO4	D9
F5011			Gin_SC2	SC2 G In	Sin In	1950 11B	IO4	D9
F5015			RCin_SC2	SC2 RC In	Sin In	1950 15B	IO4	E9
F5016			FBin_SC2	SC2 FB In	DC In	1950 16B	IO4	E9
F5401			A_V	A_V to DIGI	Sin Out	1954 01	IO1	I3
F5402			GNDV	GNDV to DIGI	GND	1954 02	IO1	I4
F5403			A_U	A_U to DIGI	Sin Out	1954 03	IO1	I4
F5405			A_Y	A_Y to DIGI	V Out	1954 05	IO1	I4
F5407			A_C	A_C to DIGI	Sin Out	1954 07	IO1	I4
F5409			A_YCVBS	AYCVBS to DIGI	V Out	1954 09	IO1	I4
F5412			D_CVBS	D_CVBS f. DIGI	V In	1954 12	IO1	I5
F5414			D_Y	D_Y f. DIGI	V In	1954 14	IO1	I5
F5416			D_C	D_C f. DIGI	Sin In	1954 16	IO1	I5
F5418			D_R	D_T f. DIGI	Sin In	1954 18	IO1	I6
F5420			D_G	D_G f. DIGI	Sin In	1954 20	IO1	I6
F5422			D_B	D_B f. DIGI	Sin In	1954 22	IO1	I6
F5301			AFCRI	A R from FC	NF In	1953 1	IO1	I1
F5303			AFCLI	A L from FC	NF In	1953 3	IO1	I1
F5304			CVBSFIN	CVBS from FC	V In	1953 4	IO1	I1
F5307			CFIN	C from FC	Sin In	1953 7	IO1	I2
F5309			YFIN	Y from FC	V In	1953 9	IO1	I2
F012			DAINOPT	A D Opt to DIGI		1900 20	DAC	A1
F013			DAINCOAX	A D Coax to DIGI		1900 21	DAC	A1
F014			DAOUT	A D from DIGI		1900 20	DAC	A1
F0002			A_BCLK	BCLK from DIGI	CLK In	1900 2	DAC	E2
F0003			A_WCLK	WCLK from DIGI	CLK In	1900 3	DAC	D2
F0005			A_DAT	A Data to DIGI	Data Out	1900 5	DAC	D2
F0007			A_PCMCLK	PCMCLK from DIGI	CLK In	1900 7	DAC	D2
F0009			D_BCLK	BCLK from DIGI	CLK In	1900 9	DAC	D2
F0011			D_WCLK	WCLK from DIGI	CLK In	1900 11	DAC	D2
F0012			D_DATA0	A Data from DIGI	Data In	1900 12	DAC	C2
F0014			D_PCMCLK	PCMCLK from DIGI	CLK In	1900 14	DAC	C2
F0016			D_KILL	A Kill from DIGI	DC In	1900 16	DAC	C2
F010			ARDAC	A R from DAC	NF Out	7002 1	DAC	C9
F011			ALDAC	A L from DAC	NF Out	7002 7	DAC	E9
F331			RCALOut	A L Rear Cinch Out	NF Out	1958 4B	IO3	E9
F334			RCAROut	A R Rear Cinch Out	NF Out	1958 5B	IO3	E9
F336			RCVBSOut	V Rear Cinch Out	V Out	1959 1B	IO3	C9

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Figure 5-31

Measurement Point Overview for NAFTA

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Schematics Coord.
F5101			ARCRI	A L Rear Cinch In	NF In	1958 1A	IO2	D2
F5103			ARCLI	A R Rear Cinch In	NF In	1958 2A	IO2	E2
F5202			RCVBSIn	V Rear Cinch In	V In	1959 2A	IO2	C2
F5503			RSVHSYIn	Y Rear SVHS In	V In	1955 3B	IO2	B2
F5504			RSVHSCIn	C Rear SVHS In	Sin In	1955 4B	IO2	B2
F338			RSVHSYOut	Y Rear SVHS Out	V Out	1955 3A	IO3	A9
F337			RSVHSCOut	C Rear SVHS Out	Sin Out	1955 4A	IO3	A9
F6001			DVAR	A R from DIGI	Sin In	1960 1	AP	D1
F6002			GNDA	GNDA	GND	1960 2	AP	D1
F6004			DVAL	A L from DIGI	Sin In	1960 4	AP	D1
F700			IF	IF Out	DC Out	1705 11	TU	C3
F701			IF In	IF In	Sin In	1705 11	TU	C3
F702			GNDFV	GND FV	GND	1705 12	TU	C2
F703			GNDFV	GND FV	GND	1700 3	TU	B6
F704			40.4	40.4 Trap	Sin Out	1700 1	TU	B5
F705			AGC	AGC	DC Out	3701	TU	A4
F812			SYNC	SYNC from Sepa.	Freq Out	7803 33	AIO1	F6
F4202			DIG OUT L	Digital Out Low	GND	1954 2	DIGI	B4
F4203			DIG OUT H	Digital Out High	Sin Out	1945 3	DIGI	A4
F4204			OPT OUT	Optical Out	DC Out	1943 1	DIGI	D3
F806			FAN OUT	FAN Out	DC Out	1984 1	FACO	C5
F807			FAN IN	FAN In	DC In	1985 1	FACO	F1
F8206			ION	ION_FAN	DC Out	1982 6	AIO1	H13
F8208			BE_FAN	BE_FAN	DC Out	1982 8	AIO1	I13
F8209			FB	FBIN SC2	DC Out	1982 9	AIO1	I13
F8210			GNDD	GNDD	GNDD	1982 10	AIO1	I13

Remark:
Indicator * means more than one signal type

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Schematics Coord.
F800			F_MODE	Fact. Mode	Condition	AIO1	AIO1	C10
F3201			12V	12 V Supply	PS IN	1932 1	PS	C1
F3202			5V	5 V Supply	PS IN	1932 2	PS	C1
F3203			5NSTBY	5 V Supply	PS IN	1932 3	PS	C1
F3204			VGNSTBY	Supply GND	PS IN	1932 4	PS	C1
F3205			33STBY	33 V Supply	PS IN	1932 5	PS	D1
F3206			FLYB	Controls PS	DC Gen	1932 6	PS	D1
F3207			GNDA	Ground Analogue	GND	1932 7	PS	D1
F0017			3VD	3V3 Supply	PS IN	1900 17	DAC	B1
F0001			GNDD	Ground Digital	GND	1900 01	DAC	E1
F803			INT Clock	Clock Adjust	Count Out	7811 7	AIO1	H5
F900			5STBY2	5V AIO	DC Out	7803 12	AIO2	D3
F902			IReset	Inverse Reset	DC Out *	7803 115	AIO2	D2
F8111			5M	5 V Motor	DC Out	1987 12	AIO1	F14
F303			5SW	5SW	DC Out	7703 21	TU	B10
F9336			8SW	8SW	DC Out	2321	PS	B6
F8105			SDA	IIC1	IIC IO	1981 6	AIO1	E13
F8107			SCL	IIC1	IIC IO	1981 8	AIO1	E13
F810			SCL1	IIC2	IIC IO	3804	AIO1	A9
F811			SDA1	IIC2	IIC IO	3805	AIO1	A9
F8104			IPOR1	IPOR to DC	DC OUT	1981 5	AIO1	E13
F8101			12STBY	12 V to DC	DC Out	1981 2	AIO1	D13
F8110			5STB	5 V to DC	DC Out	1981 11	AIO1	F13
F5306			8SW	8 SW to FRONT	DC Out	1953 6	IO1	I1
F8102			VGNSTBY	VGN to DC	GND	1981 3	AIO1	E13
F8202			A_DATA	To DIGI	DC_In	1982 2	AIO1	H13
F8203			D_DATA	To DIGI	DC_In	1982 3	AIO1	H13
F8204			A_RDY	To DIGI	DC_In	1982 4	AIO1	H13
F8205			D_RDY	To DIGI	DC_In	1982 5	AIO1	H13
F8108			INT	TO DC	DC_In	1981 9	AIO1	F13
F8109			RC	TO DC	DC_In	1981 10	AIO1	F13
F8201			IRESET_DIG	TO DIGI	DC_In	1982 1	AIO1	H13
F5103			ARIn_2	A R IN 2	NF IN	1958 3A	IO3	E13
F5101			ALIn_2	A L IN 2	NF IN	1958 1A	IO3	E14
F5906			GNDV	GND V	GND	1957 6A	IO1	H12
F5806			GNDV	GND V	GND	1956 6A	IO1	I8
F510			ARout_1	A R Out 1	NF Out	1959 5B	IO1	E13
F509			ALout_1	A L Out 1	NF Out	1959 4B	IO1	D13
F5201			RCVBSOut2	SC1 Y Out	V Out	1997 1B	IO3	A8
F5105			ARIn_1	A R IN 1	NF IN	1959 1A	IO2	E2
F5104			ALIn_1	A L IN 1	NF IN	1959 4A	IO2	E2
F5202			RCVBSIn	Y IN	Sin IN	1997 2A	IO2	C2
F5905			Y_OUT	Y Out	Sin Out*	1957 5A	IO1	I12
F5801			U_IN	U IN	Sin In*	1956 1B	IO1	I10
F5805			Y_IN	Y IN	Sin In	1956 5A	IO1	I9
F5802			V_IN	V IN	Sin In	1956 2B	IO1	I10

Figure 5-32

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MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Schematics Coord.
F5401			A_V	A_V to DIGI	Sin Out	1954 01	IO1	I3
F5402			GNDV	GNDV to DIGI	GND	1954 02	IO1	I4
F5403			A_U	A_U to DIGI	Sin Out	1954 03	IO1	I4
F5405			A_Y	A_Y to DIGI	V Out	1954 05	IO1	I4
F5407			A_C	A_C to DIGI	Sin Out	1954 07	IO1	I4
F5409			A_YCVBS	AYCVBS to DIGI	V Out	1954 09	IO1	I4
F5412			D_CVBS	D_CVBS f. DIGI	V In	1954 12	IO1	I5
F5414			D_Y	D_Y f. DIGI	V In	1954 14	IO1	I5
F5416			D_C	D_C f. DIGI	Sin In	1954 16	IO1	I5
F5418			D_R	D_T f. DIGI	Sin In	1954 18	IO1	I6
F5420			D_G	D_G f. DIGI	Sin In	1954 20	IO1	I6
F5422			D_B	D_B f. DIGI	Sin In	1954 22	IO1	I6
F5301			AFCRI	A R from FC	NF In	1953 1	IO1	I1
F5303			AFCLI	A L from FC	NF In	1953 3	IO1	I1
F5304			CVBSFIN	CVBS from FC	V In	1953 4	IO1	I1
F5307			CFIN	C from FC	Sin In	1953 7	IO1	I2
F5309			YFIN	Y from FC	V In	1953 9	IO1	I2
F012			DAINOPT	A D Opt to DIGI		1900 20	DAC	A1
F013			DAINCOAX	A D Coax to DIGI		1900 21	DAC	A1
F014			DAOUT	A D from DIGI		1900 20	DAC	A1
F0002			A_BCLK	BCLK from DIGI	CLK In	1900 2	DAC	E2
F0003			A_WCLK	WCLK from DIGI	CLK In	1900 3	DAC	D2
F0005			A_DAT	A Data to DIGI	Data Out	1900 5	DAC	D2
F0007			A_PCMCLK	PCMCLK from DIGI	CLK In	1900 7	DAC	D2
F0009			D_BCLK	BCLK from DIGI	CLK In	1900 9	DAC	D2
F0011			D_WCLK	WCLK from DIGI	CLK In	1900 11	DAC	D2
F0012			D_DATA0	A Data from DIGI	Data In	1900 12	DAC	C2
F0014			D_PCMCLK	PCMCLK from DIGI	CLK In	1900 14	DAC	C2
F0016			D_KILL	A Kill from DIGI	DC In	1900 16	DAC	C2
F010			ARDAC	A R from DAC	NF Out	7002 1	DAC	C9
F011			ALDAC	A L from DAC	NF Out	7002 7	DAC	E9
F513			ALOut_2	A L Rear Out 2	NF Out	1958 4B	IO1	B13
F512			AROut_2	A R Rear Out 2	NF Out	1958 5B	IO1	C13
F5205			RCVBSOut1	V Rear Cinch Out1	V Out	1997 5C	IO3	A8
F5503			RSVHSYIn	Y Rear SVHS In	V In	1955 3B	IO2	B2
F5504			RSVHSCIn	C Rear SVHS In	Sin In	1955 4B	IO2	B2
F338			RSVHSYOut	Y Rear SVHS Out	V Out	1955 3A	IO3	A9
F337			RSVHSCOut	C Rear SVHS Out	Sin Out	1955 4A	IO3	A9
F6001			DVAR	A R from DIGI	Sin In	1960 1	AP	D1
F6002			GNDA	GNDA	GND	1960 2	AP	D1
F6004			DVAL	A L from DIGI	Sin In	1960 4	AP	D1
F700			IF	IF Out	DC Out	1705 11	TU	C3
F701			IF In	IF In	Sin In	1705 11	TU	C3
F702			GNDFV	GND FV	GND	1705 12	TU	C2
F703			GNDFV	GND FV	GND	1700 3	TU	B6
F705			AGC	AGC	DC Out	3701	TU	A4
F812			SYNC	SYNC from Sepa.	Freq Out	7003 33	AIO1	F6
F330			RC IN	Remote Control In	DC Out	1993 2	IO3	E2

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Schematics Coord.
F4202			DIG OUT L	Digital Out Low	GND	1954 2	DIGI	B4
F4203			DIG OUT H	Digital Out High	Sin Out	1945 3	DIGI	A4
F4204			OPT OUT	Optical Out	DC Out	1943 1	DIGI	D3
F806			FAN OUT	FAN Out	DC Out	1984 1	FACO	C5
F807			FAN IN	FAN In	DC In	1985	FACO	F1
F8206			ION	ION_FAN	DC Out	1982 6	AIO1	H13
F8208			BE_FAN	BE_FAN	DC Out	1982 8	AIO1	I13
F8209			FB	FBIN SC2	DC Out	1982 9	AIO1	I13
F8210			GNDD	GNDD	GNDD	1982 10	AIO1	I13

Remark:
Indicator * means more than one signal type

Figure 5-33

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Power Part Check

RESET AND CLOCK CHECK ANALOG BOARD

Check internal Power supply voltages

5M on testpoint F9340	NOK →	check Fuse 1327
12STBY on testpoint F810	NOK →	check Fuse 1326
8STBY on pin 3 of IC7332	NOK →	check IC 7332
8SW on testpoint F9336	NOK →	check - ISTBY HIGH? - T7329, T7324, MOSFET7321
5STBY on testpoint F9333	NOK →	check Fuse 1325
5SW on testpoint F303	NOK →	check - ISTBY HIGH? - T7329, T7324, MOSFET7323
5STBY2 on testpoint F900	NOK →	check L5901, IC7900
5STBY_uP on IC7803	NOK →	check L5903, IC7803

↓ OK

Power Part OK

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Figure 5-34

DSW Check Analogue Board

DSW CHECK ANALOGUE BOARD

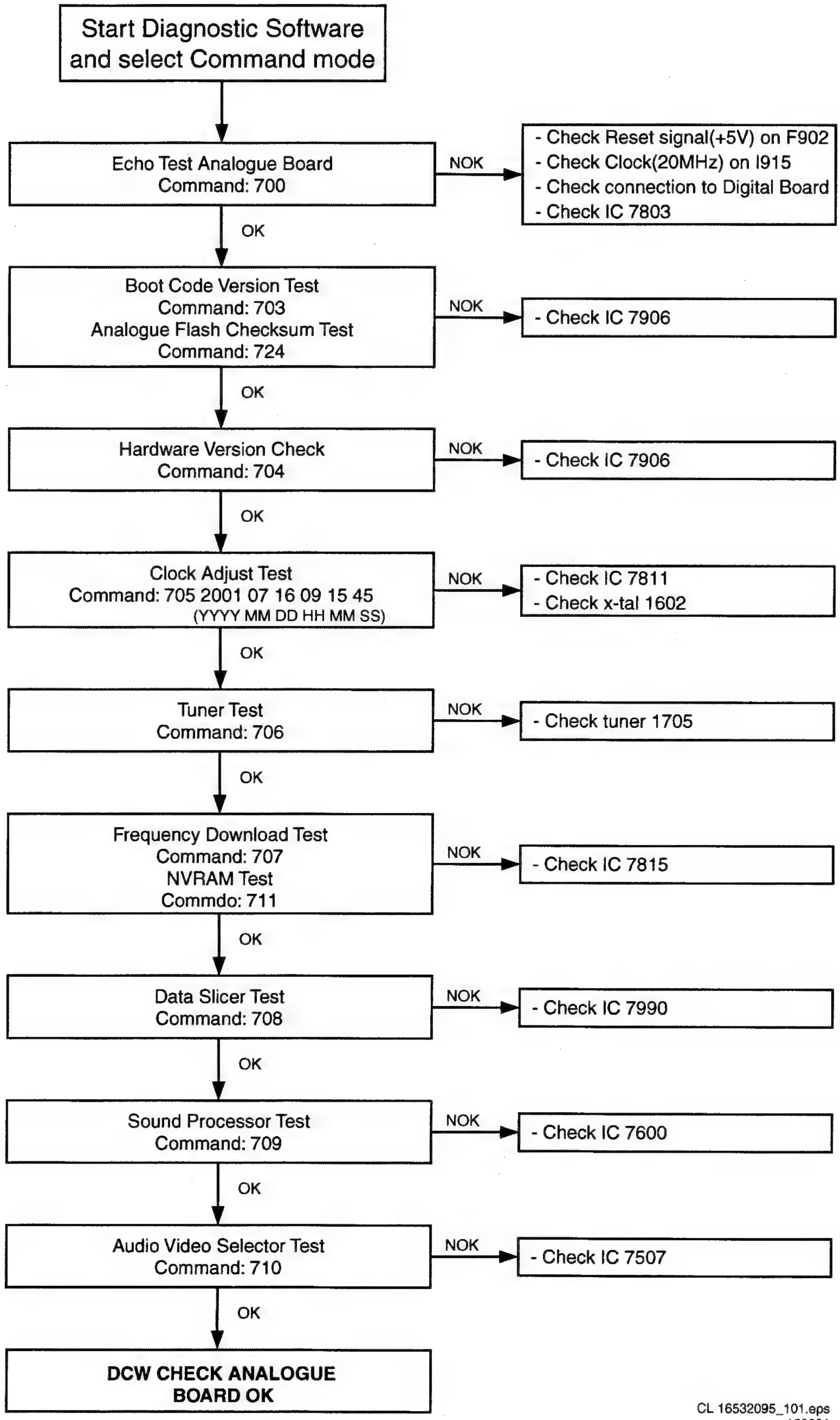

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Figure 5-35

Routing Audio and Video

Route Video
Nucleus Number: 712
Description

This nucleus routes the video signals on the analogue board to the destination determined by the input parameters
The paths that are available for video routing and their description(Europe version)

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
02	Input signal is from REAR VIDEO(CVBS) IN and will be routed to the digital board.
03	Input signal is from FRONT S-VIDEO(Y/C) and will be routed to the digital board.
04	Input signal is from REAR S-VIDEO(Y/C) and will be routed to the digital board.
05	Input signal is CVBS from SCART1 and will be routed to the digital board.
06	Input signal is CVBS from SCART2 and will be routed to the digital board.
07	No routing.
08	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to SCART1.
09	Input signal is VIDEO(CVBS) from SCART1 and will be routed to SCART2.
10	Input signal is VIDEO(CVBS) from SCART2 and will be routed to SCART1.
11	No routing.
12	Input signal is from REAR VIDEO(CVBS) IN and will be routed to SCART1 and SCART2.
13	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to SCART1.
14	Input signals VIDEO(CVBS and Y/C) from SCART 1 will be routed to SCART2.
15	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to SCART2.
16	Input signal is from FRONT S-VIDEO(Y/C) IN and will be routed to SCART2.
17	No routing
18	No routing
19	Input signals VIDEO(RGB and FAST BLANKING) from SCART2 will be routed to the corresponding pins of SCART1.

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The paths that are available for video routing and their description (Nafta region)

Path ID	Description
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
02	Input signal is from REAR VIDEO(CVBS) IN and will be routed to the digital board.
03	Input signal is from FRONT S-VIDEO(Y/C) IN and the signal received will be routed to the digital board.
04	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to the digital board.
05	Input signal is from YUV IN and will be routed to the digital board.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to VIDEO(CVBS) OUT and .
09	Input signal is from YUV IN and will be routed to YUV OUT.
10	No routing.
11	No routing.
12	Input signal is from REAR VIDEO(CVBS) IN and will be routed to REAR VIDEO(CVBS) OUT.
13	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to REAR VIDEO(CVBS) OUT.
14	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to REAR S-VIDEO(Y/C) OUT.
15	Input signal is from FRONT S-VIDEO(Y/C) IN and will be routed to REAR S-VIDEO(Y/C) OUT.

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Example
DD:> 712 01
71200: Video routing on the Analogue Board OK.

Test OK @

Route Audio
Nucleus Number: 713
Description
This nucleus routes the audio on the analogue board to the destination determined by the input parameters

The paths that are available for audio routing and their description (Europe version)

Path ID	Description
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
02	Input signal is from REAR AUDIO IN and will be routed to the digital board.
03	Input signal is AUDIO from SCART1 and will be routed to the digital board.
04	Input signal is AUDIO from SCART2 and will be routed to the digital board.
05	No routing.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) and AUDIO from ANTENNA IN and will be routed to SCART1.
09	Input signal is VIDEO(CVBS) and AUDIO from SCART1 and will be routed to SCART2.
10	Input signal is VIDEO(CVBS) and AUDIO from SCART2 and will be routed to SCART1.
11	Input signal is AUDIO from dvio board and will be routed to SCART1.
12	No routing.
13	No routing.
14	No routing.
15	No routing.
16	No routing.
17	Input signal is from REAR AUDIO IN and will be routed to SCART1.
18	Input signal is from FRONT AUDIO IN and will be routed to SCART1.

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140801

The paths that are available for audio routing and their description (Nafta region)

Path ID	Description
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
02	Input signal is from REAR AUDIO IN 1 and will be routed to the digital board.
03	Input signal is from REAR AUDIO IN 2 and will be routed to the digital board.
04	No routing.
05	No routing.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) and AUDIO from ANTENNA IN and will be routed to VIDEO(CVBS) OUT and REAR CINCH OUT 2.
09	No routing.
10	Input signal is from REAR AUDIO CINCH IN 1 and will be routed to REAR AUDIO CINCH OUT 2.
11	Input signal is from FRONT AUDIO CINCH IN and will be routed to REAR AUDIO CINCH OUT 2.
12	No routing.
13	No routing.
14	No routing.
15	No routing.
16	Input signal is AUDIO from dvio board and will be routed to AUDIO CINCH OUT 2.

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140801

EXAMPLE
DD:> 713 00
71300: Audio routing on the Analogue Board OK.
Test OK @

5.6.5 Display Board

TROUBLESHOOTING DISPLAY BOARD

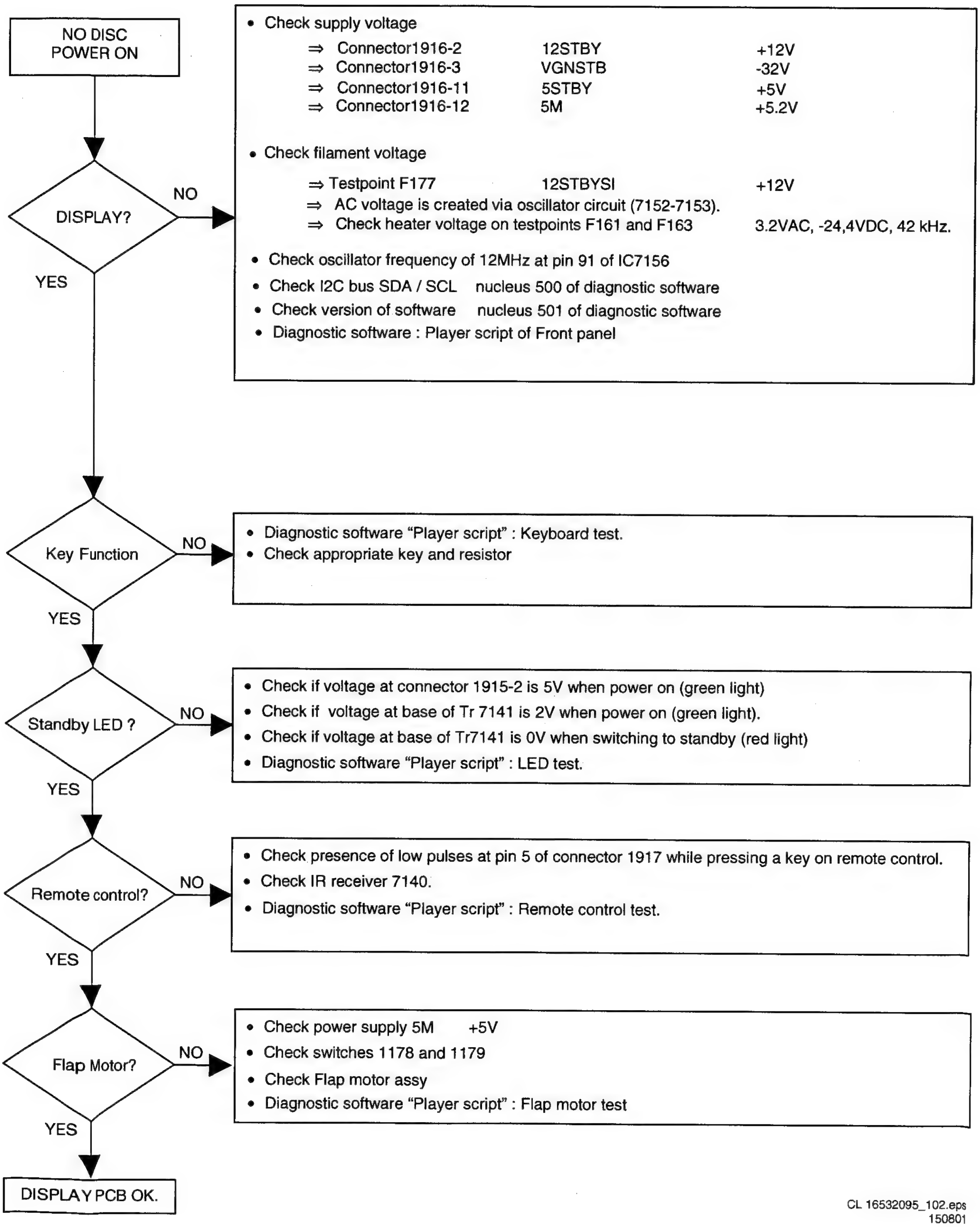

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Figure 5-36

5.6.6 DVIO Board

Power Part Check

POWER PART CHECK DVIO

USE DVIO BOARD CIRCUIT DIAGRAMS 1 2, 3, 4 AND 5 AND DVIO TOP VIEW TESTPOINTS

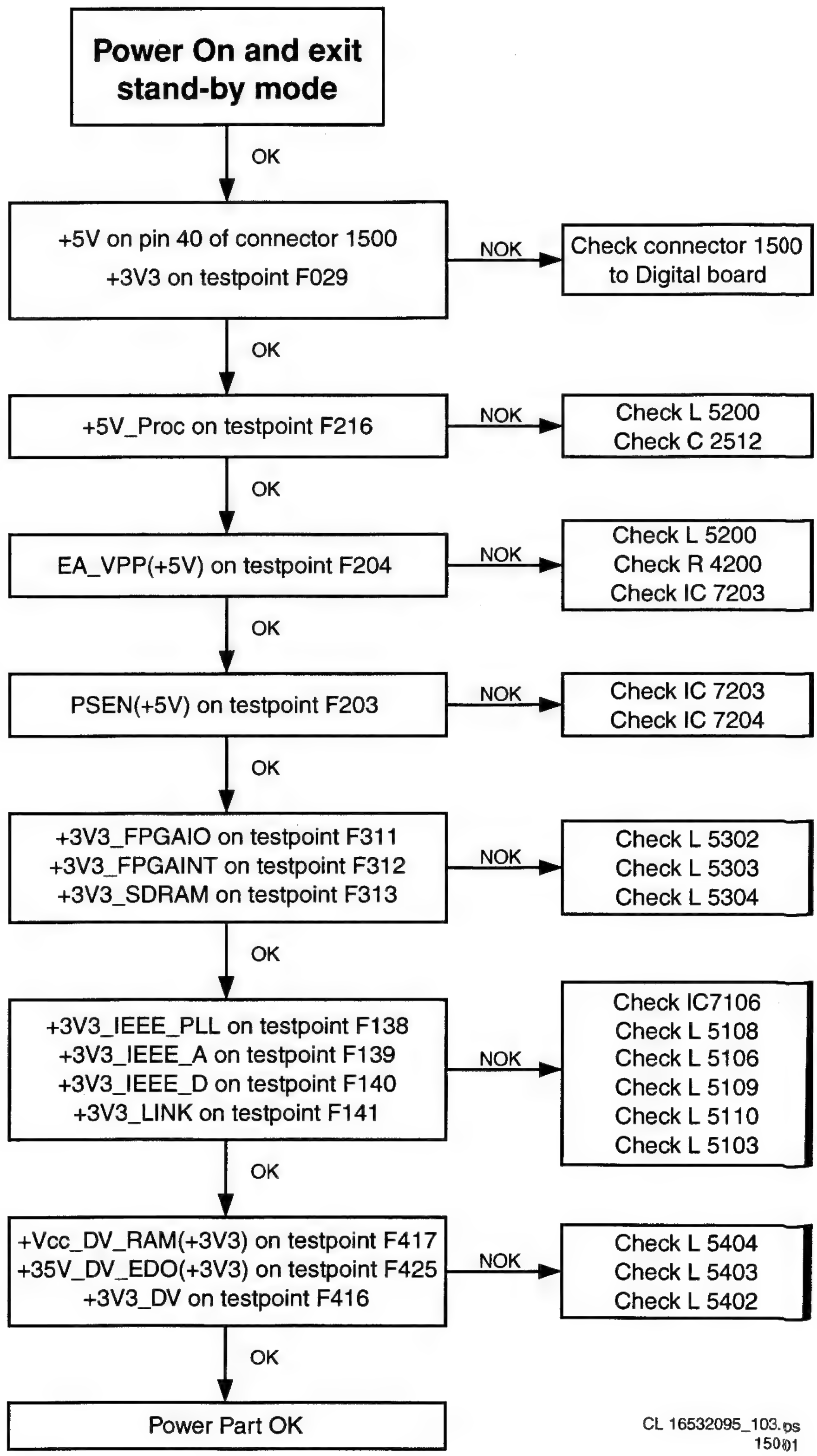


Figure 5-37

Reset and Clock Check

RESET & CLOCK CHECK DVIO

USE DVIO BOARD CIRCUIT DIAGRAMS 2, 3, 4 AND 5 AND DVIO TOP VIEW TESTPOINTS

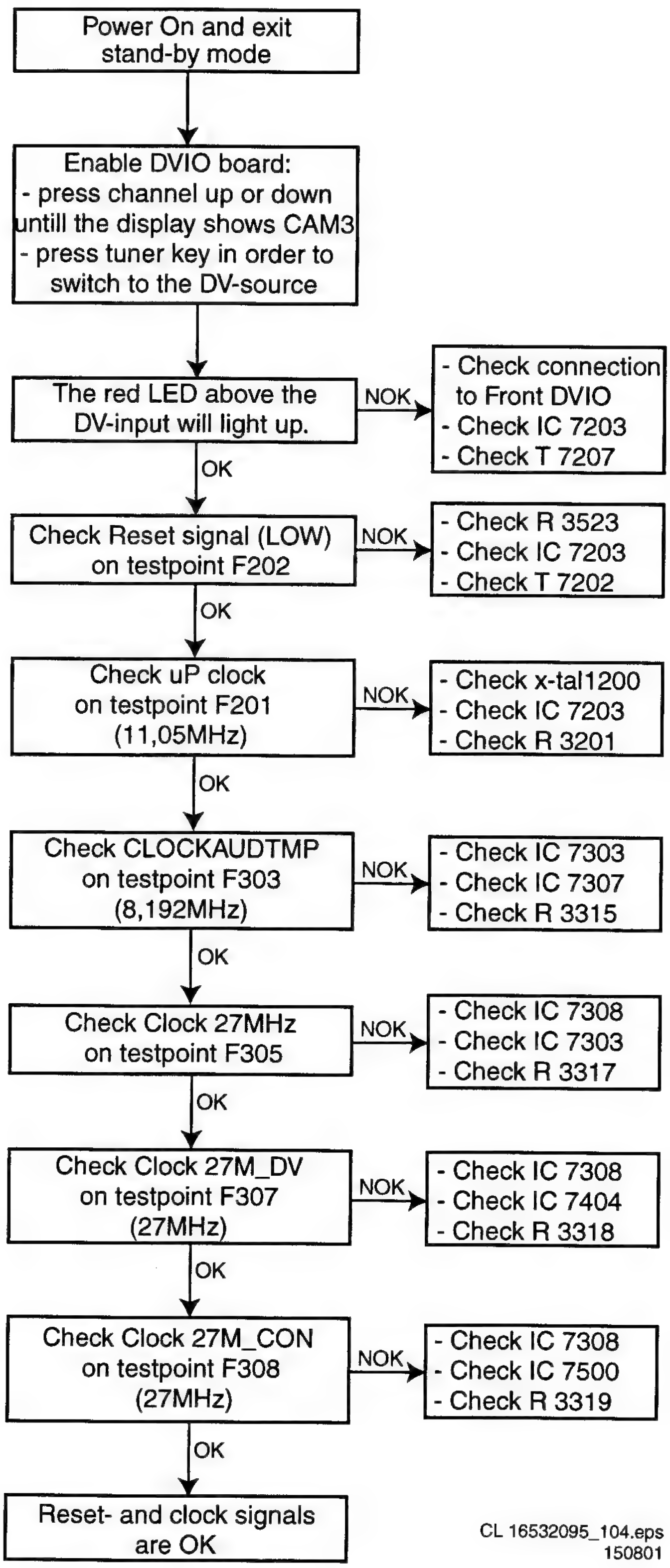
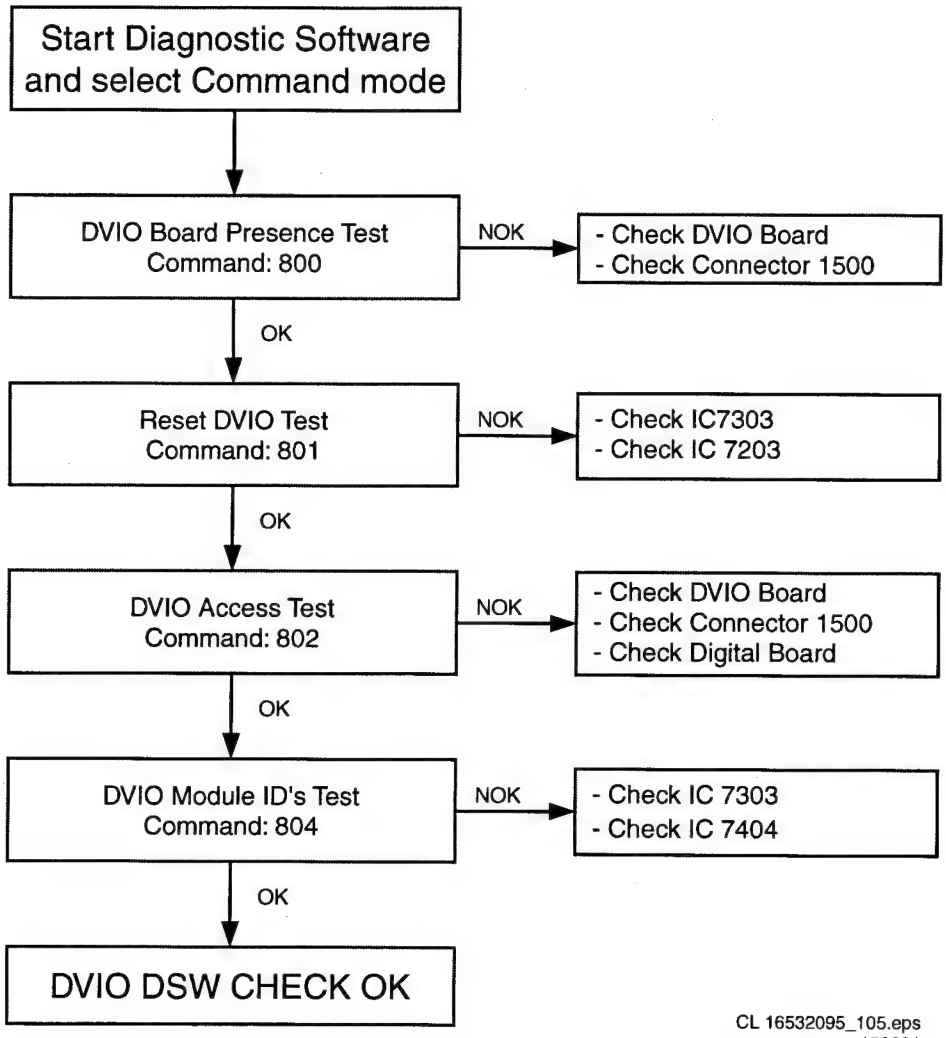


Figure 5-38

DSW DVIO Tests

DSW DVIO TESTS



CL 16532095_105.eps
150801

Figure 5-39

Functional Test

FUNCTIONAL TEST VIDEO PICTURE DVIO BOARD

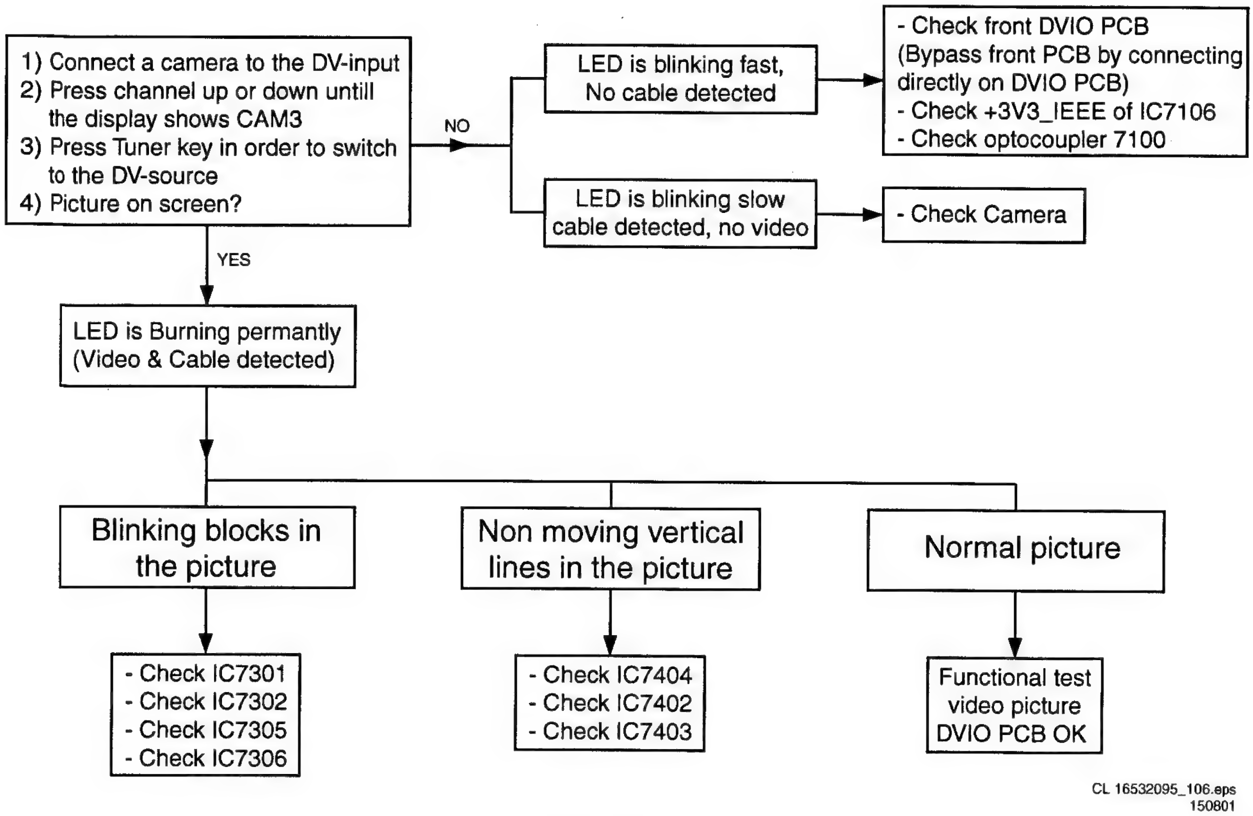


Figure 5-40

Waveforms

Waveforms DVIO

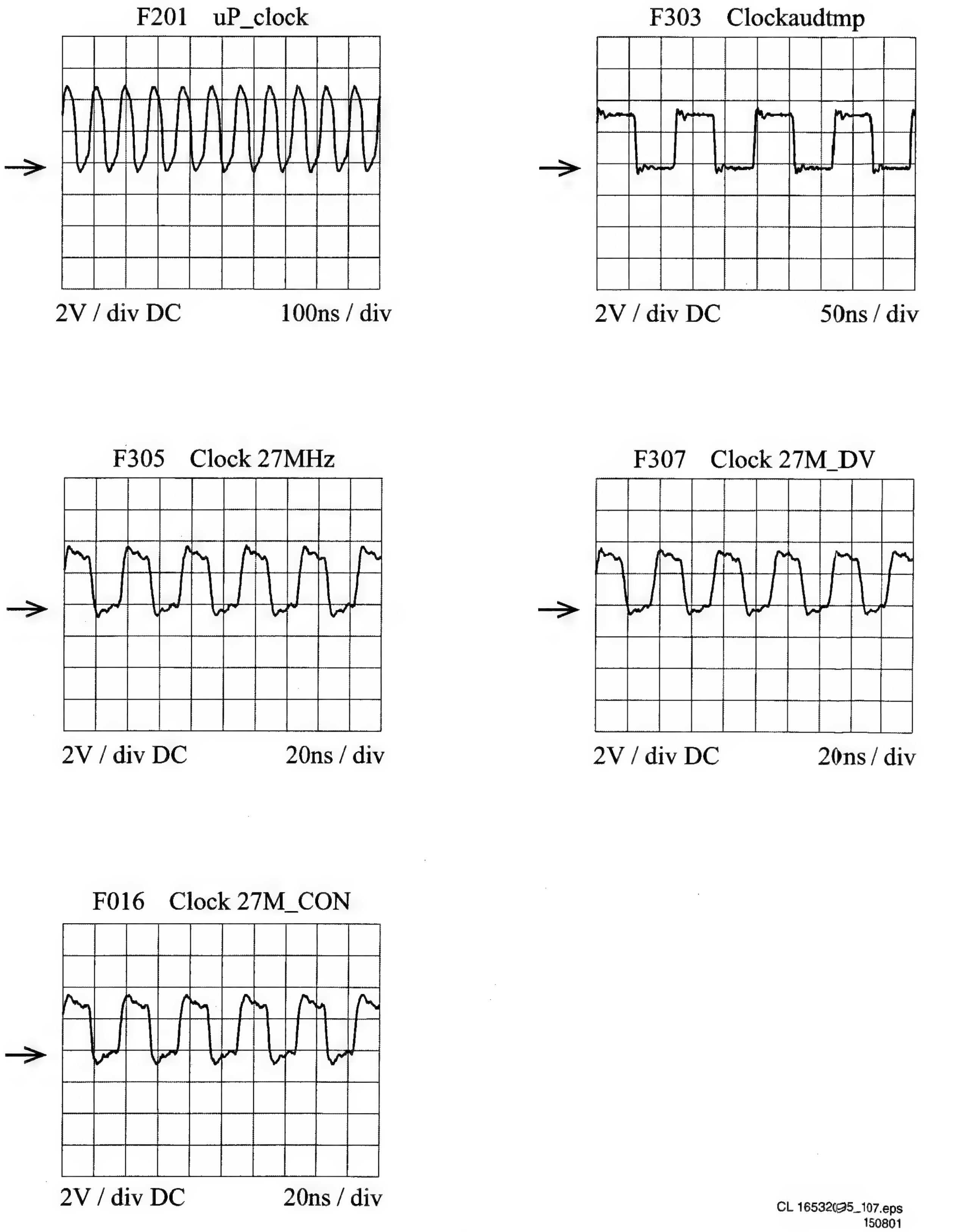
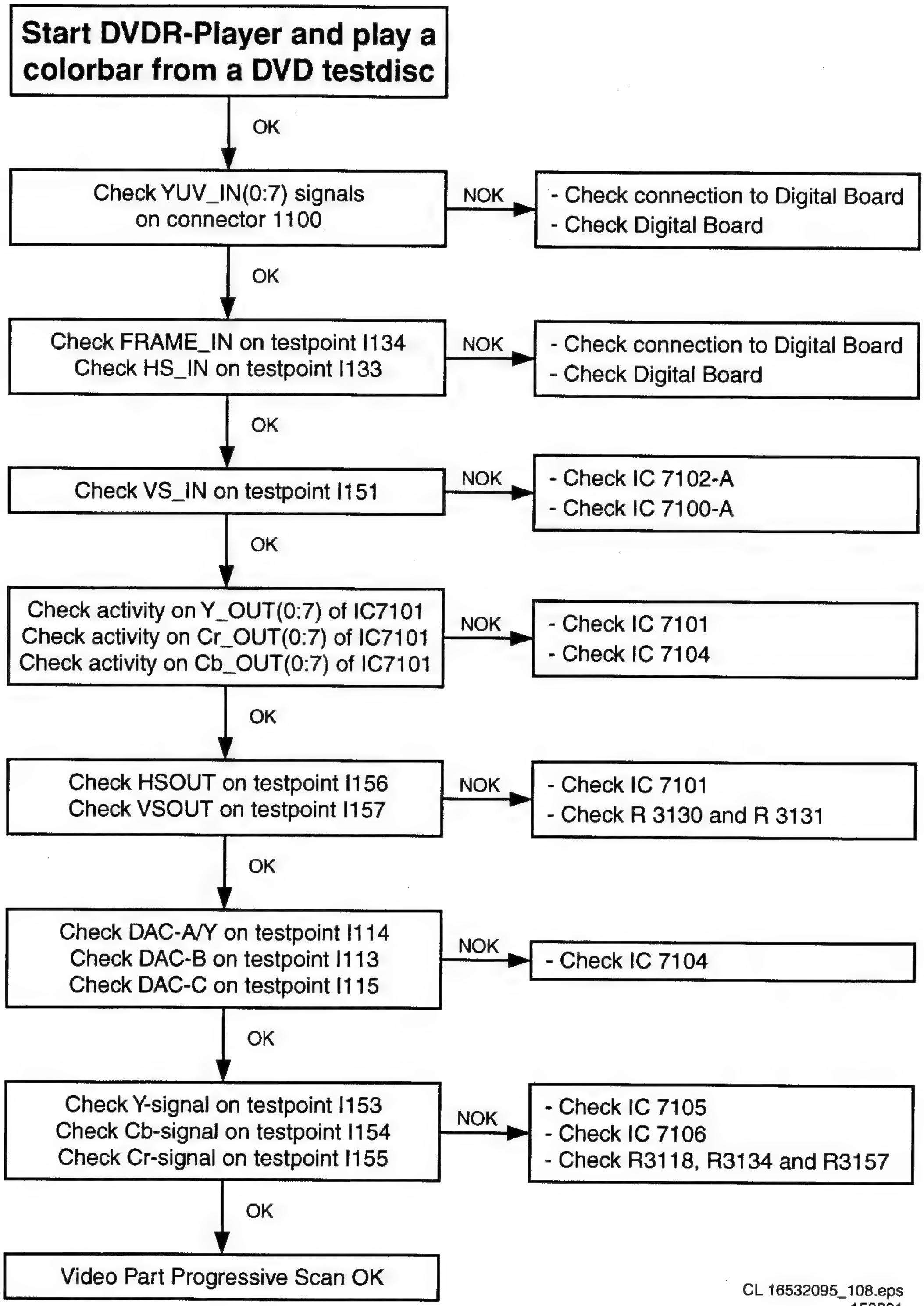


Figure 5-41

5.6.7 Progressive Scan

Video Part Check

VIDEO PART CHECK PROGRESSIVE SCAN



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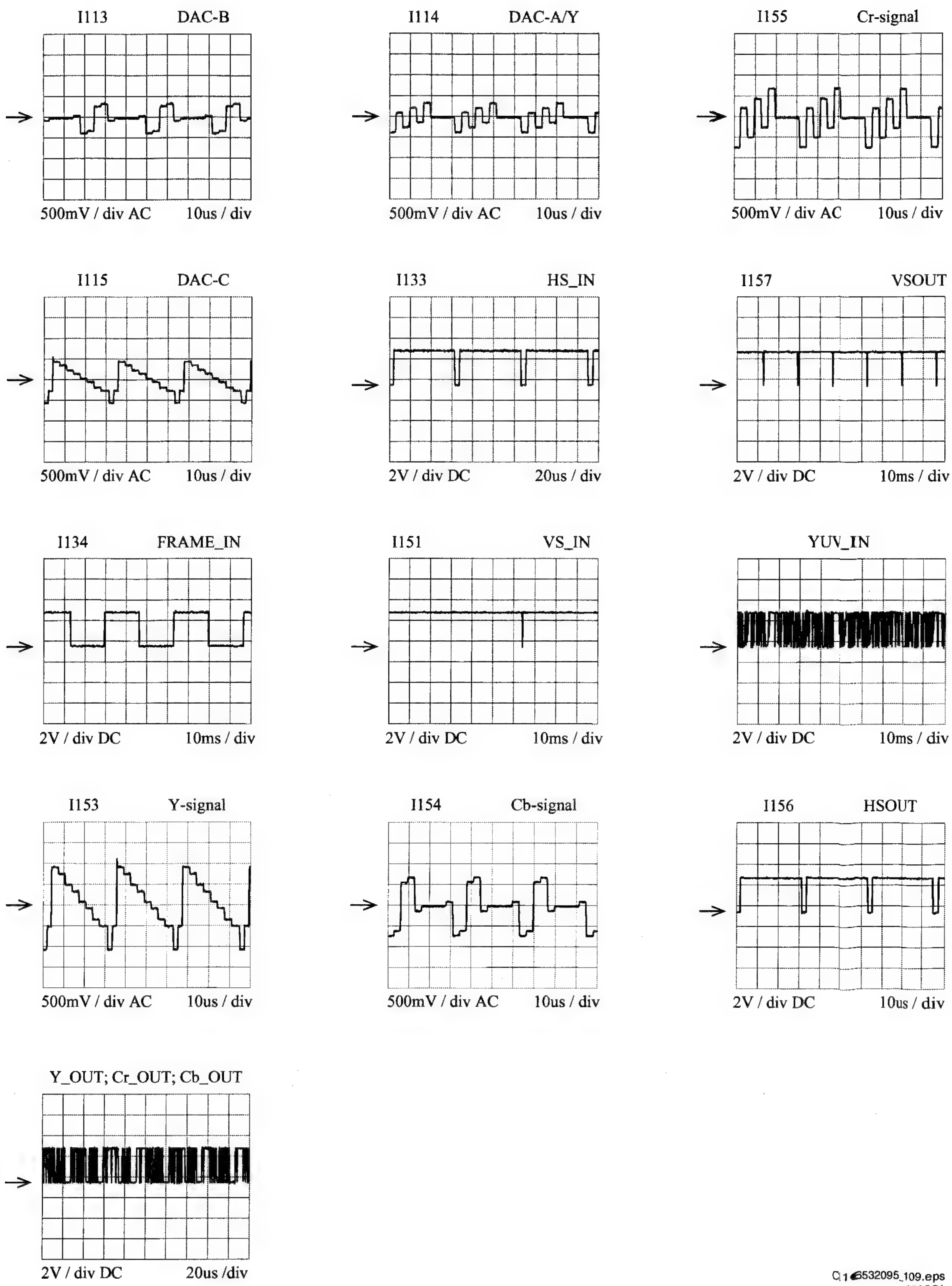
150801

Figure 5-42

Waveforms

Waveforms Progressive Scan



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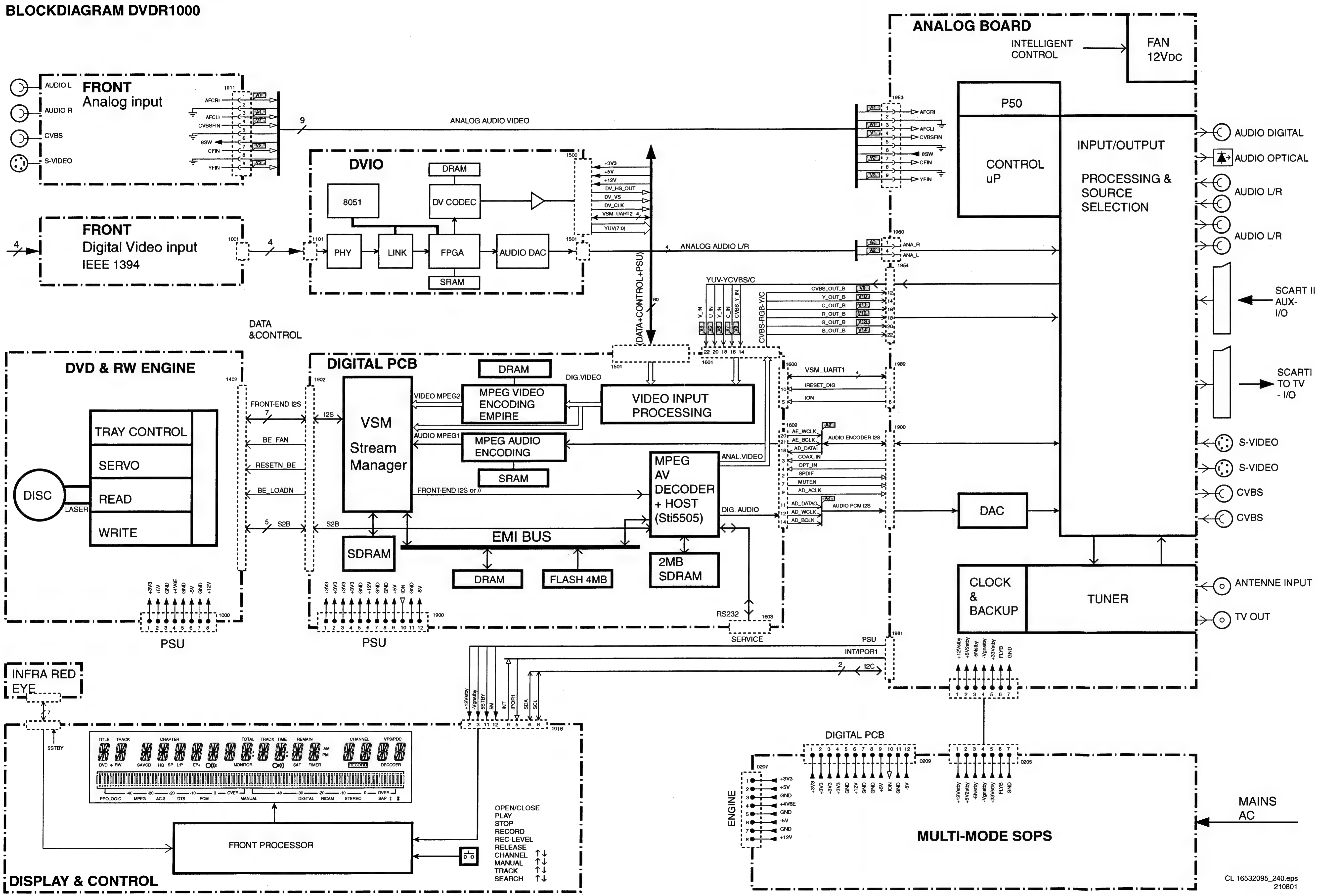
150801

Figure 5-43

Personal Notes:

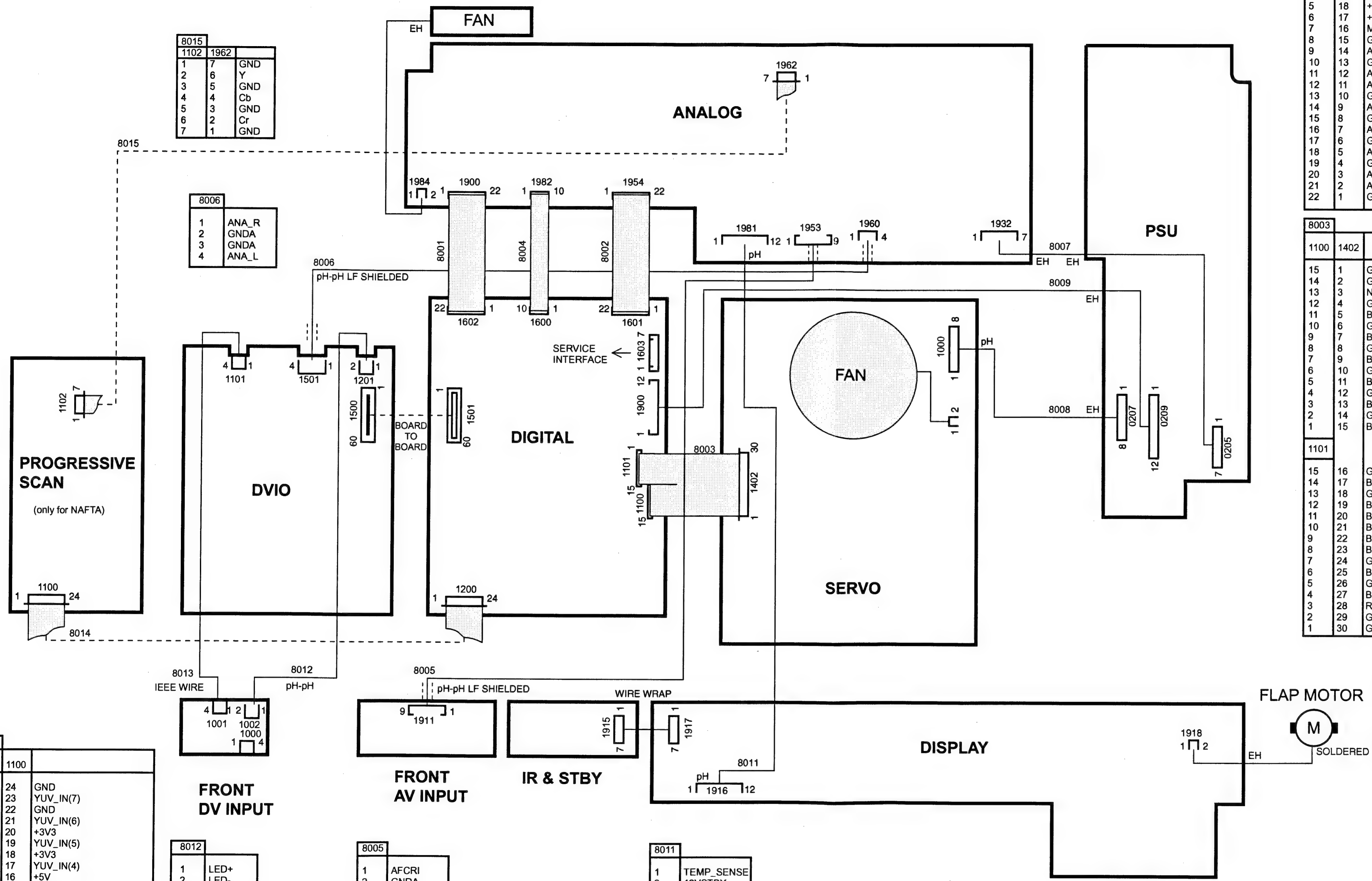
6. Block and Wiring Diagram.

Blockdiagram DVDR1000



Wiring Diagram

WIRING DIAGRAM



8015		
1102	1962	
1	7	GND
2	6	Y
3	5	GND
4	4	Cb
5	3	GND
6	2	Cr
7	1	GND

8006	
1	ANA_R
2	GNDA
3	GNDA
4	ANA_L

8001		
1602	1900	
1	22	GNDD
2	21	SPDIF
3	20	COAX_IN
4	19	OPT_IN
5	18	+5V
6	17	+3V3
7	16	MUTEN
8	15	GNDD
9	14	AD_ACLK
10	13	GNDD
11	12	AD_DATAO
12	11	AD_WCLK
13	10	GNDD
14	9	AD_BCLK
15	8	GNDD
16	7	AD_ACLK
17	6	GNDD
18	5	AD_DATAI
19	4	GNDD
20	3	AE_WCLK
21	2	AE_BCLK
22	1	GNDD

8002		
1601	1954	
1	22	B_OUT_B
2	21	GNDD
3	20	G_OUT_B
4	19	GNDD
5	18	R_OUT_B
6	17	GNDD
7	16	C_OUT_B
8	15	GNDD
9	14	Y_OUT_B
10	13	GNDD
11	12	CVBS_OUT_B
12	11	GNDD
13	10	GNDD
14	9	CVBS_Y_IN
15	8	GNDD
16	7	C_IN
17	6	GNDD
18	5	Y_IN
19	4	GNDD
20	3	U_IN
21	2	GNDD
22	1	V_IN

8003		
1100	1402	
15	1	GNDD
14	2	GNDD
13	3	NC
12	4	GNDD
11	5	BE_DATA_WR
10	6	GNDD
9	7	BE_SYNC
8	8	GNDD
7	9	BE_FLAG
6	10	GNDD
5	11	BE_BCLK
4	12	GNDD
3	13	BE_DATA_RD
2	14	GNDD
1	15	BE_WCLK
1101		
15	16	GNDD
14	17	BE_RXD
13	18	GNDD
12	19	BE_TXD
11	20	BE_CPR
10	21	BE_IRQn
9	22	BE_SUR
8	23	BE_V4
7	24	GNDD
6	25	BE_LOAD
5	26	GNDD
4	27	BE_FAN
3	28	RESETn_BE
2	29	GNDD
1	30	GNDD

8004		
1600	1982	
1	10	GNDD
2	9	FB
3	8	BE_FAN
4	7	ANA_WE
5	6	ION
6	5	VSM_UART1_RTSn (D_RDY)
7	4	VSM_UART1_CTSn (A_RDY)
8	3	VSM_UART1_TX (D_DATA)
9	2	VSM_UART1_RX (A_DATA)
10	1	IRESET_DIG

8007	
1	+12Vstby
2	+5V2stby
3	-5Nstby
4	-Vgnstby
5	+33Vstby
6	FLYB
7	GND

8008	
1	+3V3
2	+5V
3	GND
4	+4V6E
5	GND
6	-5V
7	GND
8	+12V

8009	
1	+3V3
2	+3V3
3	+3V3
4	+3V3
5	GNDD
6	+12V
7	GNDD
8	GNDD
9	+5V
10	ION(STBY_ctrl
11	GNDD
12	-5V

8014		
1200	1100	
1	24	GND
2	23	YUV_IN(7)
3	22	GND
4	21	YUV_IN(6)
5	20	+3V3
6	19	YUV_IN(5)
7	18	+3V3
8	17	YUV_IN(4)
9	16	+5V
10	15	YUV_IN(3)
11	14	GND
12	13	YUV_IN(2)
13	12	GND
14	11	YUV_IN(1)
15	10	GND
16	9	YUV_IN(0)
17	8	GND
18	7	CLK_27MHZ
19	6	GND
20	5	HS_IN
21	4	FRAME_IN
22	3	SCL
23	2	SDA
24	1	GND

8012	
1	LED+
2	LED-

8013	
1	TPB1-
2	TPB1+
3	TPA1-
4	TPA1+

8005	
1	AFCRI
2	GNDA
3	AFCLI
4	VBSFIN
5	GNDV
6	8SW
7	CFIN
8	GNDV
9	YFIN

8011	
1	TEMP_SENSE
2	12VSTBY
3	VGNSTBY
4	-GNDD
5	IPOR1
6	SDA
7	GNDD
8	SCL
9	INT
10	RC
11	5STBY
12	5M

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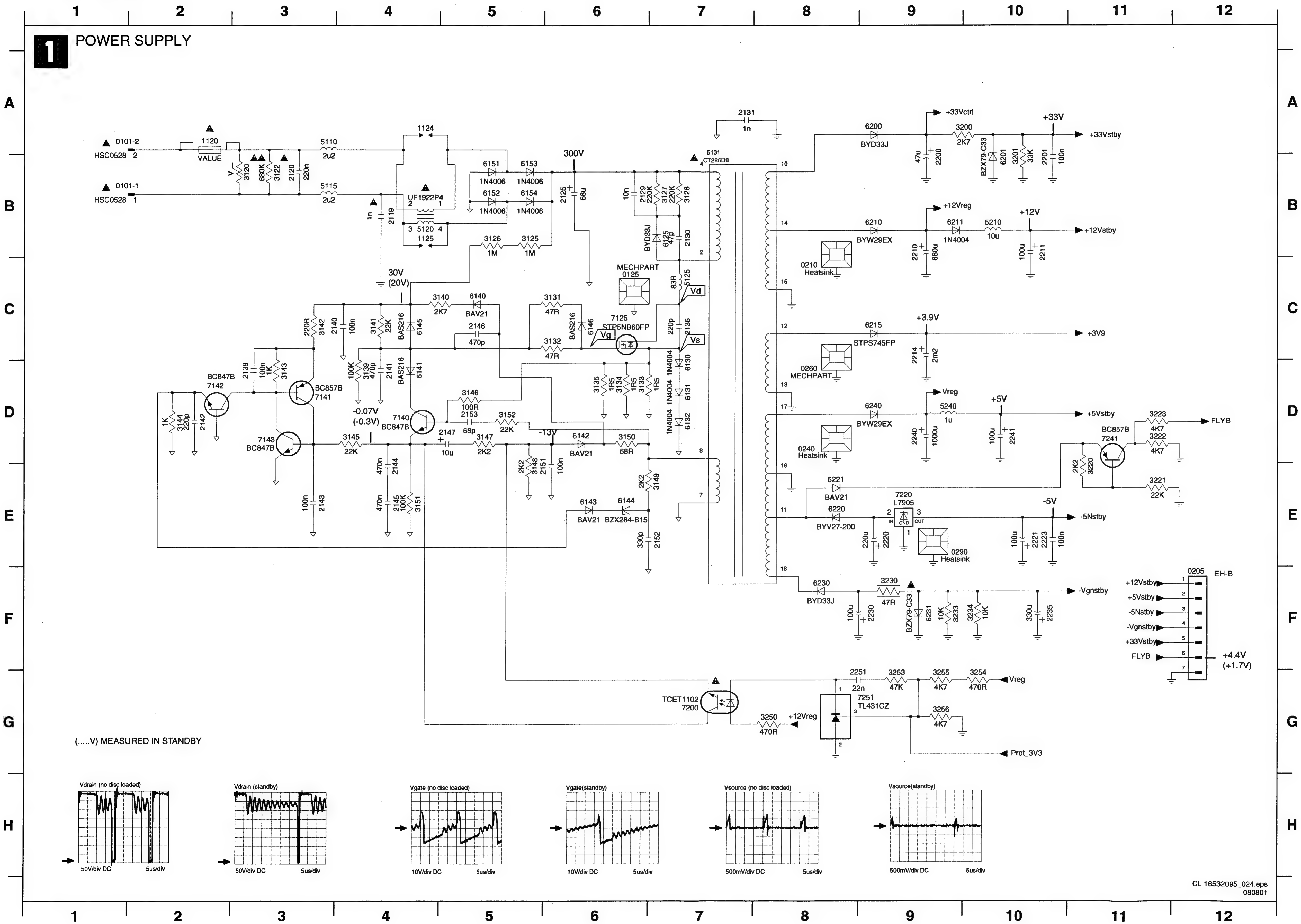
160801

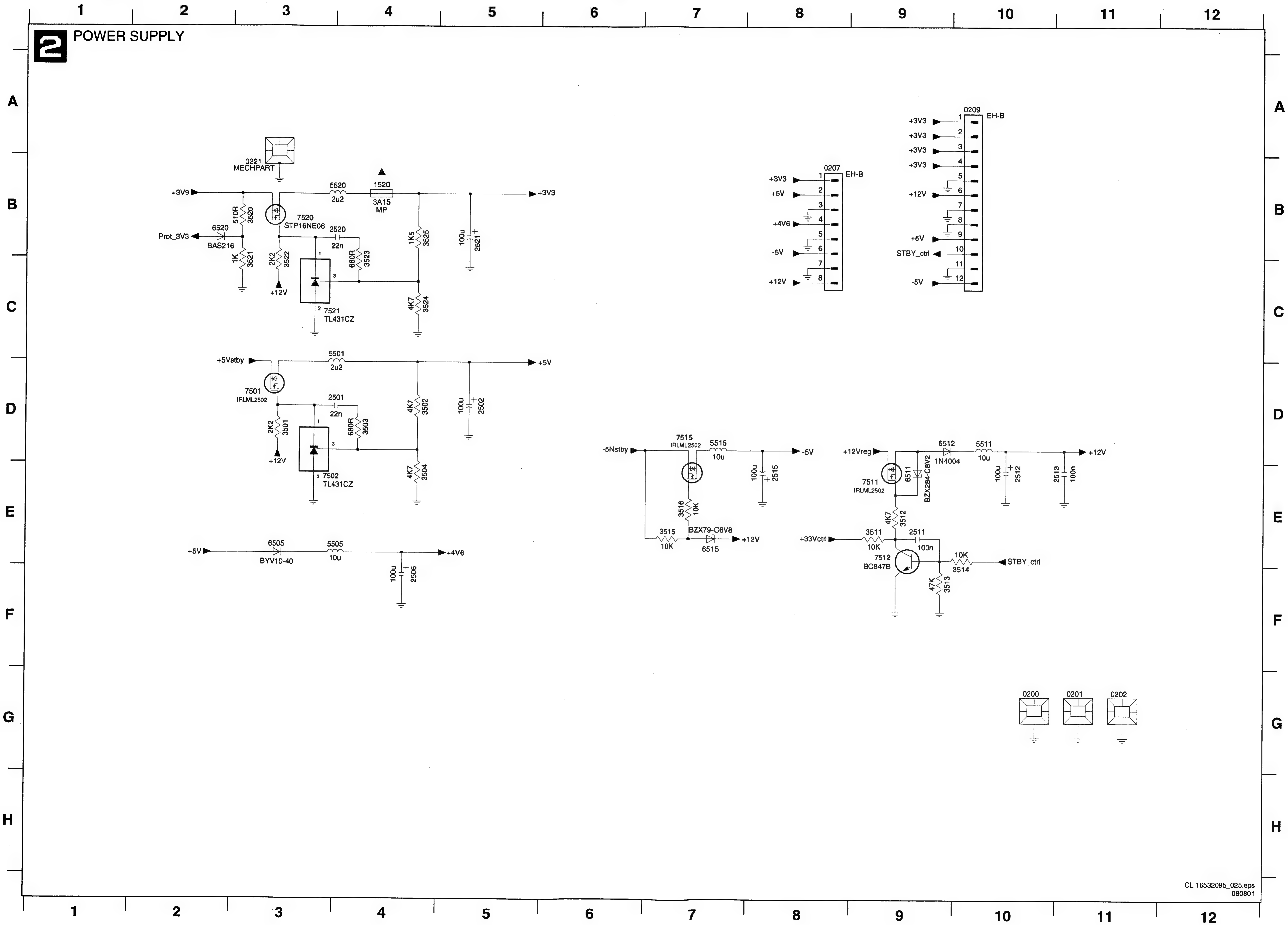
7. Electrical Diagrams And Print-Layouts

Power Supply



0101-1 B1	6130 D7
0101-2 A1	6131 D7
0125 C6	6132 D7
0205 F12	6140 C5
0210 C8	6141 D4
0240 D8	6142 D6
0260 D8	6143 E6
0290 E9	6144 E6
1120 A2	6145 C4
1124 A4	6146 C6
1125 B4	6151 B5
2119 B4	6152 B5
2120 B3	6153 B5
2125 B6	6154 B5
2126 B6	6200 A9
2127 A4	6201 B10
2129 B6	6210 B9
2130 B7	6211 B9
2131 A7	6215 C9
2136 C7	6220 E8
2139 D3	6221 E8
2140 C4	6230 F8
2141 D4	6231 F9
2142 D2	6240 D9
2143 E3	7125 C6
2144 E4	7140 D4
2145 E4	7141 D3
2146 C5	7142 D2
2147 D5	7143 D3
2151 E5	7200 G7
2152 E7	7220 E9
2153 D5	7241 D11
2200 B9	7251 G8
2201 B10	9110 A3
2210 B9	9115 B3
2211 B10	
2212 B9	
2214 C9	
2215 C9	
2220 E9	
2221 E10	
2222 E10	
2223 E10	
2230 F9	
2235 F10	
2240 D9	
2241 D10	
2242 D9	
2251 G9	
3120 B3	
3122 B3	
3123 B2	
3125 B5	
3126 B5	
3127 B7	
3128 B7	
3129 A5	
3131 C6	
3132 C6	
3133 D6	
3134 D6	
3135 D6	
3139 D4	
3140 C5	
3141 C4	
3142 C3	
3143 D3	
3144 D2	
3145 D4	
3146 D5	
3147 D5	
3148 E5	
3149 E7	
3150 D6	
3151 E4	
3152 D5	
3200 A10	
3201 B10	
3220 E11	
3221 E11	
3222 D11	
3223 D11	
3230 F9	
3233 F9	
3234 F10	
3250 G8	
3253 G9	
3254 G10	
3255 G9	
3256 G9	
5110 A3	
5115 B3	
5120 B4	
5121 B4	
5125 C7	
5131 B7	
5210 B10	
5240 D9	
6125 B7	
6128 A4	
6129 A5	

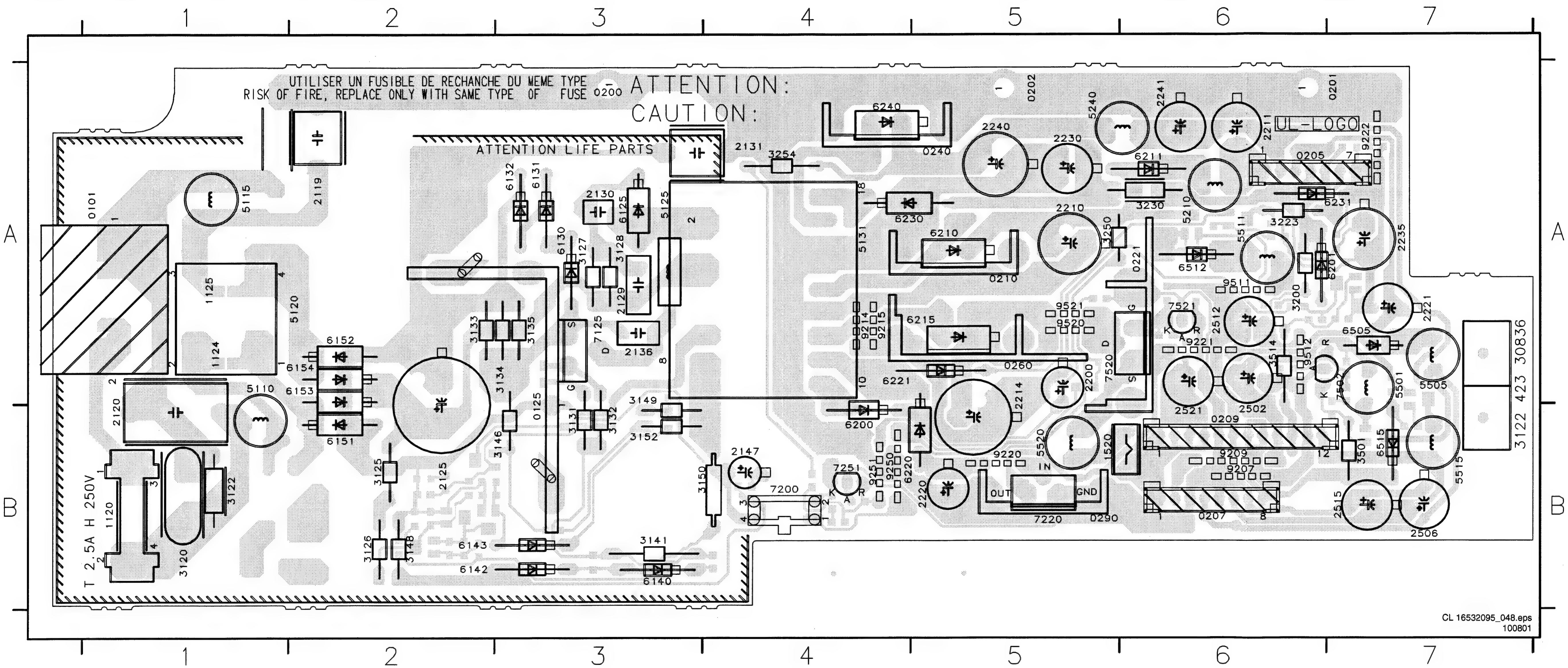
Power Supply



0200 G10
0201 G11
0202 G11
0207 B8
0209 A10
0221 B3
1520 B4
2501 D4
2502 D5
2506 F4
2511 E9
2512 E10
2513 E11
2515 E8
2520 B4
2521 B5
3501 D3
3502 D4
3503 D4
3504 E4
3511 E9
3512 E9
3513 F9
3514 E10
3515 E7
3516 E7
3520 B3
3521 C3
3522 C3
3523 C4
3524 C4
3525 B4
5501 C4
5505 E4
5511 D10
5515 D7
5520 B4
6505 E3
6511 E9
6512 D9
6515 E7
6520 B2
7501 D3
7502 E3
7511 E9
7512 E9
7515 D7
7520 B3
7521 C3

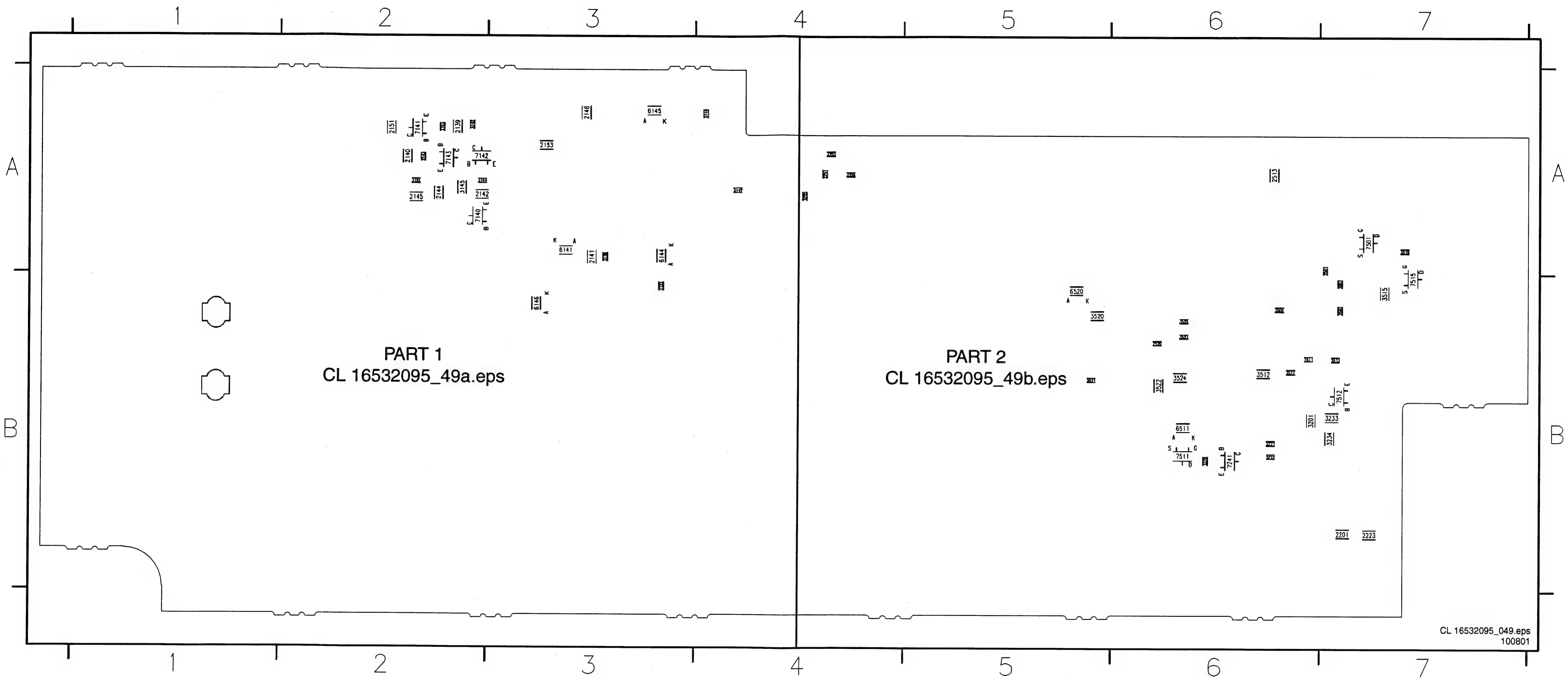
Layout Power Supply (Top View)

0101 A1	0209 B6	1520 B5	2130 A3	2212 A5	2240 A5	2521 B6	3128 A3	3141 B3	3223 A6	5115 A1	5501 A7	6129 B1	6151 B2	6211 A6	6505 A7	7502 A7	9214 A4	9511 A6
0125 B3	0210 A5	2119 A2	2131 A4	2214 A5	2241 A6	3120 B1	3129 B2	3146 B3	3230 A6	5120 A2	5505 A7	6130 A3	6152 A2	6215 A5	6512 A6	7520 A5	9215 A4	9512 A6
0200 A3	0221 A6	2120 B1	2136 A3	2215 A5	2242 A4	3122 B1	3131 B3	3148 B2	3250 A5	5121 A1	5511 A6	6131 A3	6153 A2	6220 B4	6515 B7	7521 A6	9220 B5	9520 A5
0201 A7	0240 A5	2125 B2	2147 B4	2220 B5	2502 B6	3123 A1	3132 B3	3149 A3	3254 A4	5125 A3	5515 B7	6132 A3	6154 A2	6221 A4	7125 A3	9110 B1	9221 A6	9521 A5
0202 A5	0260 A5	2126 B2	2200 A5	2221 A7	2506 B7	3125 B2	3133 A2	3150 B3	3501 B7	5131 A4	5520 B5	6140 B3	6200 B4	6230 A4	7200 B4	9115 A1	9222 A7	
0205 A6	0290 B5	2127 B1	2210 A5	2230 A5	2512 A6	3126 B2	3134 A3	3152 B3	3514 A6	5210 A6	6125 A3	6142 B2	6201 A7	6231 A7	7220 B5	9207 B6	9250 B4	
0207 B6	1120 B1	2129 A3	2211 A6	2235 A7	2515 B7	3127 A3	3135 A3	3200 A6	5110 A1	5240 A5	6128 B1	6143 B2	6210 A5	6240 A4	7251 B4	9209 B6	9251 B4	

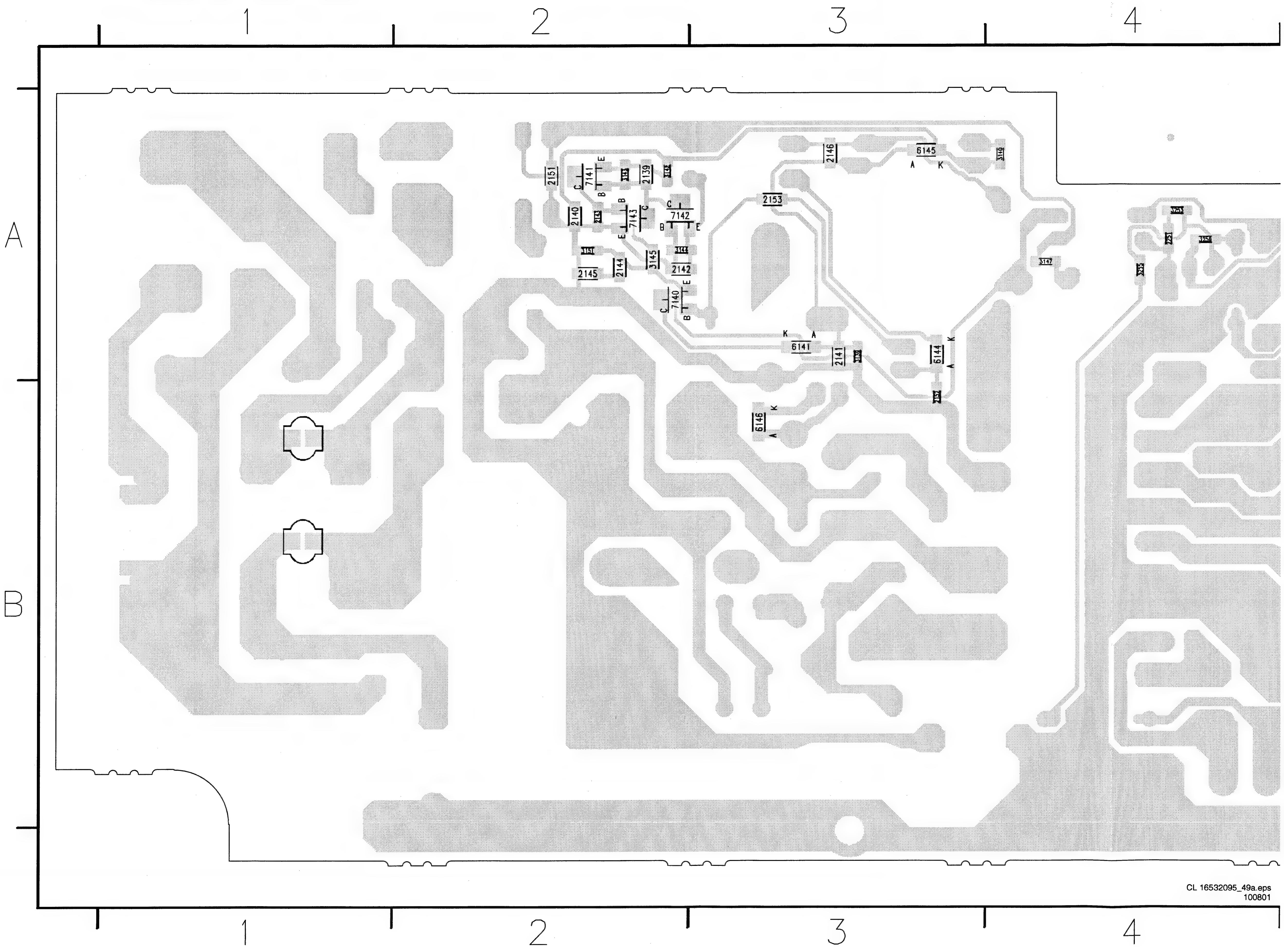


Layout Power Supply (Overview Bottom View)

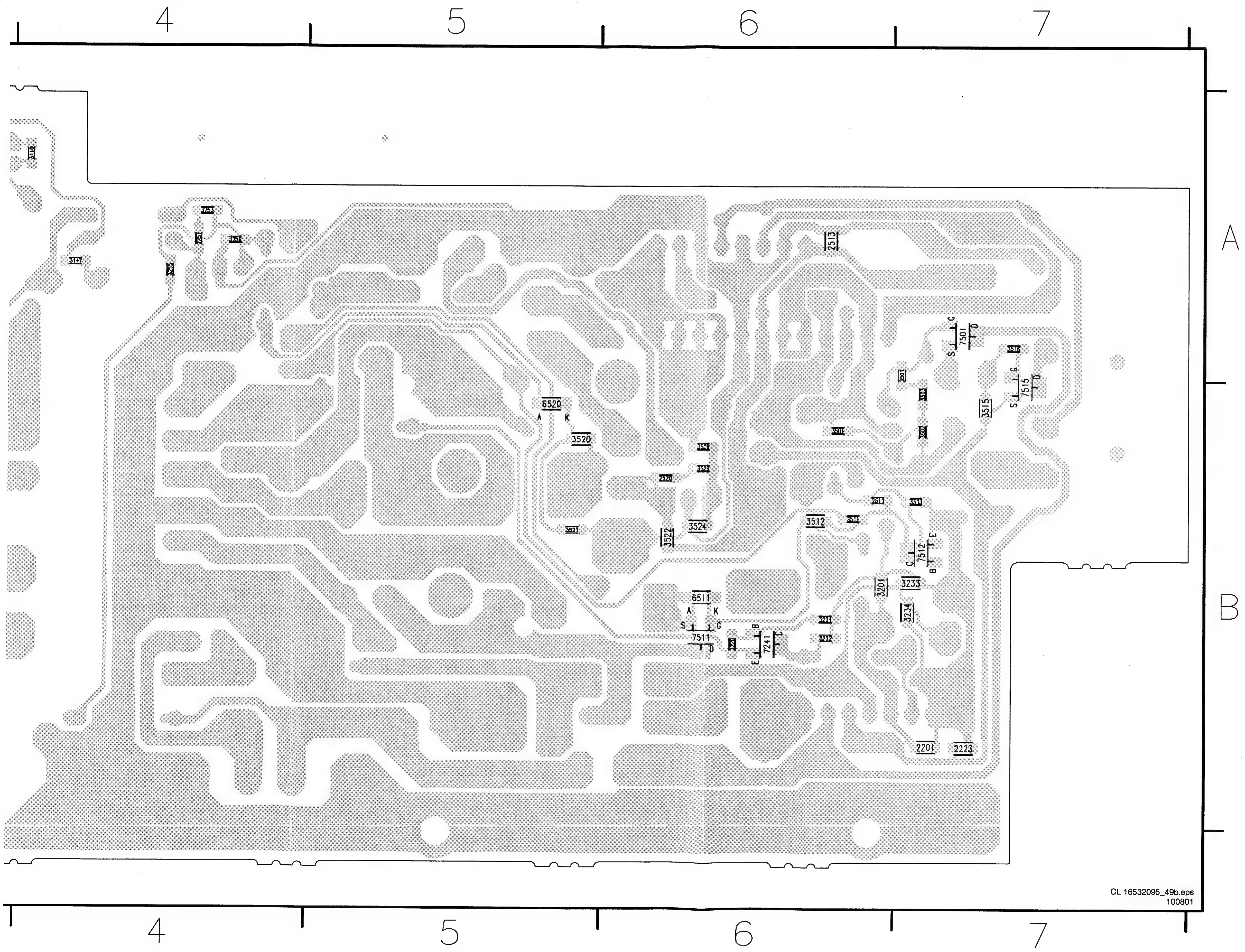
2139	A2	2143	A2	2151	A2	2222	A5	2511	B6	3140	A4	3145	A2	3220	B6	3234	B7	3502	B7	3512	B6	3520	B5	3524	B6	6145	A3	7140	A2	7241	B6	7515	B7
2140	A2	2144	A2	2152	B3	2223	B7	2513	A6	3142	A2	3147	A4	3221	B6	3253	A4	3503	B7	3513	B7	3521	B5	3525	B6	6146	B3	7141	A2	7501	A7		
2141	A3	2145	A2	2153	A3	2251	A4	2520	B6	3143	A2	3151	A2	3222	B6	3255	A4	3504	B6	3515	B7	3522	B6	6141	A3	6511	B6	7142	A2	7511	B6		
2142	A2	2146	A3	2201	B7	2501	A7	3139	A3	3144	A2	3201	B6	3233	B7	3256	A4	3511	B6	3516	A7	3523	B6	6144	A3	6520	B5	7143	A2	7512	B7		



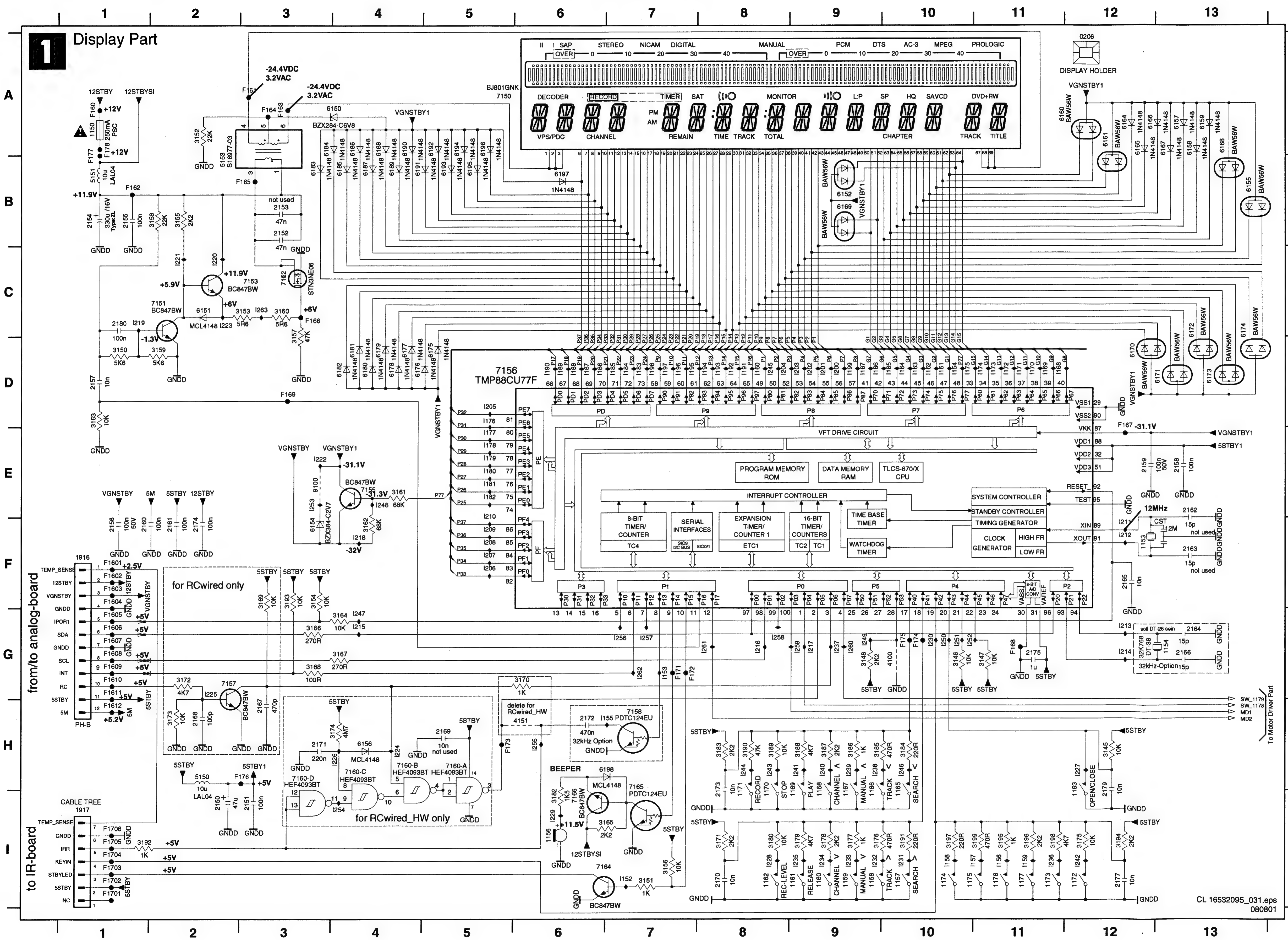
Layout Power Supply (Part 1 Bottom View)



Layout Power Supply (Part 2 Bottom View)

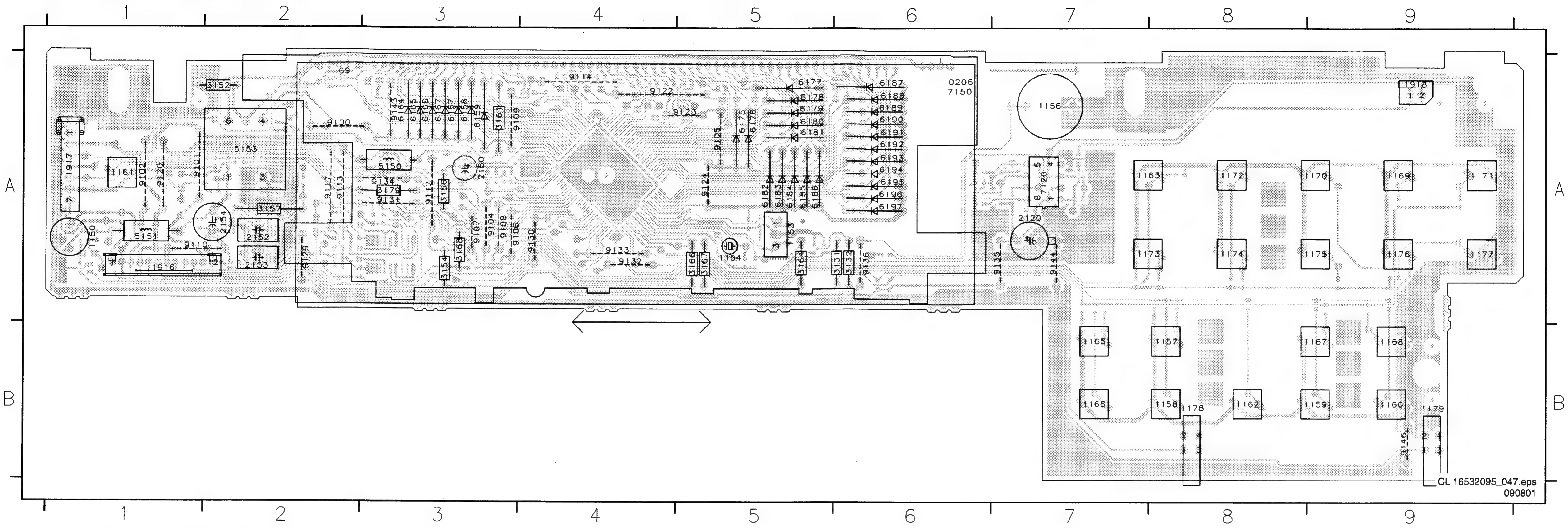


Display Panel



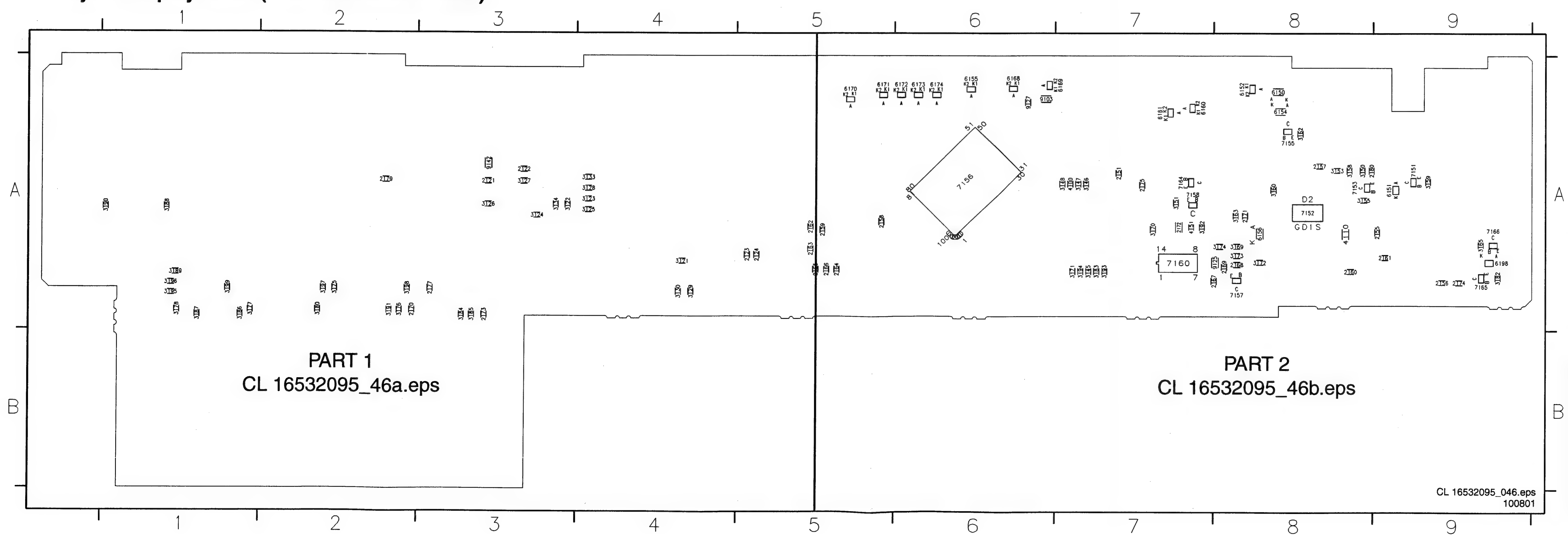
0206 A12	6154 F3	I174 D11
1150 A1	6155 B13	I175 D10
1153 F12	6156 H4	I176 D5
1154 G13	6157 A13	I177 E5
1156 I6	6158 A13	I178 E5
1157 I10	6159 A13	I179 E5
1158 I9	6160 A11	I180 E5
1159 I9	6161 A12	I181 E5
1160 I9	6164 A12	I182 E5
1161 I9	6165 A12	I183 D7
1162 I8	6166 A12	I184 D7
1163 H12	6167 A13	I185 D7
1165 H10	6168 A13	I186 D6
1166 H9	6169 B9	I187 D6
1167 H9	6170 D12	I188 D6
1168 H9	6171 D13	I189 D6
1169 H9	6172 D13	I190 D6
1170 H8	6173 D13	I191 D8
1171 H8	6174 D13	I192 D8
1172 I12	6175 D5	I193 D8
1173 I11	6176 D4	I194 D8
1174 I10	6177 D4	I195 D7
1175 I10	6178 D4	I196 D7
1176 I11	6179 D4	I197 D7
1177 I11	6180 D4	I198 D7
1916 F1	6181 D4	I199 D9
1917 I1	6182 D4	I200 D9
2150 I2	6183 B3	I201 D9
2151 I3	6184 A3	I202 D9
2152 B3	6185 B4	I203 D9
2153 B3	6186 A4	I204 D8
2154 B1	6187 B4	I205 D5
2155 B1	6188 A4	I206 F5
2156 F1	6189 B4	I207 F5
2157 D1	6190 A4	I208 F5
2158 E13	6191 B4	I209 F5
2159 E12	6192 A5	I210 E5
2160 F1	6193 B5	I211 F12
2161 F2	6194 A5	I212 F12
2162 E13	6195 B5	I213 G12
2163 F13	6196 A5	I214 G12
2164 G13	6197 B6	I215 G4
2165 F12	6198 H7	I216 G8
2166 G13	7150 A5	I217 G9
2167 H3	7151 C2	I218 F4
2168 H2	7152 C3	I219 C1
2169 H5	7153 C3	I220 C2
2170 I8	7155 E4	I221 C2
2171 H3	7156 D6	I222 E3
2172 H6	7157 G2	I223 C2
2173 H8	7158 H7	I224 H4
2174 F2	7160-A H5	I225 G2
2175 G11	7160-B H4	I226 H4
2177 I12	7160-C H4	I227 H12
2179 H12	7160-D H3	I228 I8
2180 C1	7164 I6	I229 I6
3145 H12	7165 H7	I230 G10
3146 G10	7166 I6	I231 I10
3147 G11	9100 E3	I232 I9
3148 G9	F160 A1	I233 I9
3150 D1	F1601 F1	I234 I9
3151 I7	F1602 F1	I235 I9
3152 A2	F1603 F1	I236 I11
3153 C3	F1604 F1	I237 G9
3154 F3	F1605 G1	I238 H9
3155 B2	F1606 G1	I239 H9
3156 I7	F1607 G1	I240 H9
3157 C3	F1608 G1	I241 H9
3158 B2	F1609 G1	I242 I12
3159 D2	F161 A3	I243 H8
3160 C3	F1610 G1	I244 H8
3161 E4	F1611 G1	I245 D8
3162 F4	F1612 H1	I246 H10
3163 D1	F162 B1	I247 G4
3164 G4	F163 A3	I248 E4
3165 I7	F164 A3	I249 G9
3166 G3	F165 B3	I250 G10
3167 G4	F166 C3	I251 G10
3168 G3	F167 E12	I252 G10
3169 F3	F168 G11	I253 E3
3170 G6	F169 D3	I254 I4
3171 I8	F1701 I1	I255 H6
3172 G2	F1702 I1	I256 G7
3173 H2	F1703 I1	I257 G7
3174 H4	F1704 I1	I258 G8
3175 I12	F1705 I1	I259 G9
3176 I9	F1706 I1	I260 G9
3177 I9	F171 G7	I261 G8
3178 I9	F172 G7	I262 G7
3179 I9	F173 H5	I263 C3
3180 I8	F174 G10	
3182 I6	F175 G10	
3183 H8	F176 H3	
3184 H10	F177 A1	
3185 H9	F178 A1	
3186 H9	I152 I7	
3187 H9	I153 G7	
3188 H9	I154 D10	
3189 H8	I155 H7	
3190 H8	I156 I11	
3191 I10	I157 I10	
3192 I1	I158 I10	
3193 F3	I159 I11	
3194 I12	I160 D8	
3195 I11	I161 D10	
3196 I11	I162 D10	
3197 I10	I163 D10	
3198 I11	I164 D10	
3199 I11	I165 D10	
4100 G10	I166 D9	
4151 H6	I167 D9	
5150 H2	I168 D11	
5151 B1	I169 D11	
5153 B2	I170 D11	
6150 A4	I171 D11	
6151 C2	I172 D11	
6152 B9	I173 D11	

Layout Display Panel (Top View)



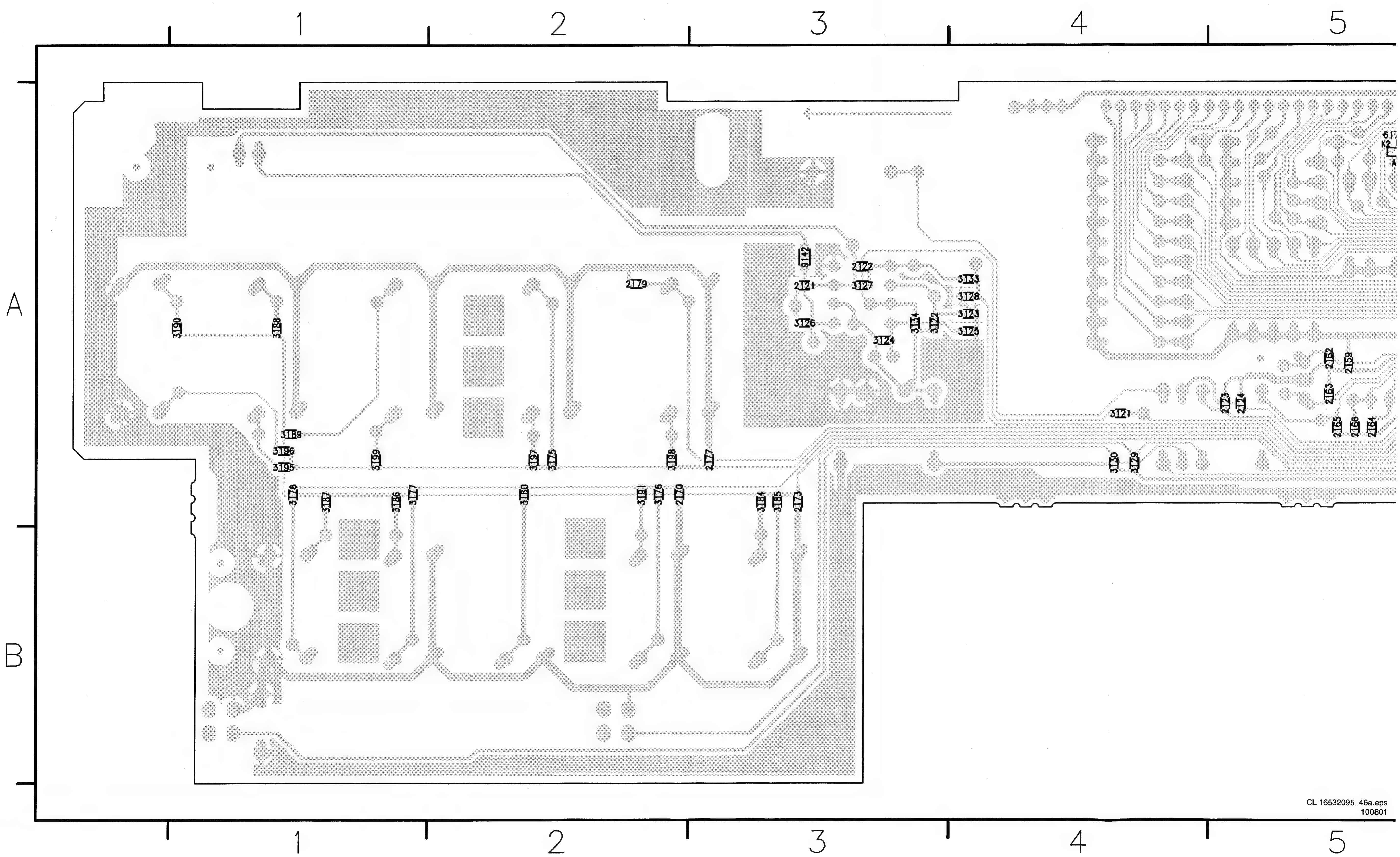
0206	A6	6179	A5
1150	A1	6180	A5
1153	A5	6181	A5
1154	A5	6182	A5
1156	A7	6183	A5
1157	B8	6184	A5
1158	B8	6185	A5
1159	B9	6186	A5
1160	B9	6187	A6
1161	A1	6188	A6
1162	B8	6189	A6
1163	A7	6190	A6
1165	B7	6191	A6
1166	B7	6192	A6
1167	B9	6193	A6
1168	B9	6194	A6
1169	A9	6195	A6
1170	A9	6196	A6
1171	A9	6197	A6
1172	A8	7120	A7
1173	A7	7150	A6
1174	A8	9100	A2
1175	A9	9101	A1
1176	A9	9102	A1
1177	A9	9104	A3
1178	B8	9105	A5
1179	B9	9106	A3
1916	A1	9107	A3
1917	A1	9108	A3
1918	A9	9109	A3
2120	A7	9110	A1
2150	A3	9112	A3
2152	A2	9113	A2
2153	A2	9114	A4
2154	A2	9117	A2
3131	A6	9120	A1
3132	A6	9122	A4
3152	A2	9123	A5
3154	A3	9124	A5
3156	A3	9129	A2
3157	A2	9130	A4
3161	A3	9131	A3
3164	A5	9132	A4
3166	A5	9133	A4
3167	A5	9134	A3
3168	A3	9135	A7
3179	A3	9136	A6
5150	A3	9143	A3
5151	A1	9144	A7
5153	A2	9146	B9
6157	A3		
6158	A3		
6159	A3		
6164	A3		
6165	A3		
6166	A3		
6167	A3		
6175	A5		
6176	A5		
6177	A5		
6178	A5		

Layout Display Panel (Overview Bottom View)



2121	A3	3146	A7	4100	A7
2122	A3	3147	A7	4110	A8
2123	A5	3148	A7	4151	A7
2124	A5	3150	A8	6150	A8
2151	A7	3151	A7	6151	A9
2155	A9	3153	A8	6152	A8
2156	A9	3155	A8	6154	A8
2157	A8	3158	A8	6155	A6
2158	A5	3159	A9	6156	A8
2159	A5	3160	A8	6160	A7
2160	A8	3162	A8	6161	A7
2161	A9	3163	A8	6168	A6
2162	A5	3165	A9	6169	A7
2163	A5	3169	A8	6170	A5
2164	A5	3170	A7	6171	A5
2165	A5	3171	A7	6172	A6
2166	A5	3172	A8	6173	A6
2167	A7	3173	A8	6174	A6
2168	A8	3174	A8	6198	A9
2169	A8	3175	A2	7151	A9
2170	A2	3176	A2	7152	A8
2171	A8	3177	A1	7153	A8
2172	A7	3178	A1	7155	A8
2173	A3	3180	A2	7156	A6
2174	A9	3182	A9	7157	A8
2175	A7	3183	A7	7158	A7
2177	A3	3184	A3	7160	A7
2179	A2	3185	A3	7164	A7
2180	A8	3186	A1	7165	A9
3121	A4	3187	A1	7166	A9
3122	A3	3188	A1	9103	A6
3123	A4	3189	A1	9125	A8
3124	A3	3190	A1	9127	A6
3125	A4	3191	A2	9142	A3
3126	A3	3192	A7		
3127	A3	3193	A7		
3128	A4	3194	A7		
3129	A4	3195	A1		
3130	A4	3196	A1		
3133	A4	3197	A2		
3134	A3	3198	A2		
3145	A7	3199	A1		

Layout Display Panel (Part 1 Bottom View)



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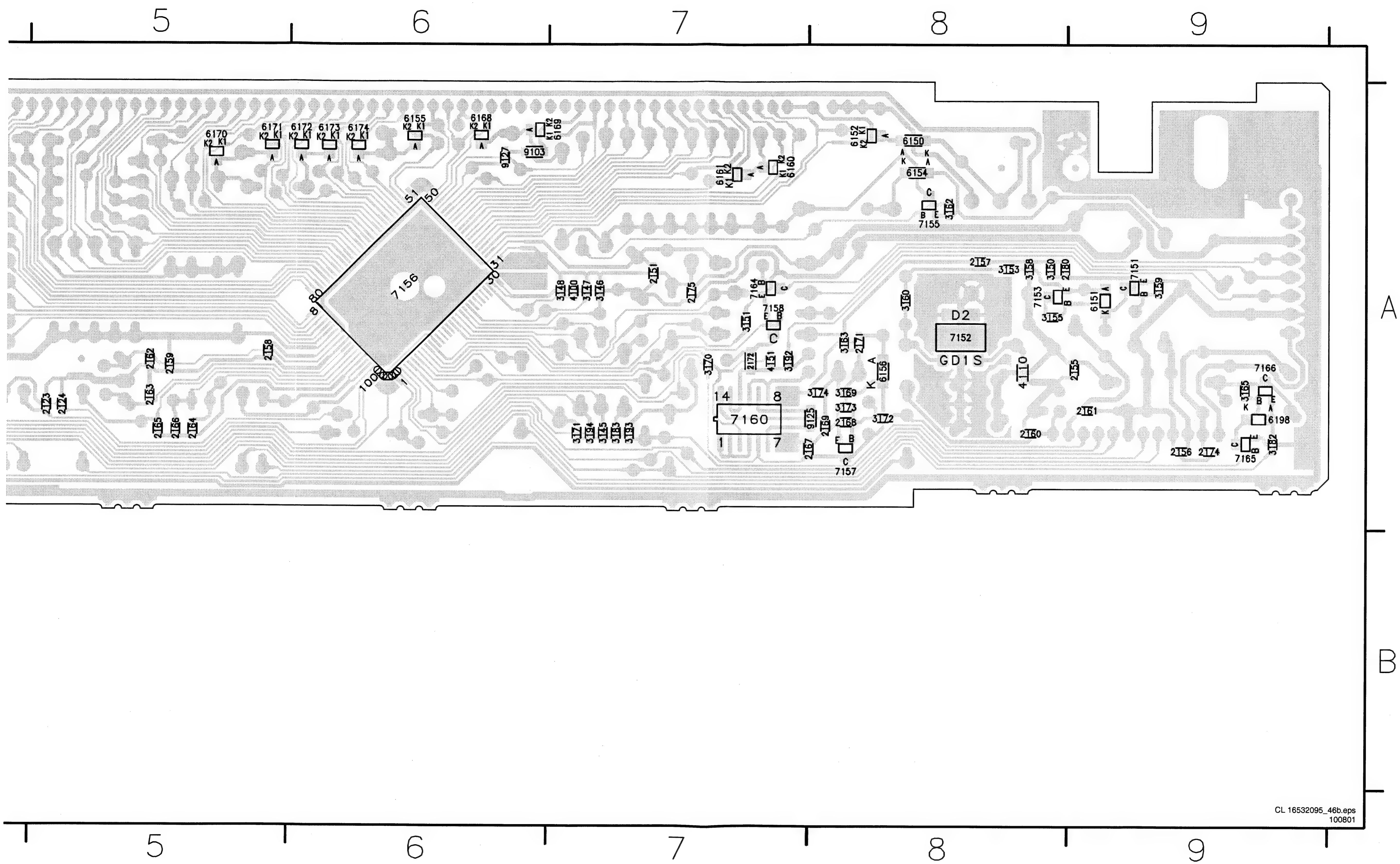
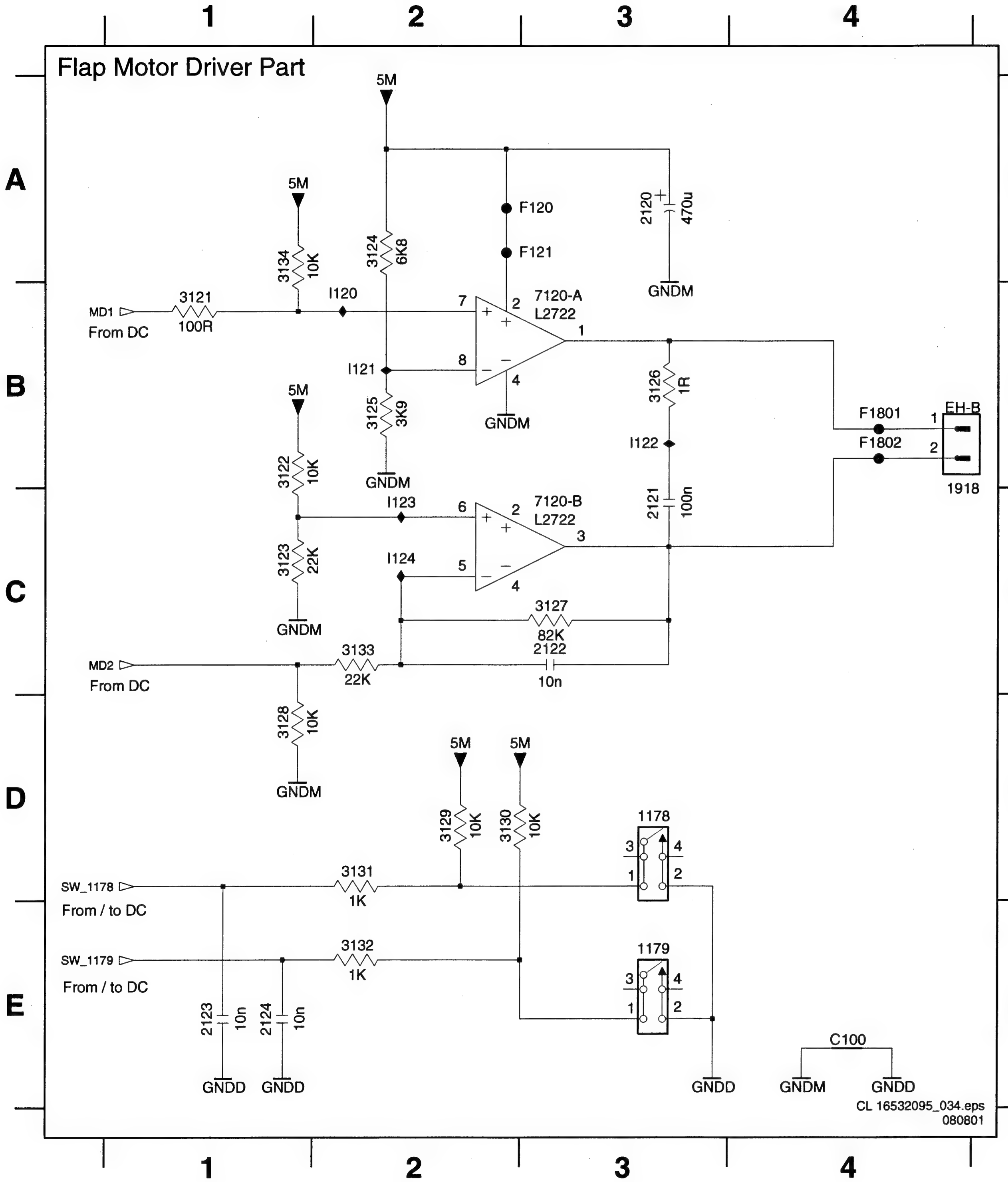
100801

Layout Display Panel (Part 2 Bottom View)

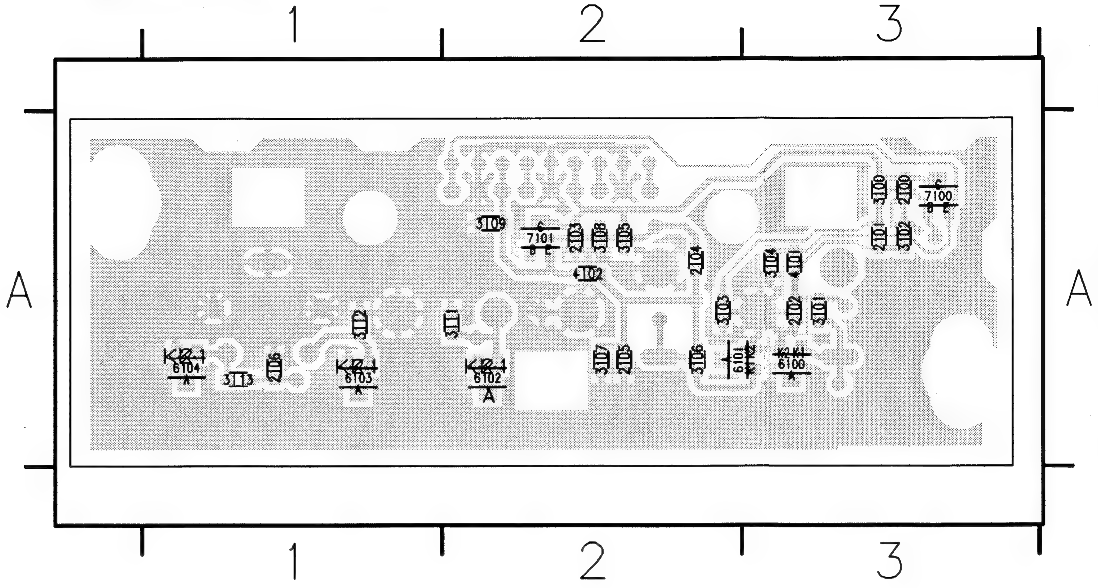


Flap Motor Driver Part

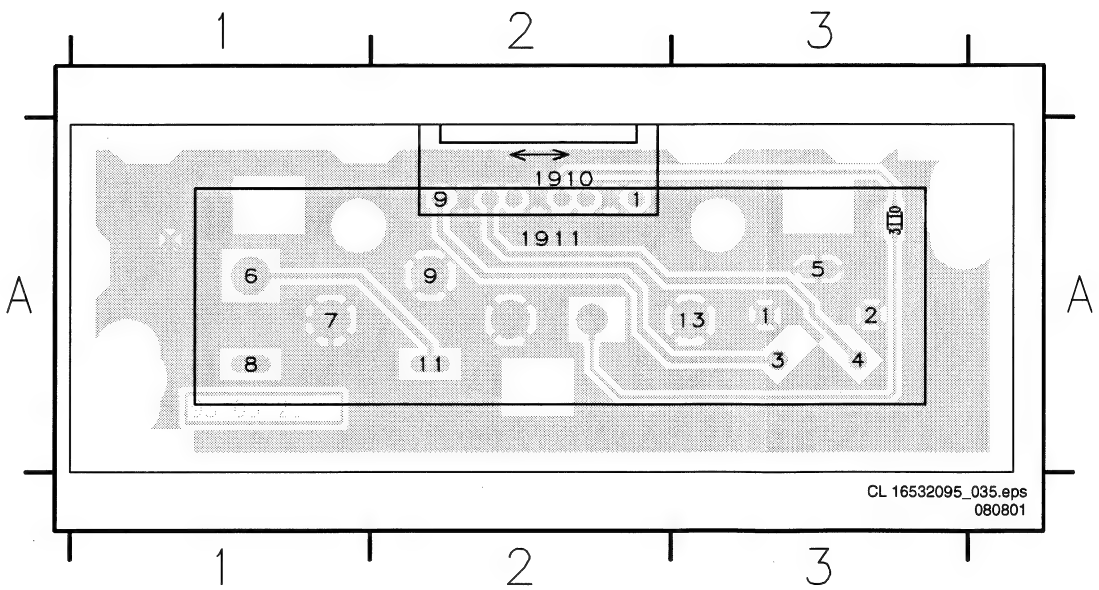
1178 D3	2121 C3	3121 B1	3125 B2	3129 D2	3133 C2	C100 E4	F1802 B4	I123 C2
1179 E3	2122 C3	3122 B1	3126 B3	3130 D2	3134 A1	F120 A3	I120 B2	I124 C2
1918 C4	2123 E1	3123 C1	3127 C3	3131 D2	7120-A B3	F121 A3	I121 B2	
2120 A3	2124 E1	3124 A2	3128 D1	3132 E2	7120-B C3	F1801 B4	I122 B3	



Layout Front AV Part

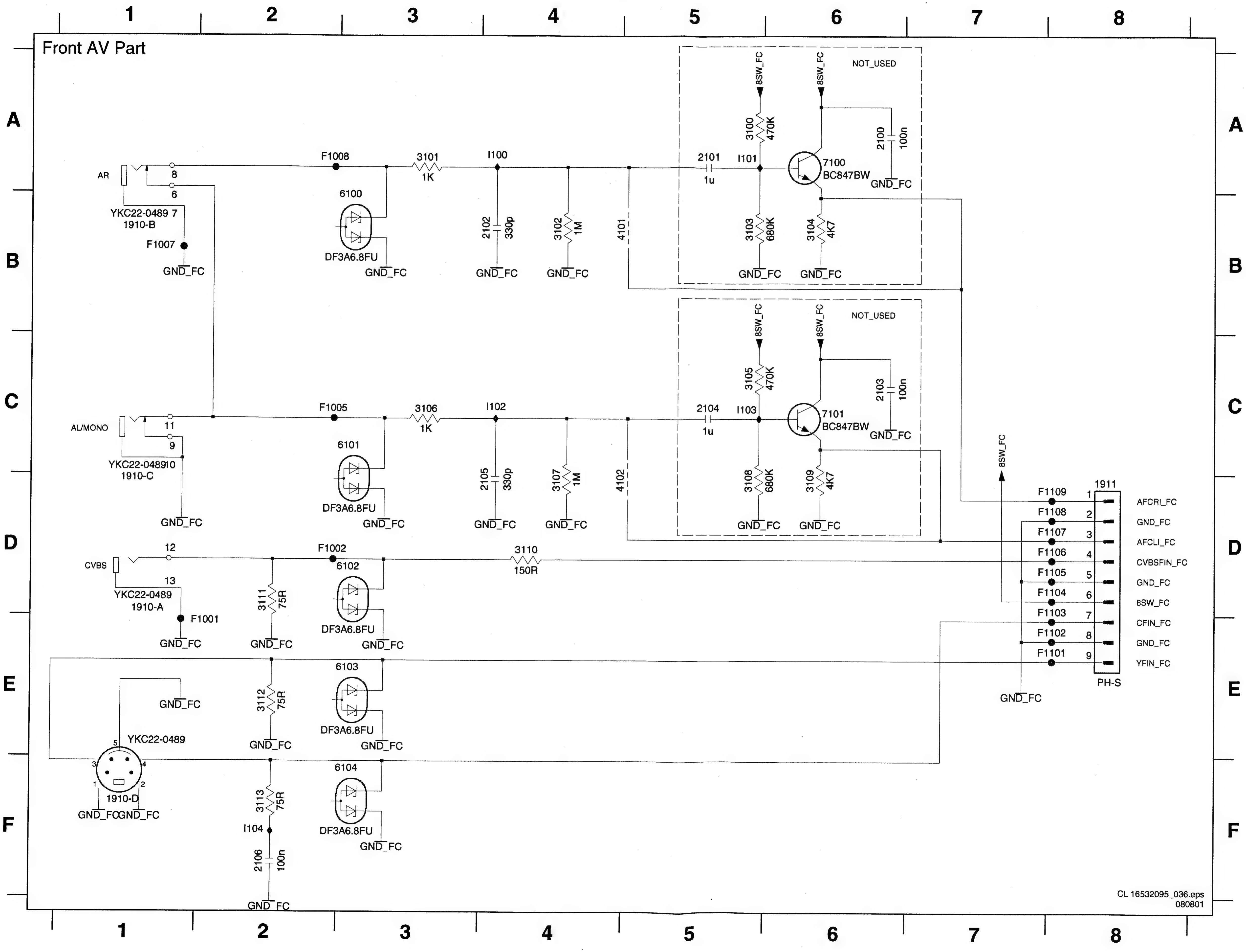


2100	A3	3113	A1
2101	A3	4101	A3
2102	A3	4102	A2
2103	A2	6100	A3
2104	A2	6101	A3
2105	A2	6102	A2
2106	A1	6103	A1
3100	A3	6104	A1
3101	A3	7100	A3
3102	A3	7101	A2
3103	A3		
3104	A3		
3105	A2		
3106	A2		
3107	A2		
3108	A2		
3109	A2		
3111	A1		
3112	A1		



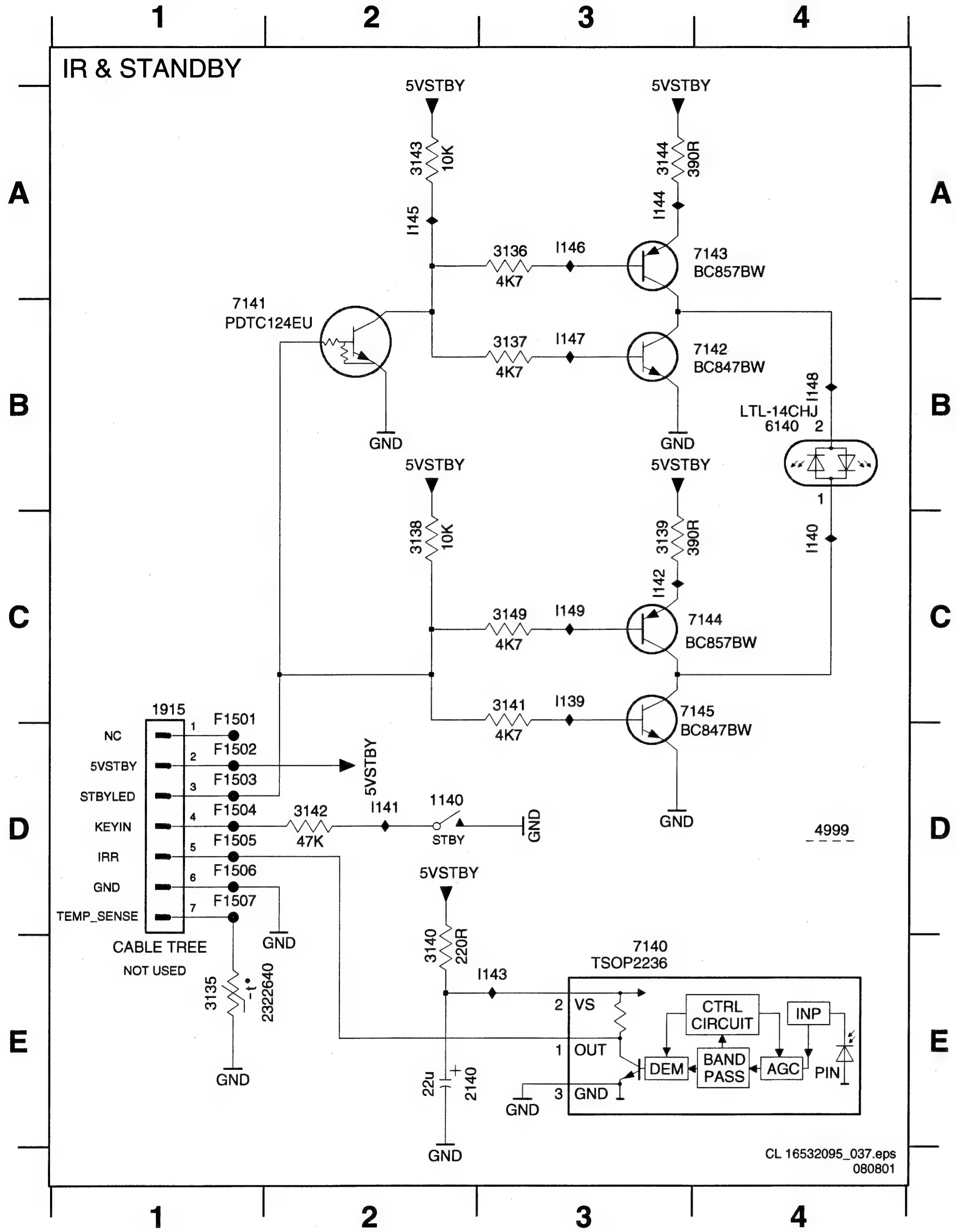
1910	A2
1911	A2

Front AV Part



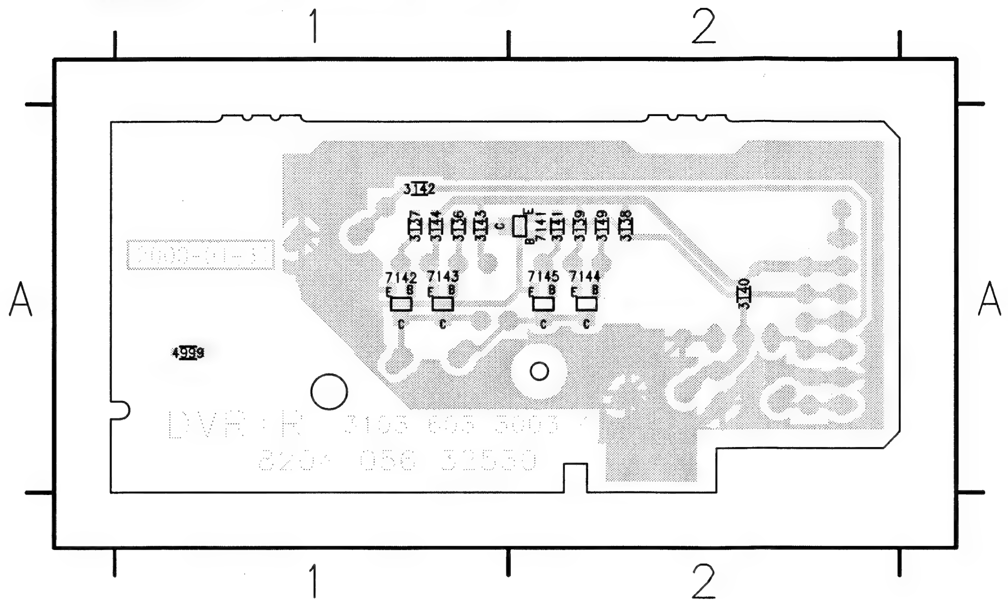
1910-A D1
1910-B B1
1910-C C1
1910-D F1
1911 D8
2100 A6
2101 A5
2102 B4
2103 C6
2104 C5
2105 D4
2106 F2
3100 A5
3101 A3
3102 B4
3103 B5
3104 B6
3105 C5
3106 C3
3107 D4
3108 D5
3109 D6
3110 D4
3111 D2
3112 E2
3113 F2
4101 B5
4102 D5
6100 A3
6101 C3
6102 D3
6103 E3
6104 F3
7100 A6
7101 C6
F1001 E2
F1002 D2
F1005 C2
F1007 B1
F1008 A2
F1101 E8
F1102 E8
F1103 D8
F1104 D8
F1105 D8
F1106 D8
F1107 D8
F1108 D8
F1109 D8
I100 A4
I101 A5
I102 C4
I103 C5
I104 F2

IR and Standby Panel

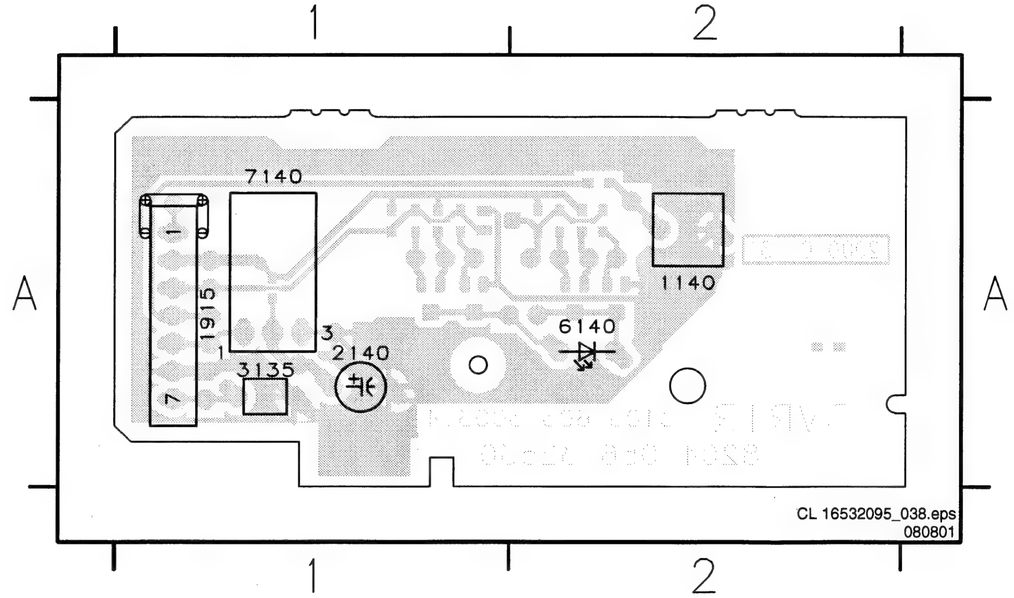


1140 D2
1915 C1
2140 E2
3135 E1
3136 A3
3137 B3
3138 C2
3139 C3
3140 E2
3141 C3
3142 D2
3143 A2
3144 A3
3149 C3
4999 D4
6140 B4
7140 E3
7141 B1
7142 B3
7143 A3
7144 C3
7145 C3
F1501 D1
F1502 D1
F1503 D1
F1504 D1
F1505 D1
F1506 D1
F1507 D1
I139 C3
I140 C4
I141 D2
I142 C3
I143 E3
I144 A3
I145 A2
I146 A3
I147 B3
I148 B4
I149 C3

Layout IR and Standby Panel

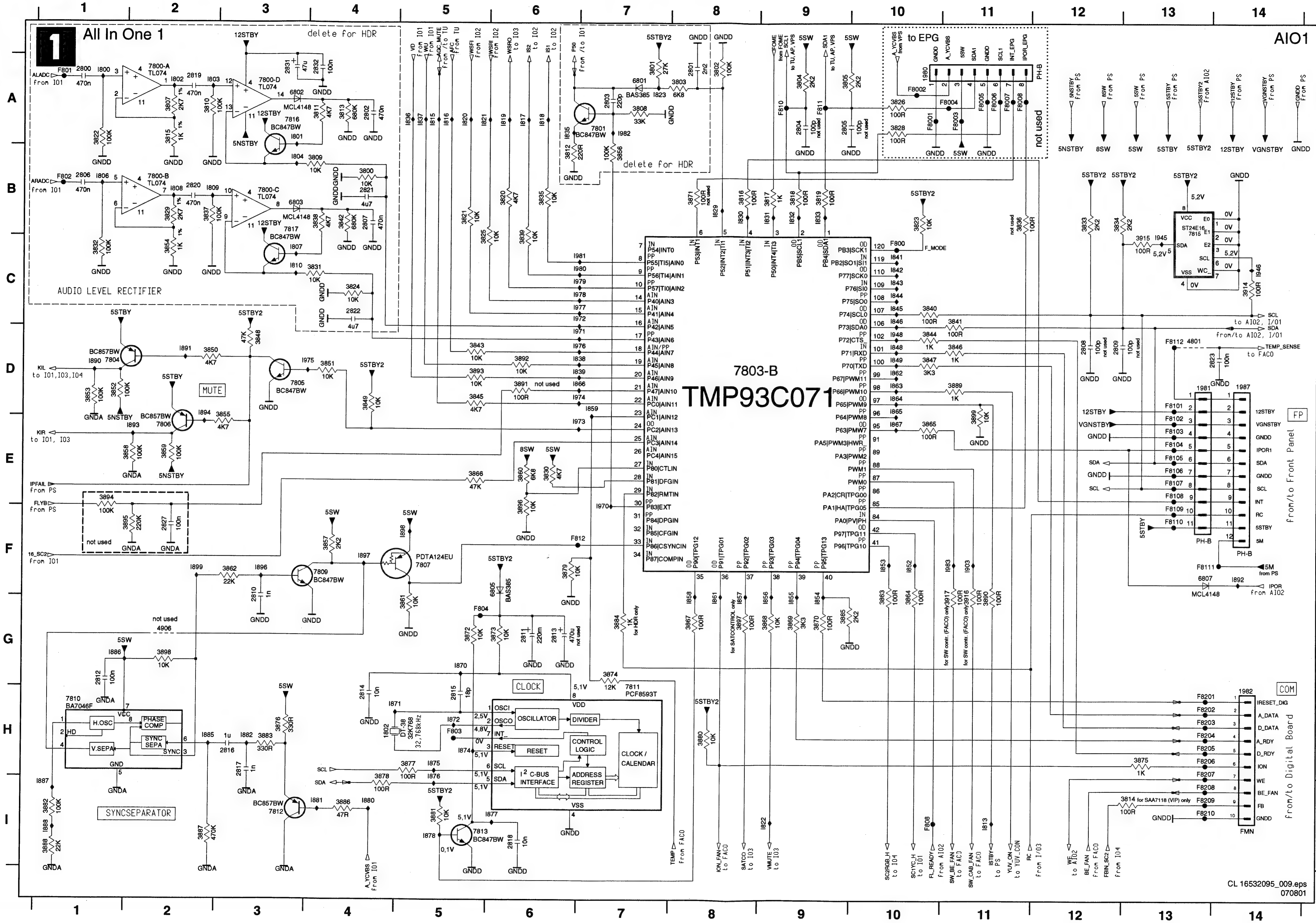


3137 A1
3137 A1
3138 A2
3139 A2
3140 A2
3141 A2
3142 A1
3143 A1
3144 A1
3149 A2
4999 A1
7141 A2
7142 A1
7143 A1
7144 A2
7145 A2



1140 A2
1915 A1
2140 A1
3135 A1
6140 A2
7140 A1

Analog Board: All in One 1



1802 H4
1980 A10
1981 D13
1982 H14
1987 D14
2800 A1
2801 A8
2802 A4
2803 A7
2804 A9
2805 A9
2806 B1
2807 B4
2808 D12
2809 D12
2810 F3
2811 G6
2812 G1
2813 G6
2814 H4
2815 H5
2816 H3
2817 H3
2818 I6
2819 A2
2820 B2
2821 B4
2822 C4
2823 D14
2827 F2
2831 A3
2832 A4
3800 B4
3801 A7
3802 A8
3803 A8
3804 A9
3805 A9
3807 A2
3808 A7
3809 B4
3810 A2
3811 A4
3812 B6
3813 A4
3814 I13
3815 A2
3816 B8
3817 B9
3818 B9
3819 B9
3820 B6
3821 B5
3822 A1
3823 B10
3824 C4
3825 C5
3826 A10
3828 A10
3829 B2
3830 E6
3831 C4
3832 C1
3833 B12
3834 B12
3835 B6
3836 B11
3837 B2
3838 B4
3839 C6
3840 C10
3841 C11
3842 B4
3843 D5
3844 D10
3845 D5
3846 D11
3847 D10
3848 D3
3849 D4
3850 D2
3851 D4
3852 D1
3853 D1
3854 C2
3855 E3
3856 B7
3857 F4
3858 E1
3859 E2
3860 E6
3861 G5
3862 F3
3863 F10
3864 F10
3865 E10
3866 E5
3867 G8
3868 G9
3869 G9
3870 G9
3871 B8
3872 G5
3873 G6
3874 G7
3875 H13
3876 H3
3877 H5
3878 I4
3879 F6
3880 H8
3881 I5
3882 I1
3883 H3
3884 G7
3885 G9
3886 I4
3887 I2
3888 I1
3889 D11
3890 G11
3891 D6
3892 D6
3893 D5
3894 E1
3895 F2
3896 F6
3897 G8
3898 G2
3899 D11
3914 C14
3915 C13

3916 F11
3917 F11
4801 D13
4906 G2
6801 A7
6802 A3
6803 B3
6805 F6
6807 F13
7800-A A2
7800-B B2
7800-C B3
7800-D A3
7801 A7
7803-B D8
7804 D1
7805 D3
7806 E2
7807 F5
7809 F4
7810 H1
7811 H7
7812 I3
7813 I5
7815 B13
7816 A3
7817 B3
F800 C10
F8001 A10
F8002 A10
F8003 A11
F8004 A11
F8005 A11
F8006 A11
F8007 A11
F8008 A11
F801 A1
F802 B1
F803 H5
F804 G5
F808 I10
F810 A9
F8101 D13
F8102 E13
F8103 E13
F8104 E13
F8105 E13
F8106 E13
F8107 E13
F8108 E13
F8109 F13
F811 A9
F8110 F13
F8111 F13
F8112 D13
F812 F6
F8201 H13
F8202 H13
F8203 H13
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F8206 H13
F8207 H13
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F8209 I13
F8210 I13
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I841 C10
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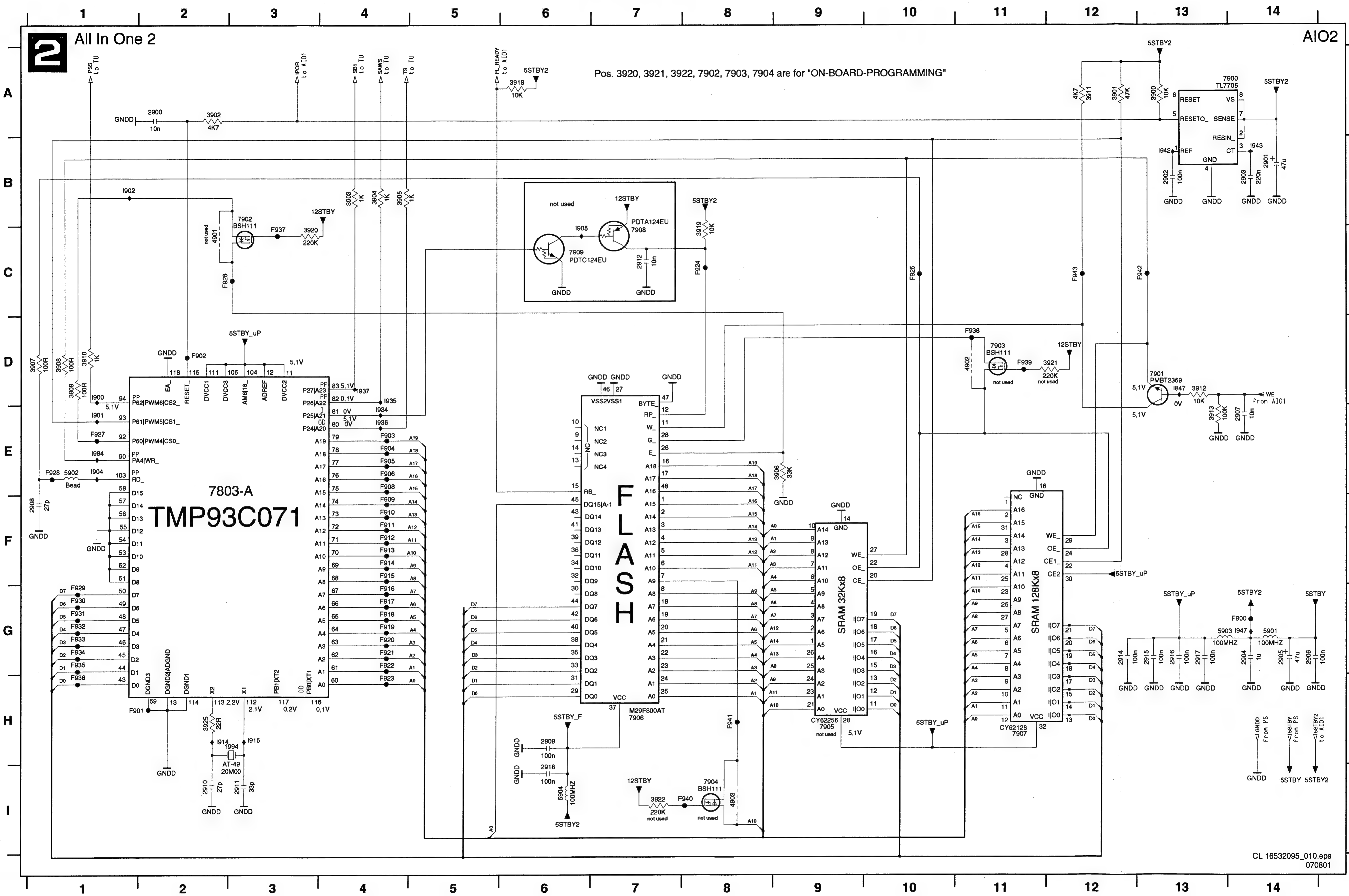
I882 H3
I885 H2
I886 G1

I887 I1
I888 I1
I890 D1
I891 D2
I892 F14
I893 E2
I894 D2
I896 F3
I897 F4
I898 F5
I899 F2
I903 F11
I945 B13
I946 C14
I948 D10
I970 E7
I971 D6
I972 C6
I973 E6
I974 D6
I975 D3
I976 D6
I977 C6
I978 C6
I979 C6
I980 C6
I981 C6
I982 A7
I983 F11

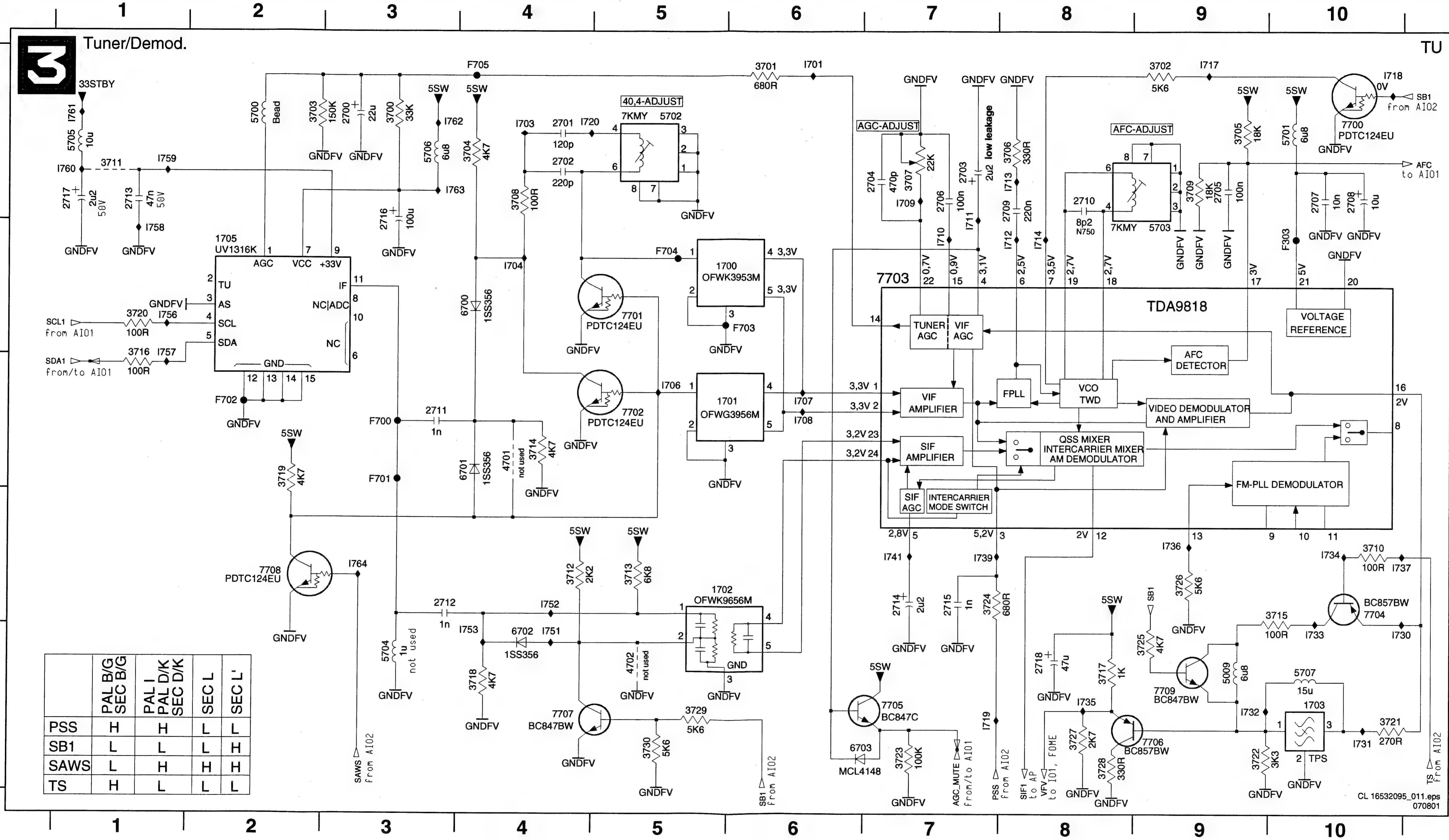
Analog Board: All in One 2



1994	H3
2900	A2
2901	B14
2902	B13
2903	B14
2904	G14
2905	G14
2906	G14
2907	E14
2908	F1
2909	H6
2910	I2
2911	I3
2912	C7
2914	G12
2915	G13
2916	G13
2917	G13
2918	I6
3900	A13
3901	A12
3902	A2
3903	B4
3904	B4
3905	B4
3906	E9
3907	D1
3908	D1
3909	D1
3910	D1
3911	A12
3912	D13
3913	E13
3918	A6
3919	C8
3920	C3
3921	D12
3922	I7
3925	H2
4901	C2
4902	D11
4903	I8
5901	G14
5902	E1
5903	G13
5904	I6
7803-A	E2
7900	A14
7901	D13
7902	B3
7903	D11
7904	I8
7905	H9
7906	H7
7907	H11
7908	C7
7909	C6
F900	G14
F901	H1
F902	D2
F903	E4
F904	E4
F905	E4
F906	E4
F908	E4
F909	F4
F910	F4
F911	F4
F912	F4
F913	F4
F914	F4
F915	F4
F916	G4
F917	G4
F918	G4
F919	G4
F920	G4
F921	G4
F922	G4
F923	H4
F924	C8
F925	C10
F926	C2
F927	E1
F928	E1
F929	G1
F930	G1
F931	G1
F932	G1
F933	G1
F934	G1
F935	G1
F936	H1
F937	C3
F938	D11
F939	D11
F940	I8
F941	H8
F942	C13
F943	C12
I847	D13
I900	D1
I901	E1
I902	B1
I904	E1
I905	C6
I914	H2
I915	H3
I934	E4
I935	D4
I936	E4
I937	D4
I942	B13
I943	B14
I947	G14
I984	E1

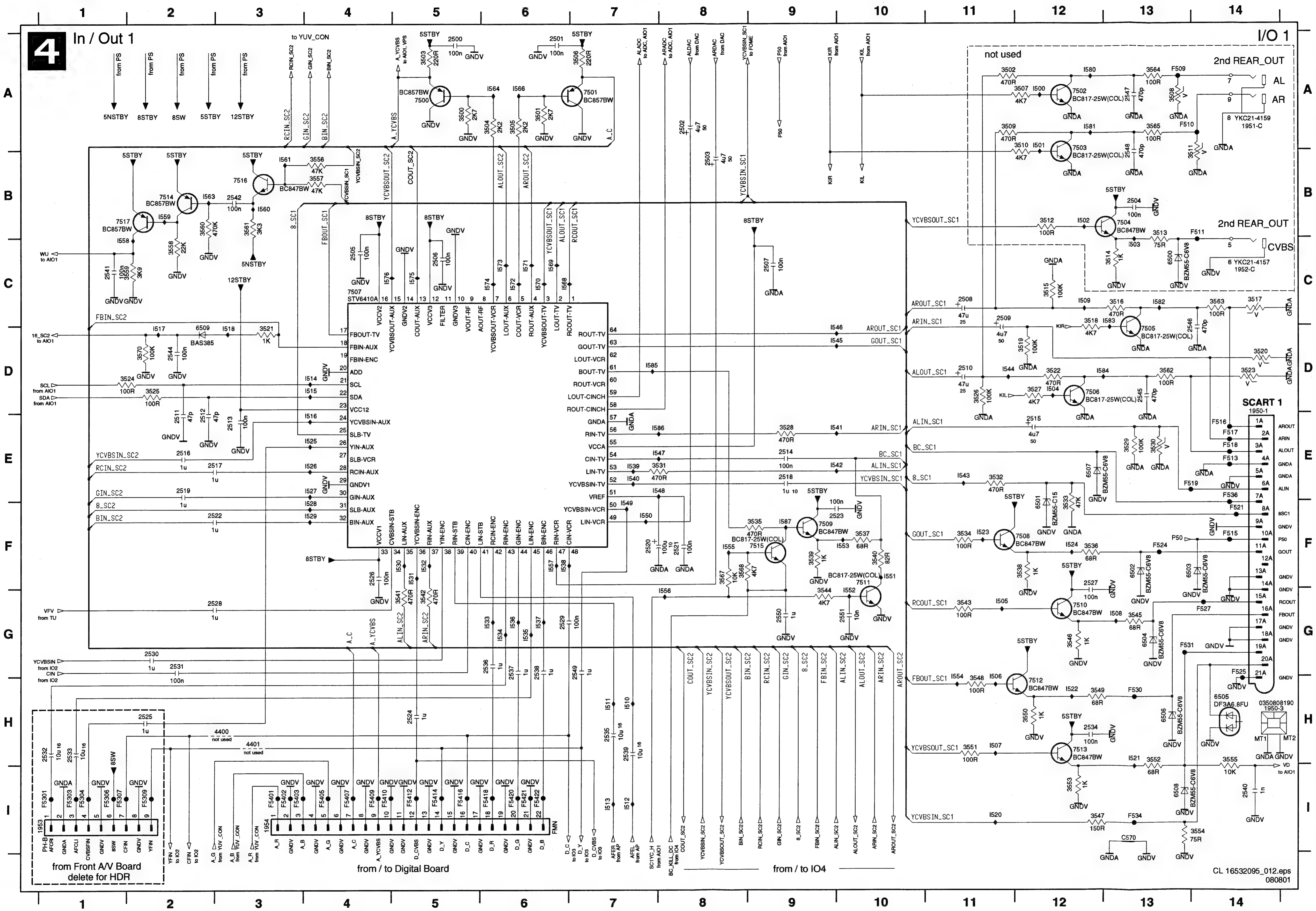
Analog Board: Tuner / Demodulator

1700 B5	2700 A3	2705 A9	2710 A8	2715 D7	3701 A6	3706 A8	3711 A1	3716 C1	3721 E10	3726 D9	4701 C4	5702 A5	5707 E10	7700 A10	7705 E7	F303 B10	F704 B5	I706 C5	I711 A7	I718 A10	I732 E9	I737 D10	I753 E4	I760 A1
1701 C5	2701 A4	2706 A7	2711 C3	2716 A3	3702 A9	3707 A7	3712 D4	3717 E8	3722 E9	3727 E8	4702 E5	5703 B9	6700 B4	7701 B5	7706 E9	F700 C3	F705 A4	I707 C6	I712 B8	I719 E7	I733 E10	I739 D7	I756 B1	I761 A1
1702 D5	2702 A4	2707 A10	2712 D3	2717 A1	3703 A2	3708 A4	3713 D5	3718 E4	3723 E7	3728 E8	5009 E9	5704 E3	6701 C4	7702 C5	7707 E4	F701 C3	I701 A6	I708 C6	I713 A8	I720 A4	I734 D10	I741 D7	I757 B1	I762 A3
1703 E10	2703 A7	2708 A10	2713 A1	2718 E8	3704 A4	3709 A9	3714 C4	3719 C2	3724 D7	3729 E5	5700 A2	5705 A1	6702 E4	7703 B7	7708 D2	F702 C2	I703 A4	I709 A7	I714 B8	I730 E10	I735 E8	I751 E4	I758 B1	I763 A3
1705 B2	2704 A7	2709 A8	2714 D7	3700 A3	3705 A9	3710 D10	3715 D10	3720 B1	3725 E9	3730 E5	5701 A10	5706 A3	6703 E6	7704 D10	7709 E9	F703 B6	I704 B4	I710 B7	I717 A9	I731 E10	I736 D9	I752 D4	I759 A1	I764 D3



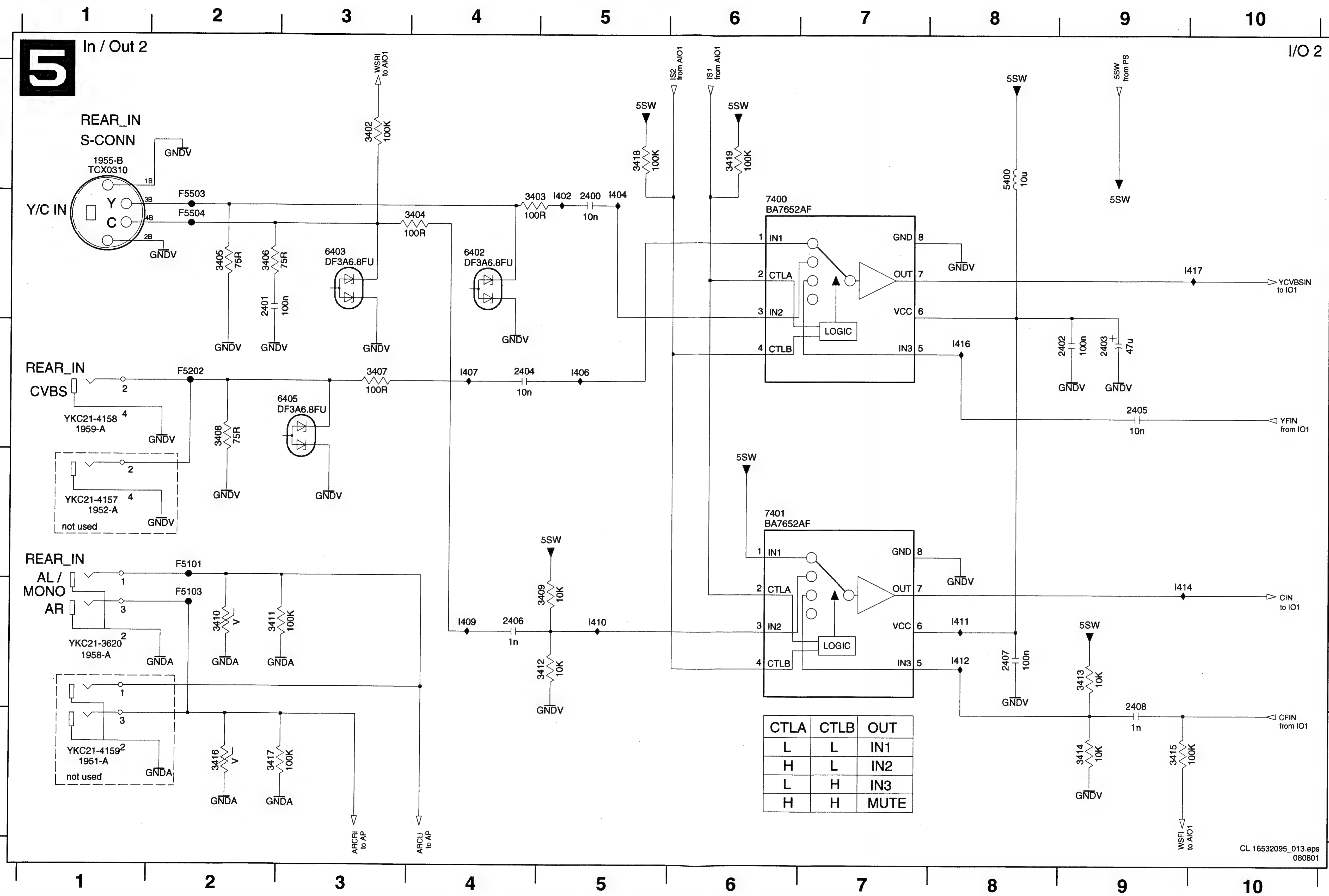
	PAL B/G SEC B/G	PAL I PAL D/K SEC D/K	SEC L	SEC L'
PSS	H	H	L	L
SB1	L	L	L	H
SAWS	L	H	H	H
TS	H	L	L	L

Analog Board: In / Out 1



1950-1 E14	3560 B2	I541 E9
1950-3 H14	3561 B3	I542 E9
1951-C A14	3562 D13	I543 E11
1952-C C14	3563 C14	I544 D11
1953 I1	3564 A13	I545 D9
1954 I3	3565 A13	I546 D9
2500 A5	3567 F8	I547 E7
2501 A6	3568 F8	I548 E7
2502 A8	3570 D2	I549 F7
2503 B8	4400 H3	I550 F7
2504 B13	4401 H3	I551 F10
2505 C4	6500 C13	I552 G10
2506 C5	6501 F12	I553 F10
2507 C9	6502 F13	I554 H11
2508 C11	6503 F13	I555 G8
2509 C11	6504 G13	I556 F8
2510 D11	6505 H14	I557 F6
2511 E2	6506 H13	I558 C1
2512 E2	6507 E12	I559 B2
2513 E3	6508 I13	I560 B3
2514 E9	6509 D2	I561 B3
2515 E12	7500 A5	I563 B2
2516 E2	7501 A7	I564 A6
2517 E2	7502 A12	I566 A6
2518 E9	7503 B12	I568 C6
2519 E2	7504 B13	I569 C6
2520 F7	7505 D13	I570 C6
2521 F8	7506 D12	I571 C6
2522 F2	7507 C4	I572 C6
2523 F9	7508 F12	I573 C6
2524 H5	7509 F9	I574 C6
2525 H2	7510 G12	I575 C5
2526 F4	7511 F10	I576 C4
2527 F12	7512 H12	I580 A12
2528 G2	7513 H12	I581 A12
2529 G6	7514 B2	I582 C13
2530 G2	7515 F9	I583 C13
2531 G2	7516 B3	I584 D12
2532 H1	7517 B2	I585 D7
2533 H1	C570 I13	I586 E7
2534 H12	F509 A13	I587 F9
2535 H7	F510 A13	
2536 G6	F511 B14	
2537 G6	F513 E14	
2538 G6	F515 F14	
2539 H7	F516 E14	
2540 I14	F517 E14	
2541 C1	F518 E14	
2542 B3	F519 E13	
2544 D2	F521 F14	
2545 D13	F524 F13	
2546 D14	F525 G14	
2547 A13	F527 G14	
2548 B13	F530 H13	
2549 G7	F5301 I1	
2550 G9	F5303 I1	
2551 G10	F5304 I1	
3500 A5	F5306 I1	
3501 A6	F5307 I1	
3502 A11	F5309 I2	
3503 A5	F531 G13	
3504 A6	F534 I13	
3505 A6	F536 E14	
3506 A7	F5401 I3	
3507 A12	F5402 I3	
3508 A13	F5403 I3	
3509 A11	F5405 I4	
3510 A12	F5407 I4	
3511 B14	F5409 I4	
3512 B12	F5410 I4	
3513 B13	F5412 I5	
3514 C13	F5414 I5	
3515 C12	F5416 I5	
3516 C13	F5418 I6	
3517 C14	F5420 I6	
3518 C12	F5421 I6	
3519 D12	F5422 I6	
3520 D14	I500 A12	
3521 D3	I501 A12	
3522 D12	I502 B12	
3523 D14	I503 C13	
3524 D2	I504 D12	
3525 D2	I505 G11	
3526 D11	I506 H11	
3527 D12	I507 H11	
3528 E9	I508 G13	
3529 E13	I509 C12	
3530 E13	I510 H7	
3531 E8	I511 H7	
3532 E11	I512 I7	
3533 F12	I513 I7	
3534 F11	I514 D4	
3535 F9	I515 D4	
3536 F12	I516 E4	
3537 F10	I517 D2	
3538 F12	I518 D3	
3539 F9	I520 I11	
3540 F10	I521 H13	
3541 G5	I522 H12	
3542 G5	I523 F11	
3543 G11	I524 F12	
3544 G9	I525 E4	
3545 G13	I526 E4	
3546 G12	I527 E4	
3547 I12	I528 F4	
3548 H11	I529 F4	
3549 H12	I530 F5	
3550 H12	I531 F5	
3551 H11	I532 F5	
3552 H13	I533 G6	
3553 I12	I534 G6	
3554 I14	I535 G6	
3555 H14	I536 G6	
3556 B4	I537 G6	
3557 B4	I538 F6	
3558 C2	I539 E7	
3559 C2	I540 E7	

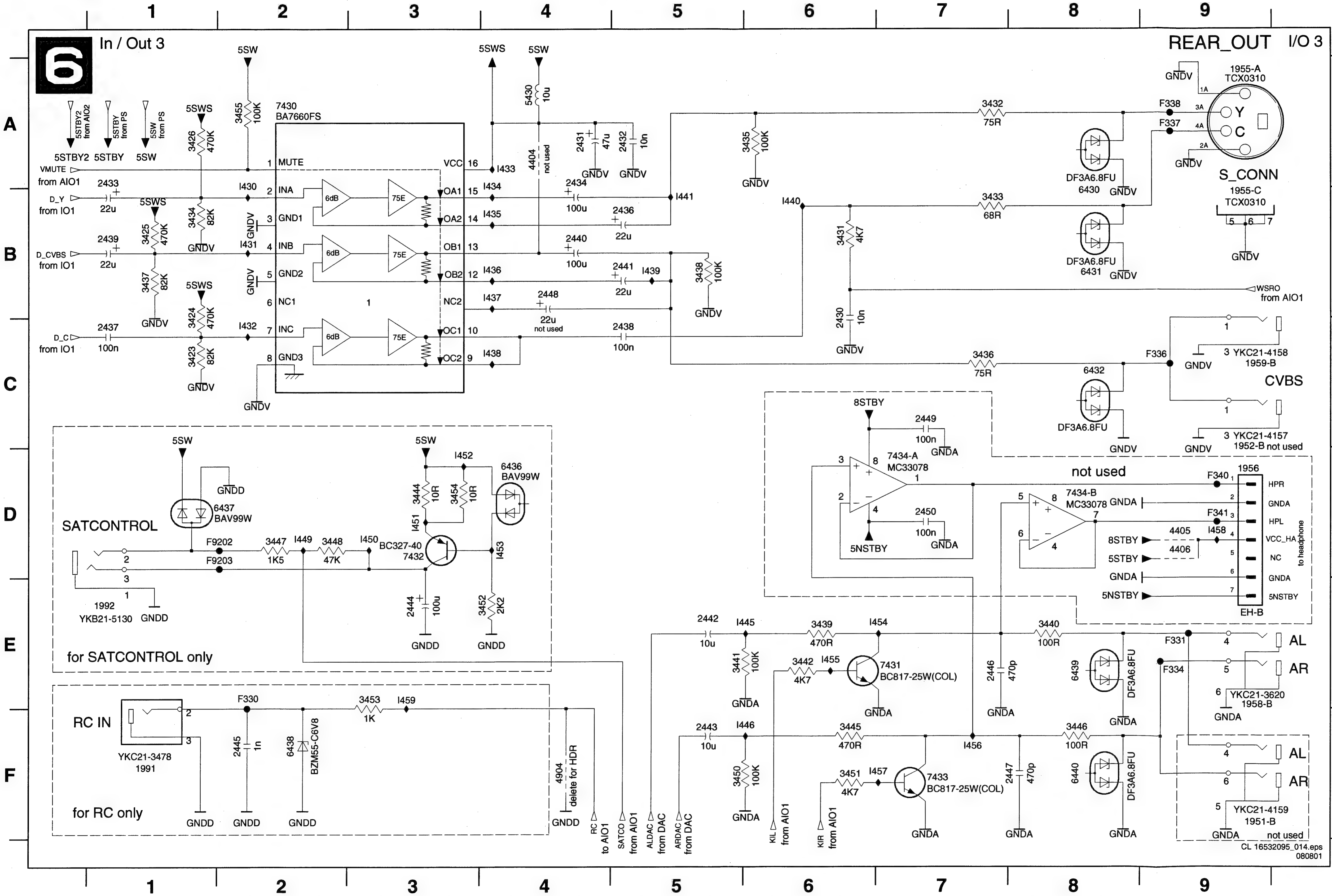
Analog Board: In / Out 2



CTLA	CTLB	OUT
L	L	IN1
H	L	IN2
L	H	IN3
H	H	MUTE

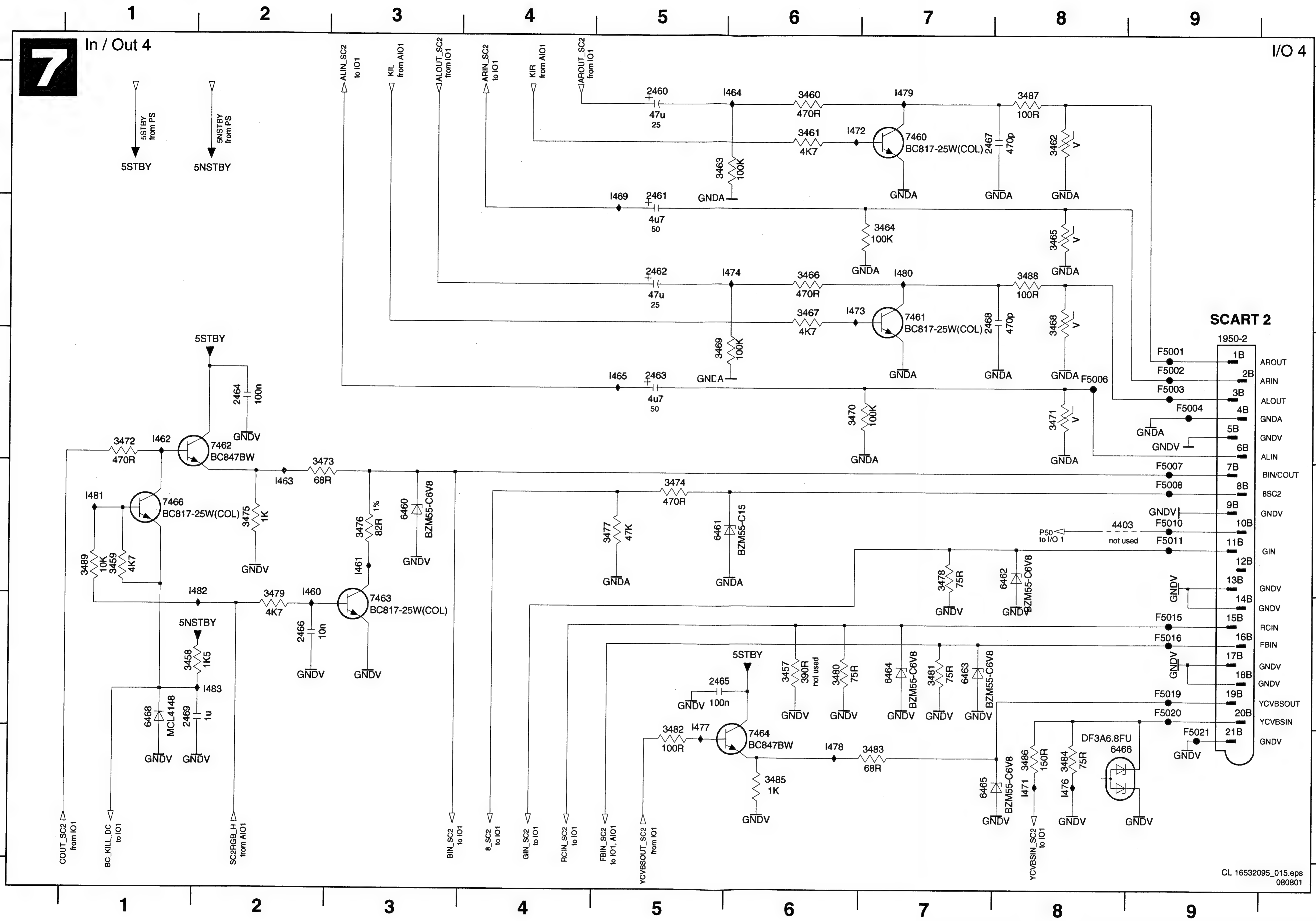
1951-A F1
1952-A D1
1955-B A1
1958-A E1
1959-A C1
2400 B5
2401 B2
2402 C9
2403 C9
2404 C4
2405 C9
2406 E4
2407 E8
2408 E9
3402 A3
3403 B4
3404 B4
3405 B2
3406 B2
3407 C3
3408 C2
3409 E5
3410 E2
3411 E2
3412 E5
3413 E9
3414 F9
3415 F9
3416 F2
3417 F2
3418 A5
3419 A6
5400 A8
6402 B4
6403 B3
6405 C2
7400 B6
7401 D6
F5101 D2
F5103 E2
F5202 C2
F5503 B2
F5504 B2
I402 B5
I404 B5
I406 C5
I407 C4
I409 E4
I410 E5
I411 E8
I412 E8
I414 E9
I416 C8
I417 B10

Analog Board: In / Out 3



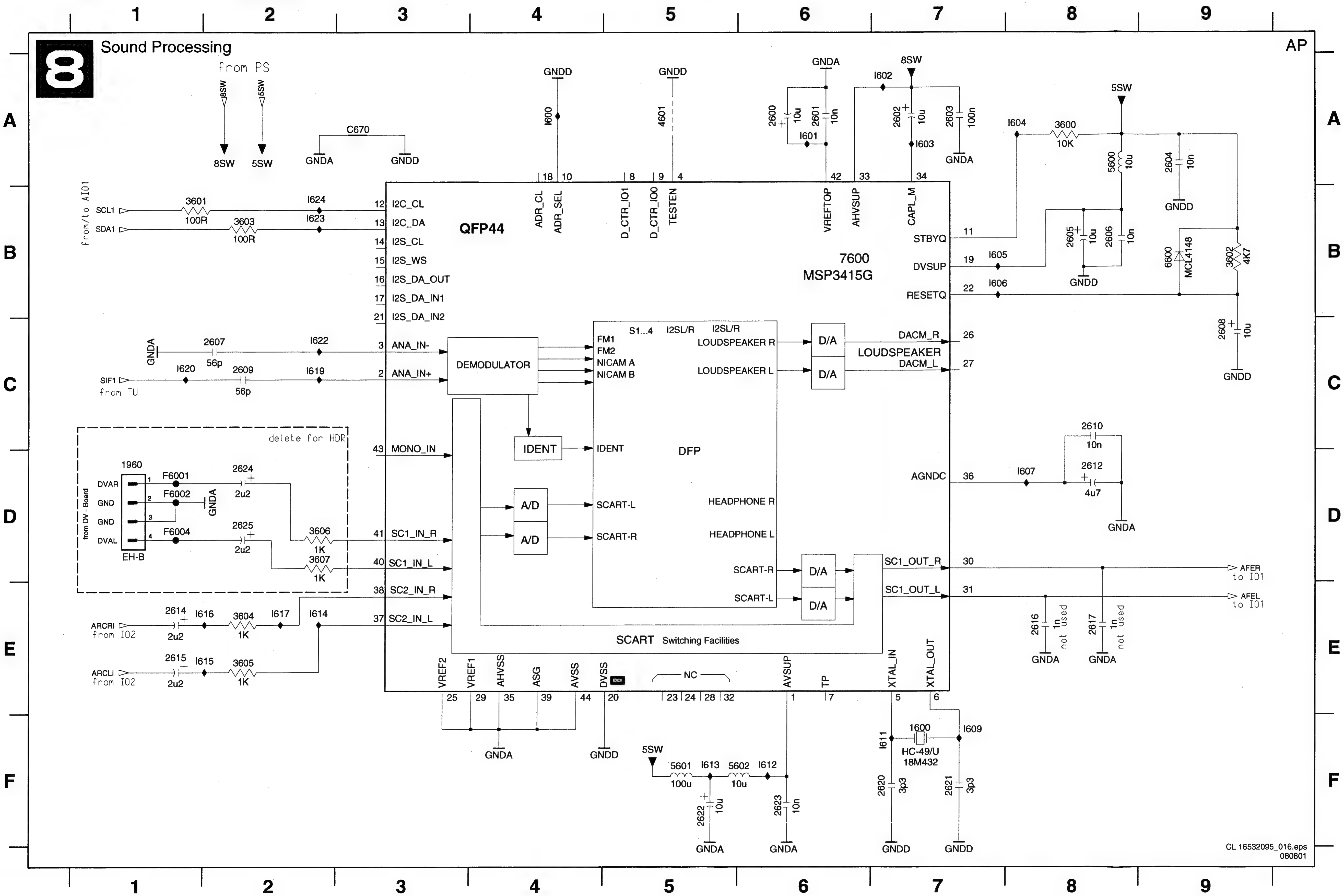
1951-B F9
1952-B C9
1955-A A9
1955-C B9
1956 D9
1958-B E9
1959-B C9
1991 F1
1992 E1
2430 B6
2431 A4
2432 A5
2433 A1
2434 A4
2436 B5
2437 C1
2438 C5
2439 B1
2440 B4
2441 B5
2442 E5
2443 F5
2444 E3
2445 F2
2446 E7
2447 F8
2448 B4
2449 C7
2450 D7
3423 C1
3424 B1
3425 B1
3426 A1
3431 B6
3432 A7
3433 B7
3434 B1
3435 A6
3436 C7
3437 B1
3438 B5
3439 E6
3440 E8
3441 E5
3442 E6
3444 D3
3445 F6
3446 F8
3447 D2
3448 D2
3450 F5
3451 F6
3452 E4
3453 E3
3454 D3
3455 A2
4404 A4
4405 D9
4406 D9
4904 F4
5430 A4
6430 A8
6431 B8
6432 C8
6436 D4
6437 D1
6438 F2
6439 E8
6440 F8
7430 A2
7431 E7
7432 D3
7433 F7
7434-A D7
7434-B D8
F330 E2
F331 E9
F334 E9
F336 C9
F337 A9
F338 A9
F340 D9
F341 D9
F9202 D2
F9203 D2
I430 A2
I431 B2
I432 C2
I433 A4
I434 A4
I435 B4
I436 B4
I437 B4
I438 C4
I439 B5
I440 B6
I441 B5
I445 E6
I446 F6
I449 D2
I450 D3
I451 D3
I452 D3
I453 D4
I454 E7
I455 E6
I456 F7
I457 F7
I458 D9
I459 E3

Analog Board: In / Out 4



1950-2 C9
2460 A5
2461 B5
2462 B5
2463 C5
2464 C2
2465 E6
2466 E2
2467 A7
2468 B7
2469 E2
3457 E6
3458 E2
3459 D1
3460 A6
3461 A6
3462 A8
3463 A5
3464 B7
3465 B8
3466 B6
3467 B6
3468 B8
3469 C5
3470 C6
3471 C8
3472 C1
3473 D3
3474 D5
3475 D2
3476 D3
3477 D5
3478 D7
3479 E2
3480 E6
3481 E7
3482 F5
3483 F7
3484 F8
3485 F6
3486 F8
3487 A8
3488 B8
3489 D1
4403 D8
6460 D3
6461 D5
6462 D8
6463 E7
6464 E7
6465 F7
6466 F9
6468 E1
7460 A7
7461 B7
7462 C2
7463 E3
7464 F6
7466 D1
F5001 C9
F5002 C9
F5003 C9
F5004 C9
F5006 C8
F5007 D9
F5008 D9
F5010 D9
F5011 D9
F5015 E9
F5016 E9
F5019 E9
F5020 E9
F5021 F9
I460 D2
I461 D3
I462 C1
I463 D2
I464 A6
I465 C5
I469 A5
I471 F8
I472 A7
I473 B7
I474 B6
I476 F8
I477 E5
I478 F6
I479 A7
I480 B7
I481 D1
I482 D2
I483 E2

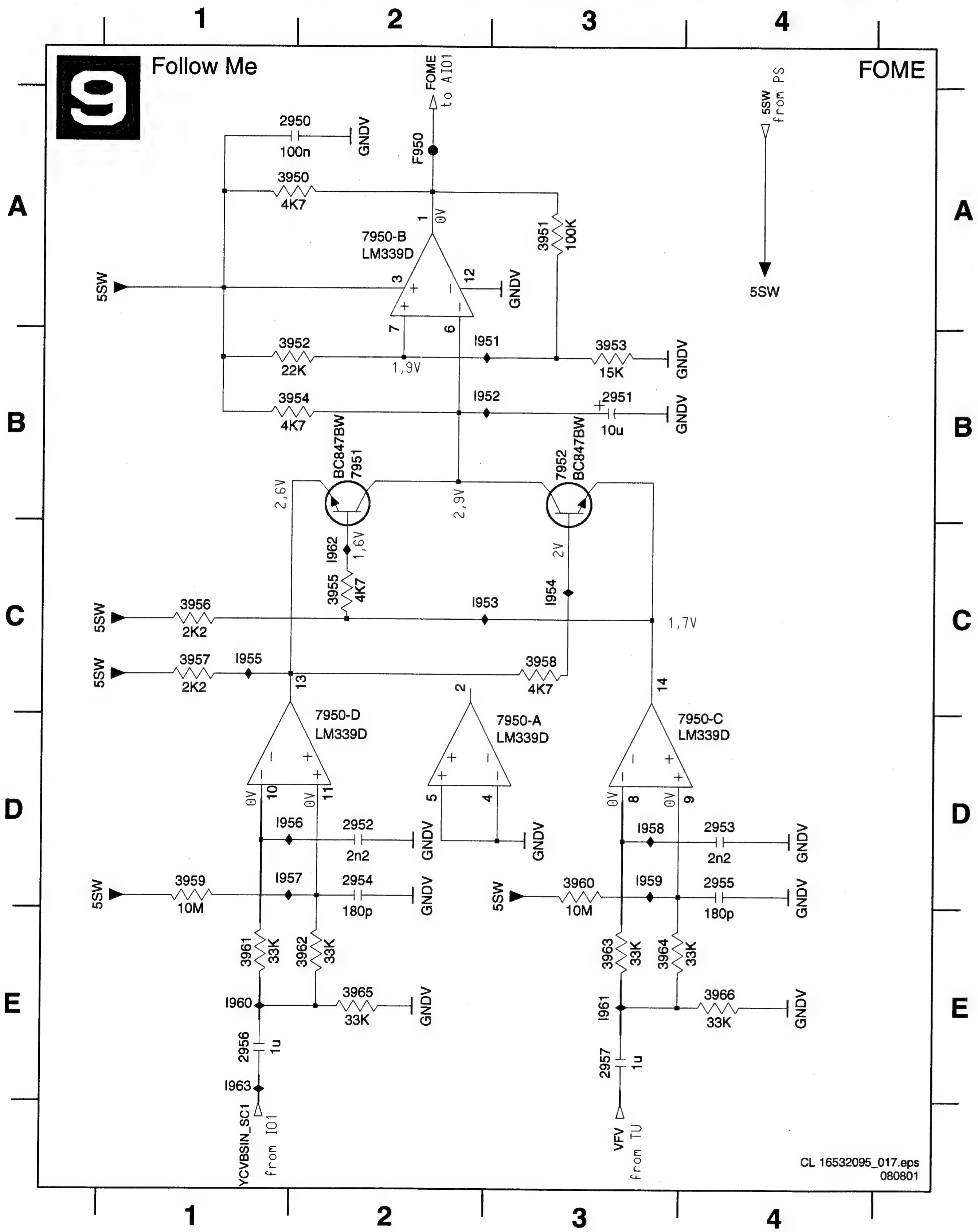
Analog Board: Sound Processing



1600	F7
1960	D1
2600	A6
2601	A6
2602	A7
2603	A7
2604	A9
2605	B8
2606	B8
2607	C2
2608	C9
2609	C2
2610	C8
2612	D8
2614	E1
2615	E1
2616	E8
2617	E8
2620	F7
2621	F7
2622	F5
2623	F6
2624	D2
2625	D2
3600	A8
3601	B1
3602	B9
3603	B2
3604	E2
3605	E2
3606	D2
3607	D2
4601	A5
5600	A8
5601	F5
5602	F6
6600	B9
7600	B6
C670	A3
F6001	D1
F6002	D1
F6004	D1
I600	A4
I601	A6
I602	A7
I603	A7
I604	A8
I605	B7
I606	B7
I607	D8
I609	F7
I611	F7
I612	F6
I613	F5
I614	E2
I615	E2
I616	E2
I617	E2
I619	C2
I620	C1
I622	C2
I623	B2
I624	B2

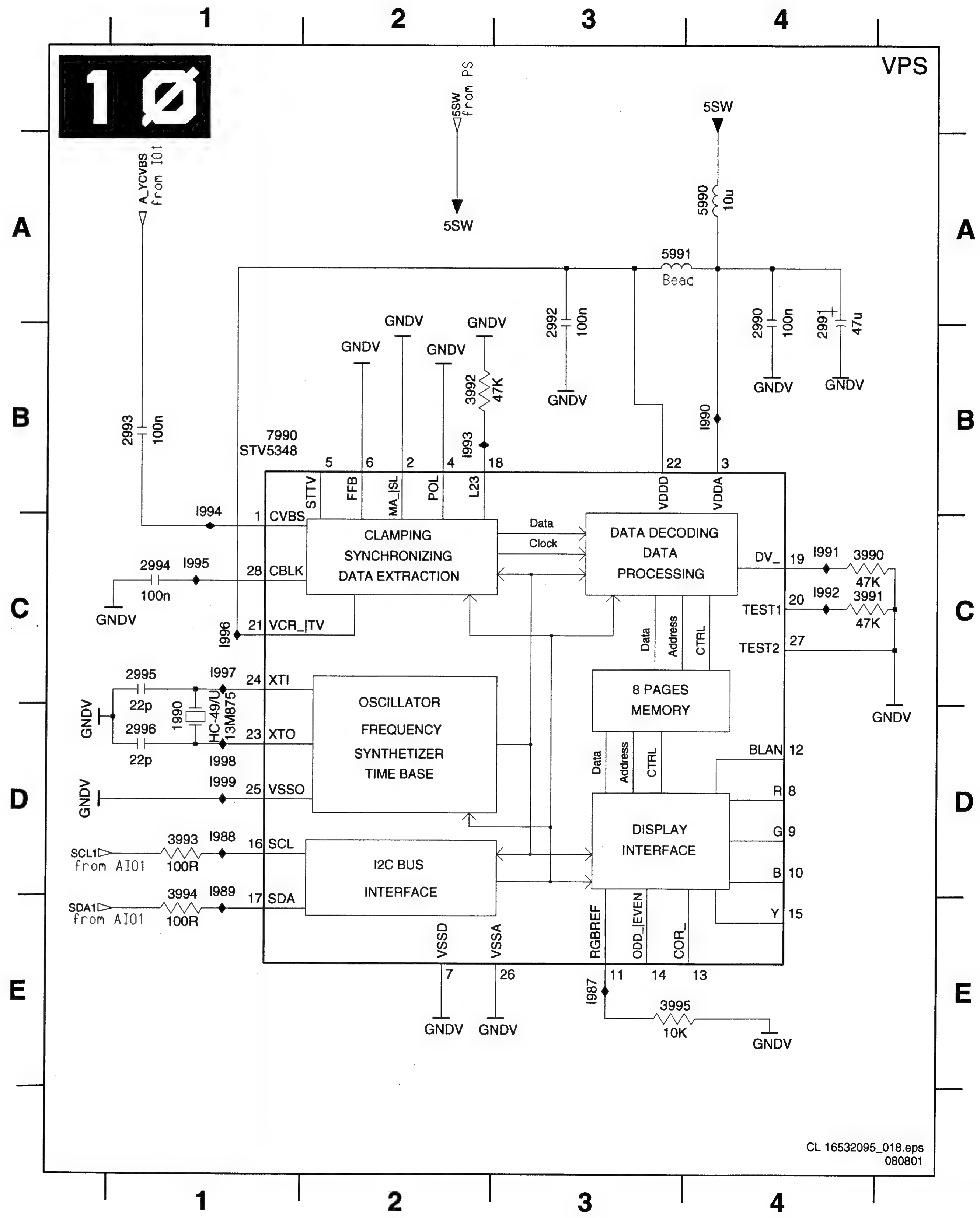
Analog Board: Follow Me

2950 A1	2954 D2	3950 A1	3954 B1	3958 C3	3962 E2	3966 E4	7950 D4	I951 B2	I955 C1	I959 D3	I963 E1
2951 B3	2955 D4	3951 A3	3955 C2	3959 D1	3963 E3	7950 A2	7951 B2	I952 B2	I956 D1	I960 E1	
2952 D2	2956 E1	3952 B1	3956 C1	3960 D3	3964 E3	7950 D2	7952 B3	I953 C2	I957 D1	I961 E3	
2953 D4	2957 E3	3953 B3	3957 C1	3961 E1	3965 E2	7950 D2	F950 A3	I954 C3	I958 D3	I962 C2	

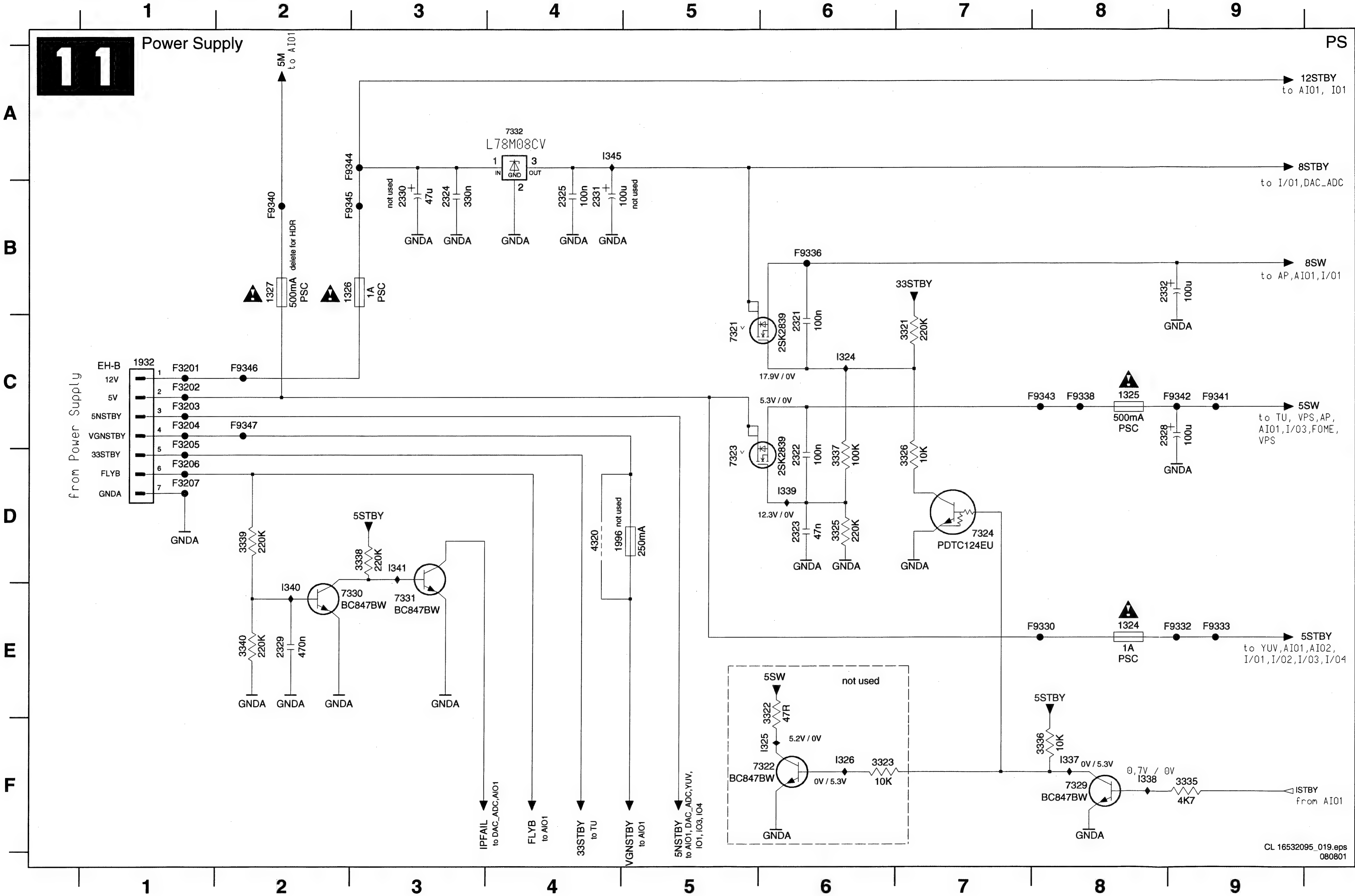


Analog Board: VPS

1990 D1	2992 A3	2995 C1	3991 C4	3994 E1	5991 A3	I988 D1	I991 C4	I994 B1	I997 C1
2990 A4	2993 B1	2996 D1	3992 B2	3995 E3	7990 B1	I989 D1	I992 C4	I995 C1	I998 D1
2991 A4	2994 C1	3990 C4	3993 D1	5990 A4	I987 E3	I990 B4	I993 B2	I996 C1	I999 D1

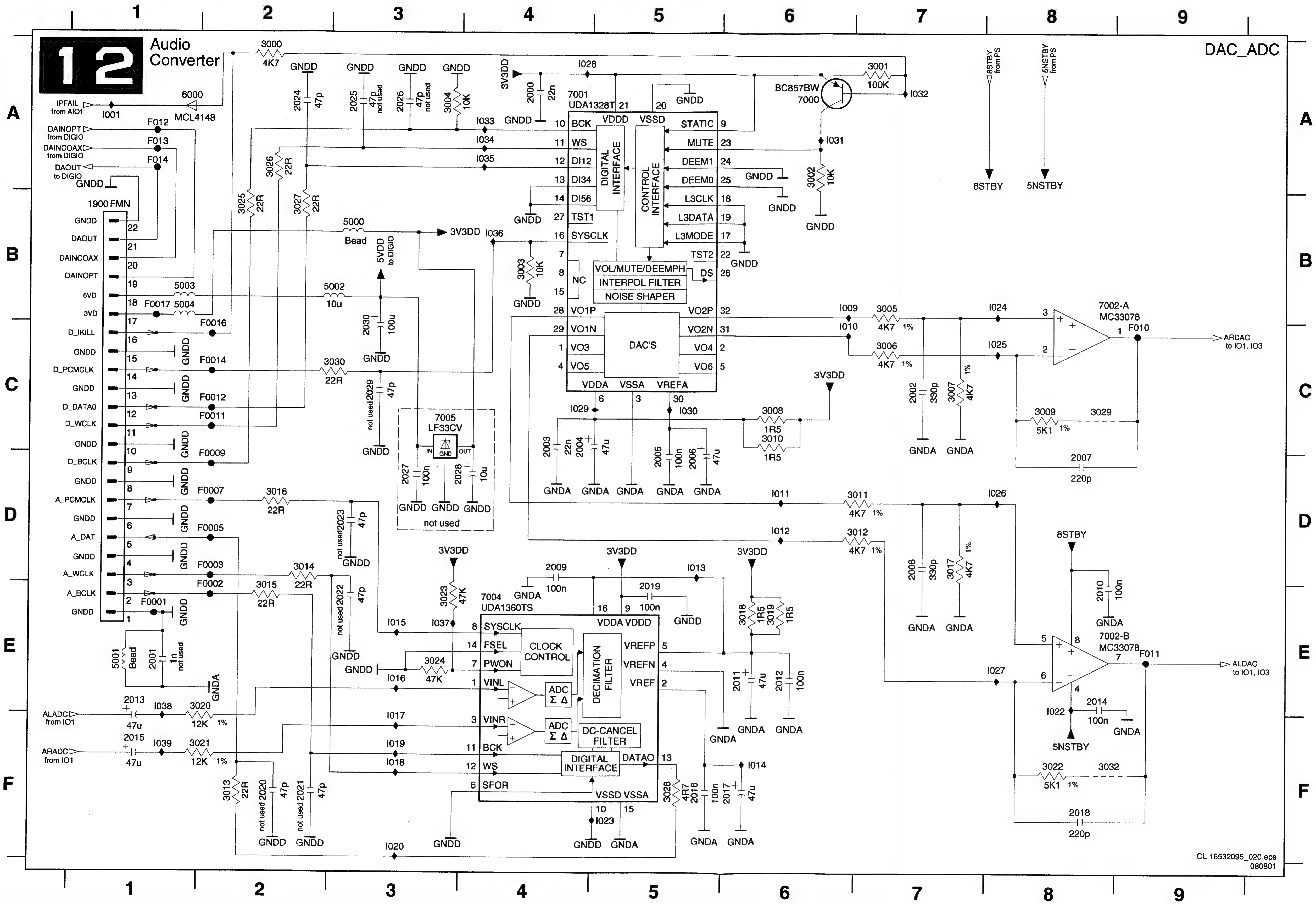


Analog Board: Power Supply



1324 E8
1325 C8
1326 B2
1327 B2
1932 C1
1996 D4
2321 C6
2322 D6
2323 D6
2324 B3
2325 B4
2328 C8
2329 E2
2330 B3
2331 B4
2332 B8
3321 C7
3322 E6
3323 F6
3325 D6
3326 D7
3335 F9
3336 F8
3337 D6
3338 D3
3339 D2
3340 E2
4320 D4
7321 C5
7322 F6
7323 D5
7324 D7
7329 F8
7330 E2
7331 E3
7332 A4
F3201 C1
F3202 C1
F3203 C1
F3204 C1
F3205 C1
F3206 D1
F3207 D1
F9330 E8
F9332 E9
F9333 E9
F9336 B6
F9338 C8
F9340 B2
F9341 C9
F9342 C9
F9343 C8
F9344 A3
F9345 B3
F9346 C2
F9347 C2
I324 C6
I325 F6
I326 F6
I337 F8
I338 F8
I339 D6
I340 E2
I341 D3
I345 A4

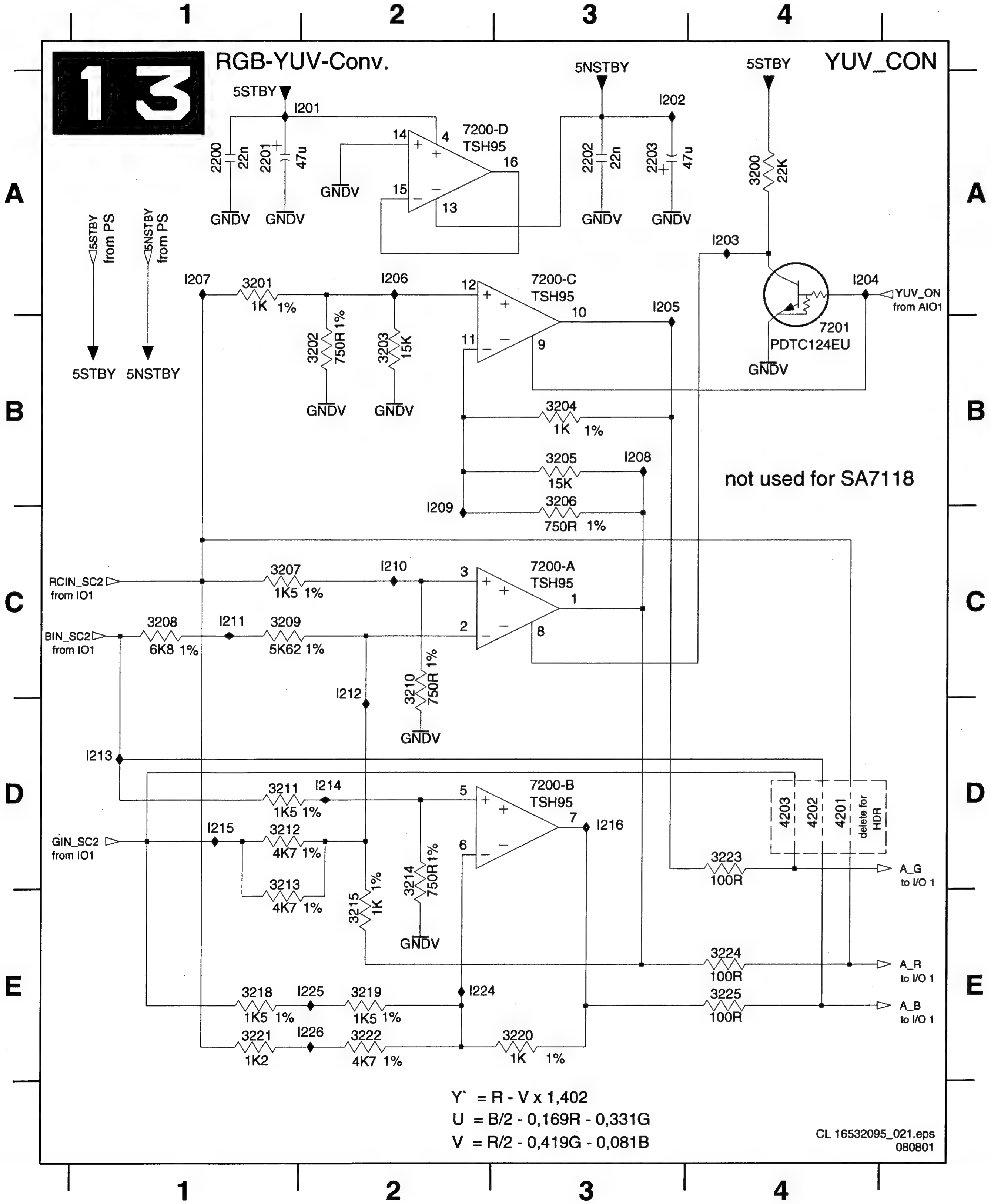
Analog Board: Audio Converter



1900 B1
2000 A4
2001 E1
2002 C7
2003 C4
2004 C4
2005 D5
2006 D5
2007 D8
2008 D7
2009 D4
2010 E8
2011 E6
2012 E6
2013 E1
2014 E8
2015 F1
2016 F5
2017 F6
2018 F8
2019 E5
2020 F2
2021 F2
2022 E3
2023 D3
2024 A2
2025 A3
2026 A3
2027 D3
2028 D4
2029 C3
2030 C3
3000 A2
3001 A7
3002 A6
3003 B4
3004 A3
3005 B7
3006 C7
3007 C7
3008 C6
3009 C8
3010 C6
3011 D7
3012 D7
3013 F2
3014 D2
3015 E2
3016 D2
3017 D7
3018 E6
3019 E6
3020 E2
3021 F2
3022 F8
3023 E3
3024 E3
3025 B2
3026 A2
3027 B2
3028 F5
3029 C8
3030 C3
3032 F8
5000 B3
5001 E1
5002 B3
5003 B1
5004 B1
6000 A1
7000 A6
7001 A4
7002-A B8
7002-B E8
7004 E4
7005 C3
F0001 E1
F0002 E2
F0003 D2
F0005 D2
F0007 D2
F0009 D2
F0011 C2
F0012 C2
F0014 C2
F0016 C2
F0017 B1
F010 C9
F011 E9
F012 A1
F013 A1
F014 A1
I001 A1
I009 B6
I010 C6
I011 D6
I012 D6
I013 D5
I014 F6
I015 E3
I016 E3
I017 F3
I018 F3
I019 F3
I020 F3
I022 E8
I023 F5
I024 B8
I025 C8
I026 D8
I027 E8
I028 A4
I029 C4
I030 C5
I031 A6
I032 A7
I033 A4
I034 A4
I035 A4
I036 B4
I037 E3
I038 E1
I039 F1

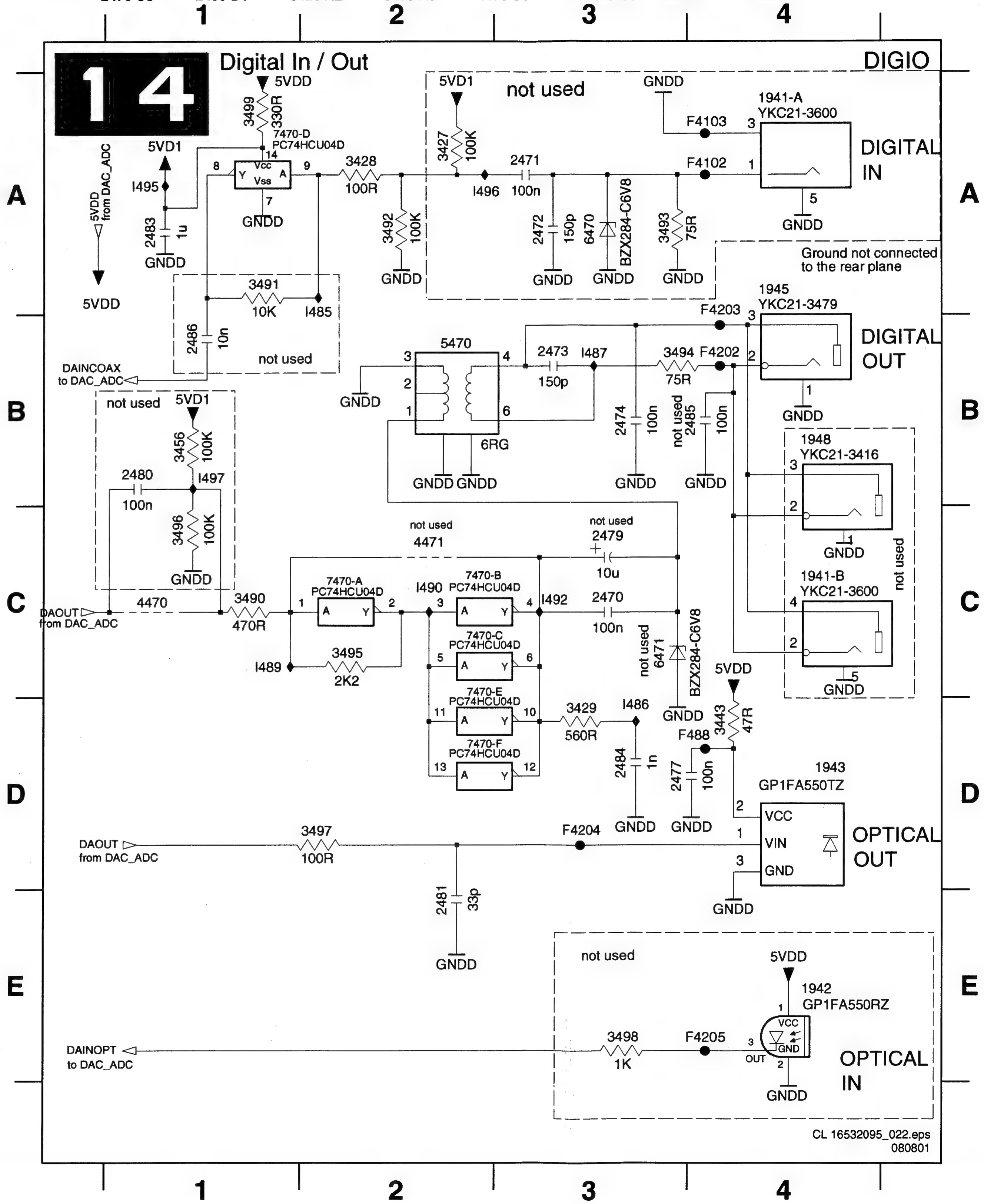
Analog Board: RGB-YUV-Converter

2200 A1	3202 B2	3208 C1	3214 D2	3222 E2	4203 D4	I201 A2	I207 A1	I213 D1	I226 E2
2201 A1	3203 B2	3209 C1	3215 E2	3223 D4	7200-A C3	I202 A3	I208 B3	I214 D2	
2202 A3	3204 B3	3210 C2	3218 E1	3224 E4	7200-B D3	I203 A4	I209 C2	I215 D1	
2203 A3	3205 B3	3211 D1	3219 E2	3225 E4	7200-C A3	I204 A4	I210 C2	I216 D3	
3200 A4	3206 B3	3212 D1	3220 E3	4201 D4	7200-D A2	I205 A3	I211 C1	I224 E2	
3201 A1	3207 C1	3213 D1	3221 E1	4202 D4	7201 B4	I206 A2	I212 C2	I225 E2	



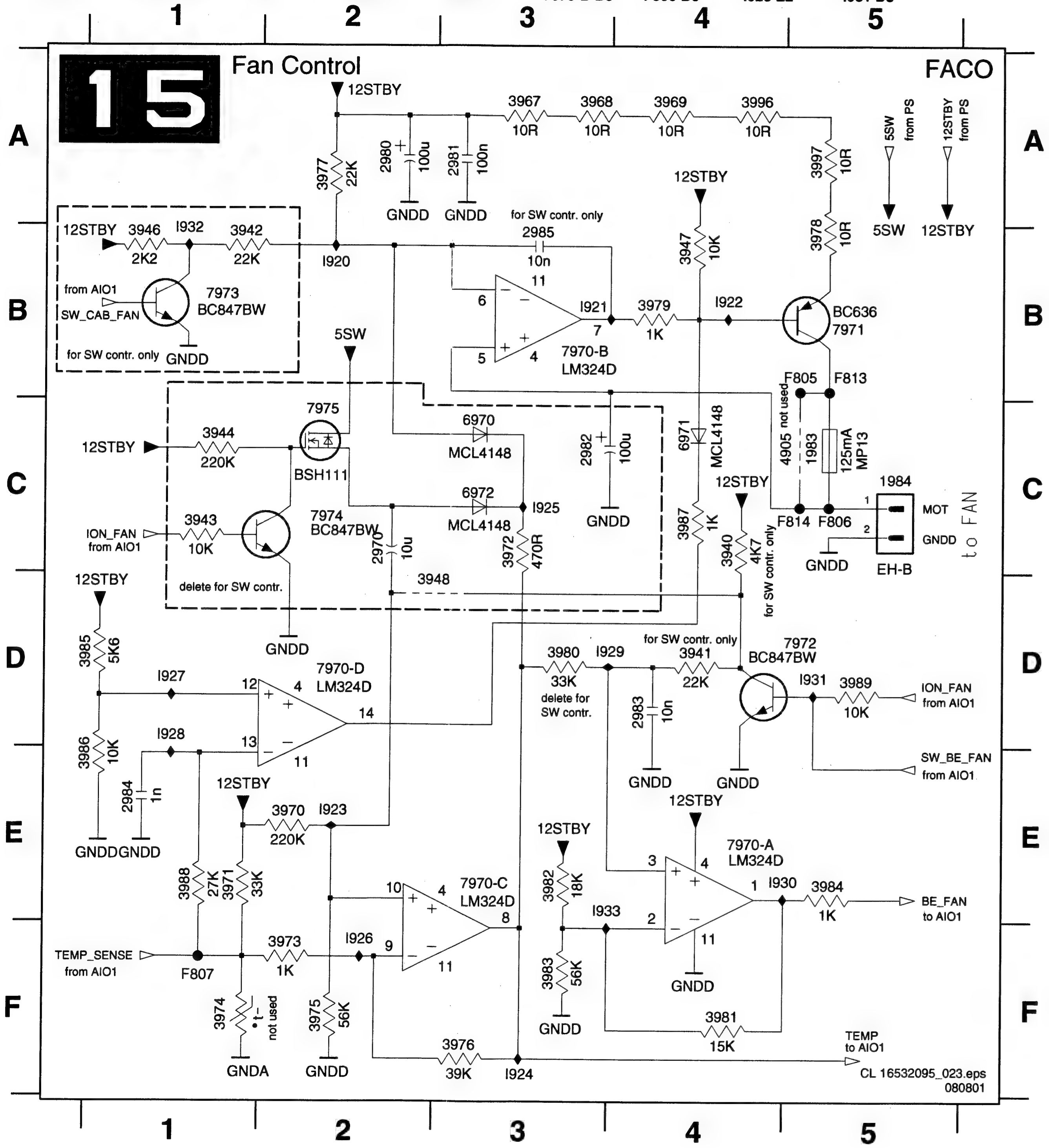
Analog Board: Digital In / Out

1941-A A4	2471 A3	2481 E2	3429 D3	3494 B3	4471 C2	7470-D A1	F4204 D3	I490 C2
1941-B C4	2472 A3	2483 A1	3443 D4	3495 C2	5470 B2	7470-E C2	F4205 E4	I492 C3
1942 E4	2473 B3	2484 D3	3456 B1	3496 C1	6470 A3	7470-F D2	F488 D4	I495 A1
1943 D4	2474 B3	2485 B4	3490 C1	3497 D2	6471 C3	F4102 A4	I485 A2	I496 A2
1945 A4	2477 D3	2486 B1	3491 A1	3498 E3	7470-A C2	F4103 A4	I486 D3	I497 B1
1948 B4	2479 C3	3427 A2	3492 A2	3499 A1	7470-B C2	F4202 B4	I487 B3	
2470 C3	2480 B1	3428 A2	3493 A3	4470 C1	7470-C C2	F4203 A4	I489 C1	



Analog Board: Fan Control

1983 C5	2985 B3	3948 D2	3974 F1	3982 E3	3996 A4	7970-C E3	F806 C5	I924 F3	I932 B1
1984 C5	3940 C4	3967 A3	3975 F2	3983 F3	3997 A5	7970-D D2	F807 F1	I925 C3	I933 E3
2970 C2	3941 D4	3968 A3	3976 F3	3984 E5	4905 C5	7971 B5	F813 B5	I926 F2	
2980 A2	3942 B1	3969 A4	3977 A2	3985 D1	6970 C3	7972 D5	F814 C5	I927 D1	
2981 A3	3943 C1	3970 E2	3978 B5	3986 E1	6971 C4	7973 B1	I920 B2	I928 D1	
2982 C3	3944 C1	3971 E1	3979 B4	3987 C4	6972 C3	7974 C2	I921 B3	I929 D4	
2983 D4	3946 B1	3972 C3	3980 D3	3988 E1	7970-A E4	7975 C2	I922 B4	I930 E4	
2984 E1	3947 B4	3973 F2	3981 F4	3989 D5	7970-B B3	F805 B5	I923 E2	I931 D5	

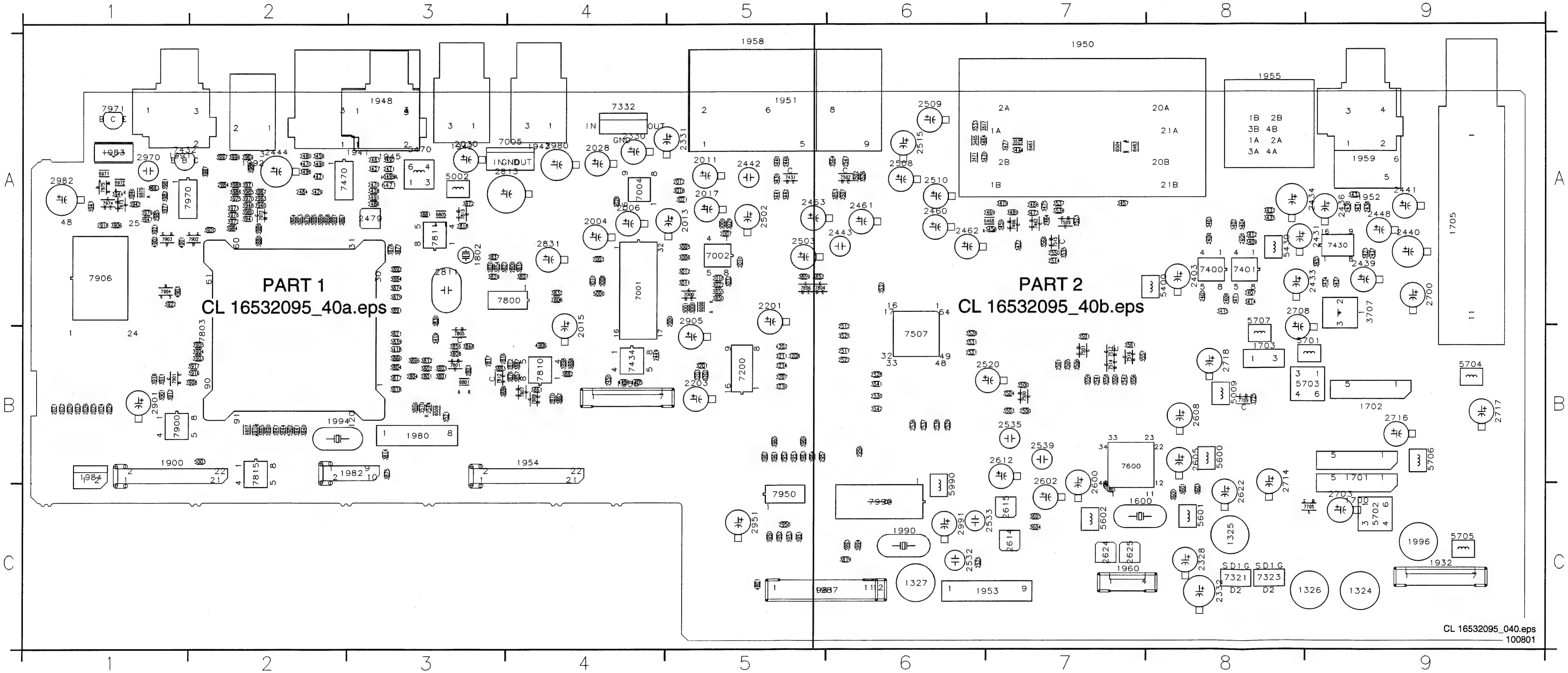


Personal Notes:

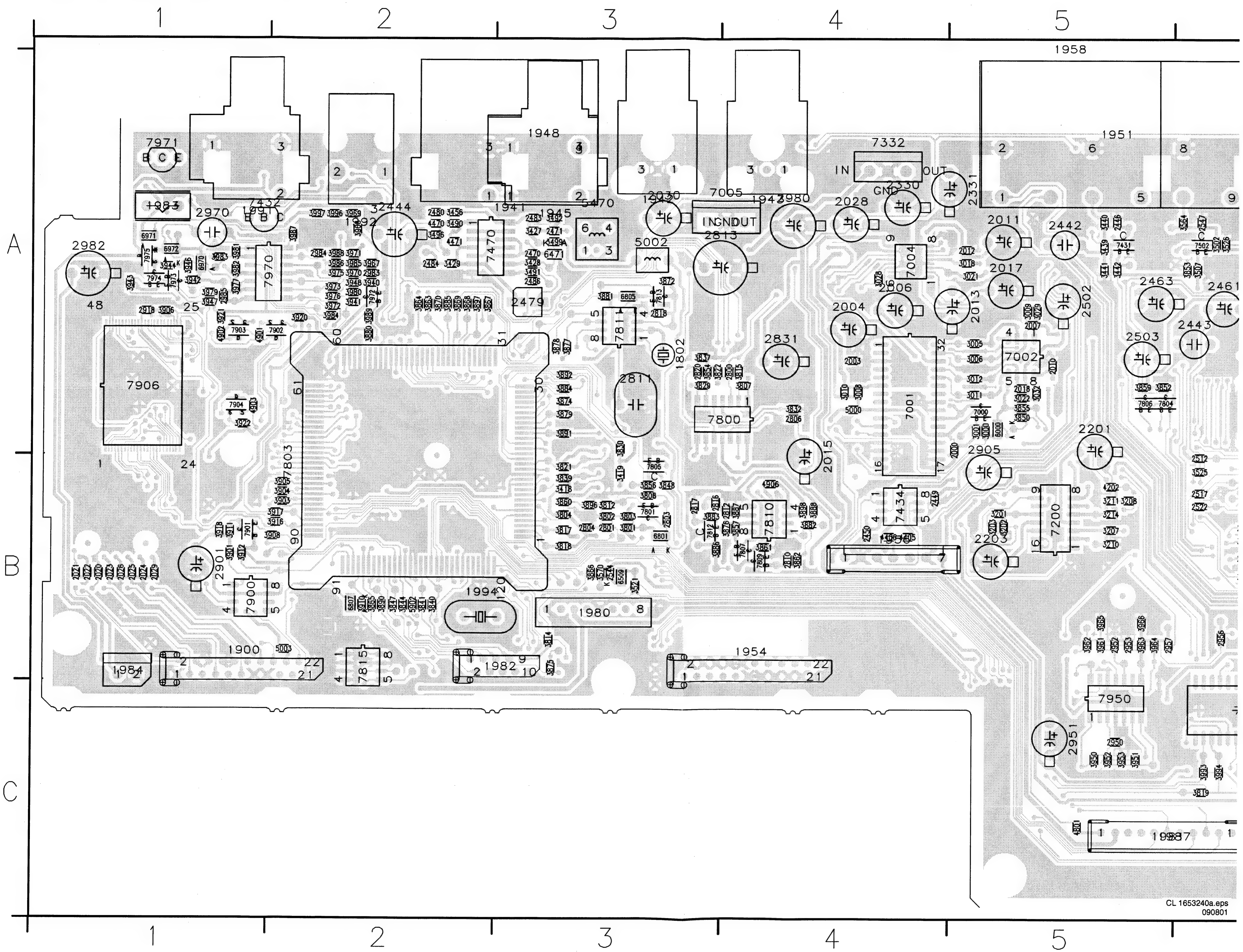
Layout Analog Board (Overview Top View)

1323	C8	1954	B4	2012	A5	2405	A8	2463	A5	2522	B6	2622	C8	2901	B1	3012	A5	3418	B3	3471	A6
1324	C9	1955	A8	2013	A5	2406	A8	2464	A7	2523	A7	2624	C7	2903	A3	3018	A5	3419	B3	3472	A7
1326	C9	1956	B4	2015	B4	2407	A8	2466	A7	2523	C6	2625	C7	2918	A1	3021	A5	3423	A9	3473	A7
1327	C6	1958	A5	2017	A5	2408	A8	2469	A7	2528	B6	2700	A9	2950	C5	3022	A5	3427	A3	3474	A7
1600	C7	1959	A9	2018	A5	2430	A9	2470	A3	2529	B6	2703	C9	2951	C5	3028	A4	3428	A3	3475	A7
1700	C9	1960	C7	2020	B1	2431	A9	2471	A3	2530	B6	2708	A8	2952	B5	3029	A5	3429	A2	3477	A7
1701	B9	1980	B3	2021	B1	2433	A9	2479	A3	2530	A7	2714	B8	2953	B5	3032	A5	3431	A9	3479	A7
1702	B9	1981	C5	2022	B1	2434	A9	2480	A2	2532	C6	2716	B9	2956	B6	3110	C4	3432	A8	3489	A7
1703	B8	1982	B3	2023	B1	2436	A9	2483	A3	2533	C7	2717	B9	2957	B5	3201	B5	3433	A9	3490	A2
1703	A9	1983	A1	2024	B1	2437	A9	2484	A2	2533	B7	2718	B8	2970	A1	3202	B5	3434	A9	3491	A3
1802	A3	1984	B1	2025	B1	2438	A9	2486	A3	2537	B6	2800	A4	2980	A4	3203	B5	3435	A8	3492	A3
1900	B1	1987	C6	2026	B1	2439	A9	2500	B7	2538	B6	2801	B3	2982	A1	3207	B5	3437	A9	3496	A2
1910	C3	1990	C6	2028	A4	2440	A9	2501	B7	2539	B7	2803	B3	2983	A2	3208	B5	3439	A5	3499	A3
1911	C3	1991	A1	2029	B1	2441	A9	2502	A5	2541	B7	2804	B3	2984	A2	3210	B5	3440	A5	3500	B7
1932	C9	1992	A2	2030	A3	2442	A3	2503	A5	2542	B7	2806	A4	2985	A1	3211	B5	3441	A5	3501	B7
1941	A3	1994	B2	2201	A5	2443	A6	2508	A6	2544	B3	2810	B4	2991	C6	3214	B5	3442	A5	3502	A6
1942	A3	1996	C9	2203	B5	2444	A2	2509	A6	2547	A6	2811	A3	3000	A5	3402	A8	3455	A9	3503	B7
1943	A4	2000	A3	2328	C8	2446	A5	2510	A6	2600	B7	2812	B4	3001	A5	3403	A8	3456	A2	3503	B7
1943	A3	2003	A4	2330	A4	2448	A9	2512	B6	2602	B7	2813	A3	3005	A5	3404	A8	3457	A7	3504	B7
1948	A3	2004	A4	2331	A5	2449	B4	2513	A6	2603	B8	2816	B3	3006	A5	3409	A8	3458	A7	3506	B7
1950	A7	2006	A4	2332	C8	2450	B4	2514	A7	2608	B8	2817	B3	3008	A4	3412	A8	3459	A7	3507	A6
1951	A5	2007	A5	2336	B6	2460	A6	2517	B6	2612	B7	2818	A3	3009	A5	3413	A8	3464	A6	3517	A6
1952	A9	2010	A5	2400	A8	2461	A6	2520	B7	2614	C7	2820	A3	3010	A4	3414	A8	3465	A6	3521	B3
1953	C7	2011	A5	2403	A8	2462	A6	2521	B6	2615	C7	2831	A4	3011	A5	3415	A8	3470	A6	3523	A7

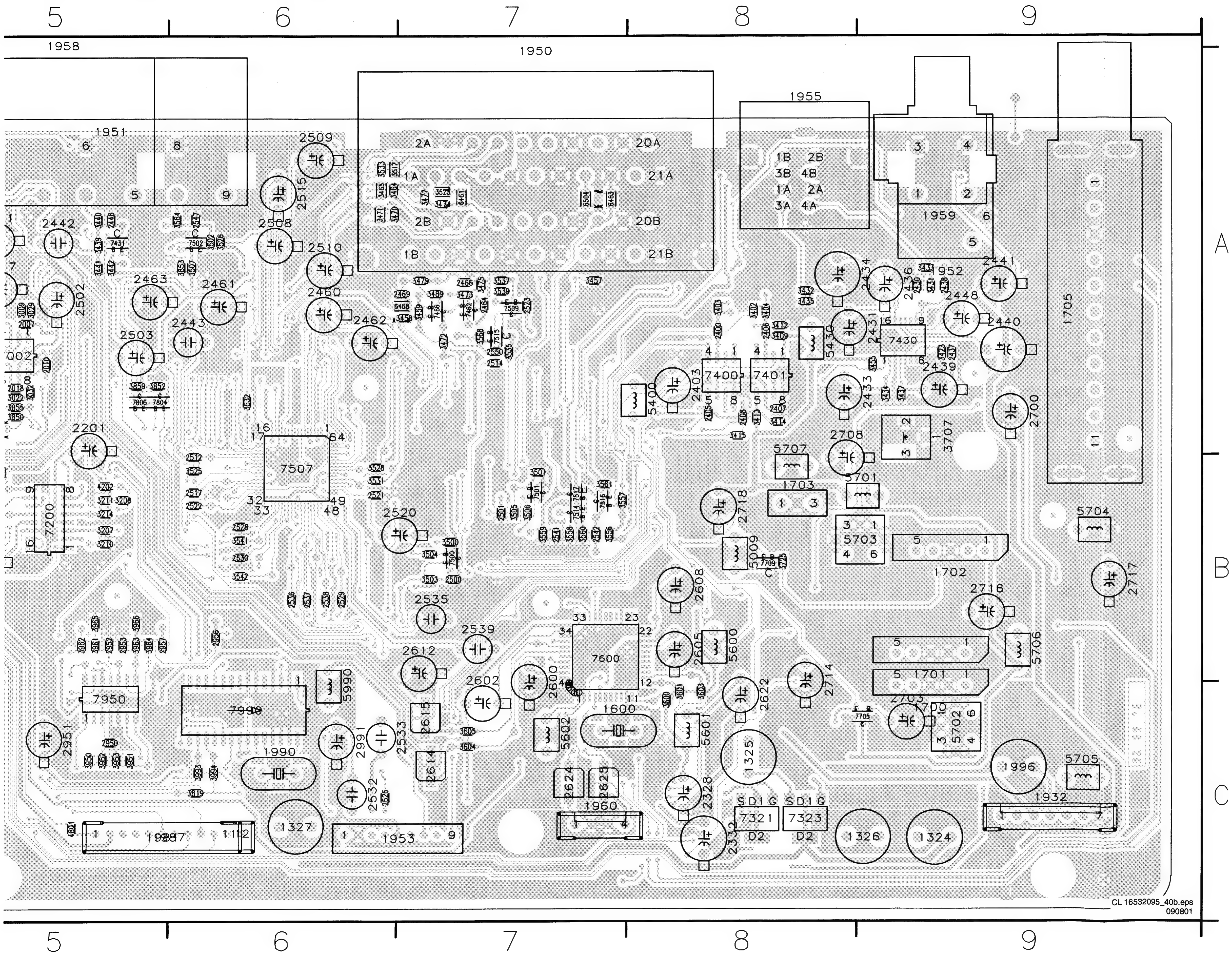
3523	B6	3604	C7	3841	B2	3874	A3	3905	B2	3961	B5	3987	A2	5601	C8	7000	A5	7507	B6	7906	A1
3526	A6	3605	C7	3844	B2	3875	B3	3906	A1	3962	B5	3988	A2	5602	C7	7001	A4	7509	A7	7950	C5
3528	B6	3707	A9	3847	B2	3876	B4	3908	B2	3963	B5	3989	A2	5701	B9	7002	A5	7514	B7	7970	A1
3531	B6	3725	B8	3848	B3	3877	A3	3910	B2	3964	B5	3993	C6	5702	C9	7003	A4	7600	B7	7971	A1
3532	A6	3801	B3	3850	A5	3878	A3	3911	B1	3965	B5	3994	C6	5703	B9	7004	A4	7705	C9	7972	A2
3533	A6	3802	B3	3852	A5	3879	A3	3912	B1	3966	B5	3996	A2	5703	C9	7200	B5	7709	B8	7973	A1
3533	A7	3803	B3	3853	A6	3880	A2	3916	B2	3967	A2	3997	A2	5704	B9	7315	A7	7800	A4	7974	A1
3536	B7	3804	B3	3854	A3	3881	A3	3917	B2	3968	A2	4202	B3	5706	B9	7316	B7	7801	B3	7975	A1
3537	A7	3807	A4	3855	A5	3882	B4	3918	B1	3969	A2	4405	B4	5707	A8	7317	B7	7803	B2	7990	C6
3537	B7	3808	B3	3856	B3	3883	B3	3920	A2	3970	A2	4406	B4	5902	B2	7321	C8	7804	A3		
3538	B7	3812	B3	3857	B4	3884	A3	3921	A1	3971	A2	4470	A2	5990	C6	7323	C8	7805	B3		
3539	A7	3814	B3	3859	A5	3885	A2	3922	A1	3972	A2	4471	A2	6000	A5	7332	A4	7806	A5		
3539	B7	3815	A4	3860	B5	3886	B3	3930	C5	3973	A2	4801	C5	6304	A7	7400	A8	7807	B4		
3541	B6	3817	B3	3861	B4	3887	B4	3940	A2	3975	A2	4901	A1	6309	B3	7401	A8	7809	B4		
3542	B6	3818	B3	3862	B4	3888	B4	3941	A2	3976	A2	4902	A1	6461	A7	7430	A9	7810	B4		
3560	B7	3819	C6	3863	A2	3890	B2	3942	A1	3977	A1	4903	A1	6463	A7	7431	A5	7811	A3		
3561	B7	3821	B3	3864	A2	3891	A3	3943	A1	3979	A1	4906	B4	6468	A7	7432	A1	7812	B3		
3564	A6	3822	A3	3865	B2	3892	A3	3944	A1	3980	A2	5000	A4	6471	A3	7434	B4	7813	A3		
3568	A7	3829	A3	3866	B3	3896	B3	3946	A1	3981	A1	5002	A3	6801	B3	7462	A7	7815	B2		
3570	B3	3830	A3	3867	A2	3897	A2	3947	A1	3982	A1	5003	B2	6803	A3	7466	A7	7900	B1		
3600	C8	3832	A4	3868	A2	3898	B4	3948	A2	3983	A1	5009	B8	6807	B2	7470	A2	7901	B1		
3600	B8	3837	A3	3869	A2	3901	B1	3951	C5	3984	A2	5400	A8	6970	A1	7500	B7	7902	A2		
3601	C8	3839	B3	3870	A2	3903	B2	3952	C5	3985	A2	5430	A8	6971	A1	7501	B7	7903	A1		
3603	C8	3840	B2	3872	A3	3904	B2	3953	C5	3986	A2	5470	A3	6972	A1	7502	A6	7904	A1		



Layout Analog Board (Part 1 Top View)



Layout Analog Board (Part 2 Top View)



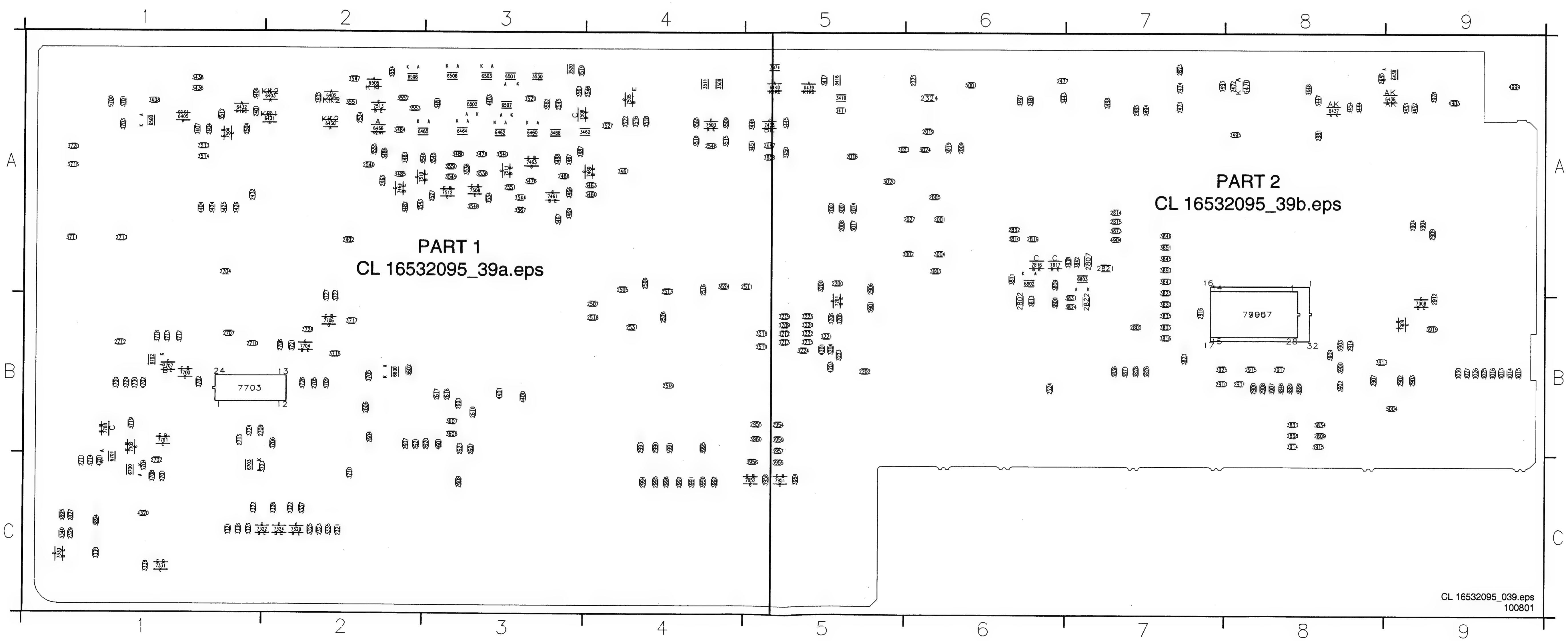
Layout Analog Board (Overview Bottom View)

2001	A6	2402	A2	2526	B4	2702	C1	2900	B8
2002	A5	2404	A1	2527	A3	2704	A1	2902	B9
2005	A6	2432	A1	2529	C1	2705	B2	2903	B9
2008	A5	2445	A9	2531	B4	2706	B2	2904	A9
2009	A6	2447	A5	2534	A2	2707	B1	2906	B5
2014	A5	2465	A2	2540	A2	2709	B2	2907	B8
2016	A5	2467	A3	2545	A3	2710	B1	2908	B8
2019	A6	2468	A3	2546	A4	2711	C1	2909	A9
2027	A6	2472	A8	2548	A4	2712	B1	2910	B8
2100	C7	2473	A7	2549	B4	2713	A1	2911	B8
2101	C7	2474	A7	2551	A3	2715	B1	2912	B9
2102	C7	2477	A7	2601	C3	2802	B6	2914	B8
2103	C7	2481	A6	2603	B3	2805	B7	2915	B8
2104	C7	2485	A7	2604	B2	2807	A7	2916	B7
2105	C7	2504	A1	2606	B2	2808	B8	2917	B8
2106	C6	2505	B4	2607	B2	2809	B8	2954	B5
2200	A5	2506	A4	2609	C3	2814	A7	2955	B5
2202	B5	2507	B4	2610	B3	2815	A7	2981	A8
2321	C2	2511	B5	2616	B3	2819	A6	2990	C4
2322	C2	2513	B4	2617	B3	2821	A7	2992	C4
2323	C2	2516	B4	2620	B3	2822	B7	2993	C4
2324	A6	2518	B4	2621	B3	2823	A7	2994	C4
2325	A6	2519	B5	2623	C3	2827	C1	2995	C4
2401	A1	2524	B6	2701	C1	2832	A6	2996	C4

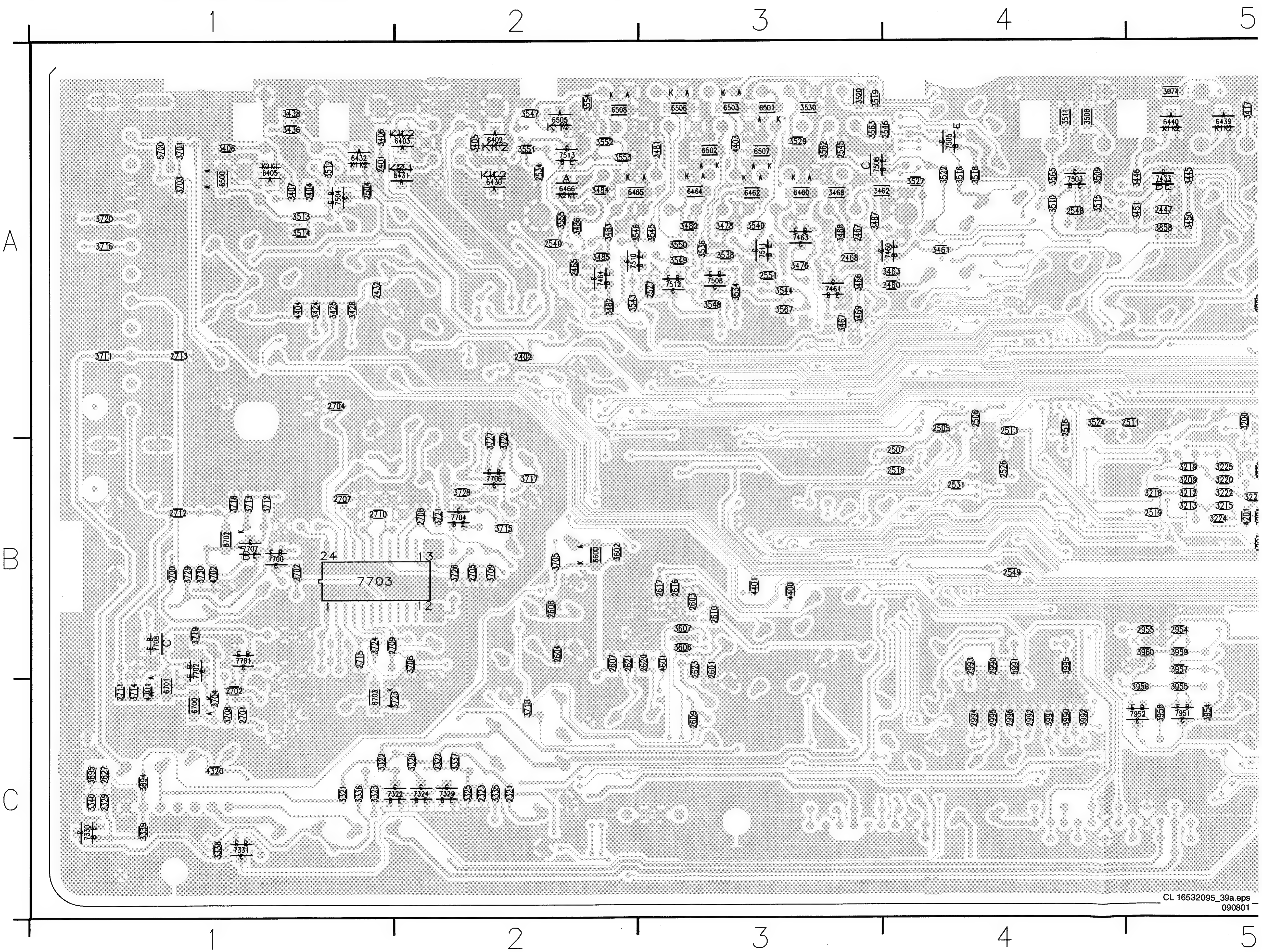
3002	A6	3107	C7	3322	A4	3444	A8	3484	A2
3003	A6	3108	C7	3323	C1	3445	A5	3485	A2
3004	A6	3109	C6	3325	C2	3446	A5	3486	A2
3007	A5	3111	C6	3326	C2	3447	A8	3487	A4
3013	B9	3112	C6	3335	C2	3448	A8	3488	A3
3014	B9	3113	C6	3336	C1	3450	A5	3493	A8
3015	B9	3200	A5	3337	C2	3451	A5	3494	A7
3016	B9	3204	B5	3338	C1	3452	A9	3495	A8
3017	A5	3205	B5	3339	C1	3453	A9	3497	A6
3019	A6	3206	B5	3340	C1	3454	A8	3498	A7
3020	A5	3209	B5	3405	A2	3460	A4	3508	A4
3023	A6	3212	B5	3406	A1	3461	A4	3509	A4
3024	A6	3213	B5	3407	A1	3462	A4	3510	A4
3025	B9	3215	B5	3408	A1	3463	A4	3511	A4
3026	B9	3218	B5	3410	A5	3466	A3	3512	A1
3027	B9	3219	B5	3411	A5	3467	A3	3513	A1
3030	B9	3220	B5	3416	A5	3468	A3	3514	A1
3100	C7	3221	B5	3417	A5	3469	A3	3515	A4
3101	C7	3222	B5	3424	A1	3476	A3	3516	A4
3102	C7	3223	B5	3425	A1	3478	A3	3518	A4
3103	C7	3224	B5	3426	A1	3480	A3	3519	A4
3104	C7	3225	B5	3436	A1	3481	A3	3520	A3
3105	C7	3321	C1	3438	A1	3482	A2	3522	A4
3106	C7	3322	C1	3443	A7	3483	A2	3524	B4

3524	B4	3602	B2	3722	B2	3835	B7	3919	B9
3527	A4	3606	B3	3723	C2	3836	B7	3925	B8
3529	A3	3607	B3	3724	B1	3838	A7	3954	C5
3530	A3	3700	B1	3726	B2	3842	A7	3955	C5
3534	A3	3701	A1	3727	B2	3843	A7	3956	C5
3538	A3	3702	B1	3728	B2	3845	A7	3957	C5
3540	A3	3703	A1	3729	B1	3846	B8	3958	C5
3543	A3	3704	C1	3730	B1	3849	A7	3959	B5
3544	A3	3705	B2	3800	B6	3851	A7	3960	B5
3545	A3	3706	B2	3805	B7	3858	A5	3974	A5
3546	A3	3708	C1	3809	A6	3871	B7	3978	A9
3547	A2	3709	B2	3810	A6	3873	A7	3990	C4
3548	A3	3710	C2	3811	A6	3889	B8	3991	C4
3549	A3	3711	A1	3813	B6	3893	A7	3992	C4
3550	A3	3712	B1	3816	B7	3894	C1	3995	C4
3551	A2	3713	B1	3820	B7	3895	C1	4101	C7
3552	A2	3714	C1	3823	B7	3899	B8	4102	C7
3553	A2	3715	B2	3824	B7	3900	B8	4201	B5
3554	A2	3716	A1	3825	B7	3902	B8	4203	B5
3555	A2	3717	B2	3826	B7	3907	B8	4320	C1
3562	A3	3718	B1	3828	B7	3909	B8	4400	B3
3563	A4	3719	B1	3831	B7	3913	B9	4401	B3
3565	A4	3720	A1	3833	B8	3914	B8	4403	A3
3567	A3	3721	B2	3834	B8	3915	B8	4404	A1

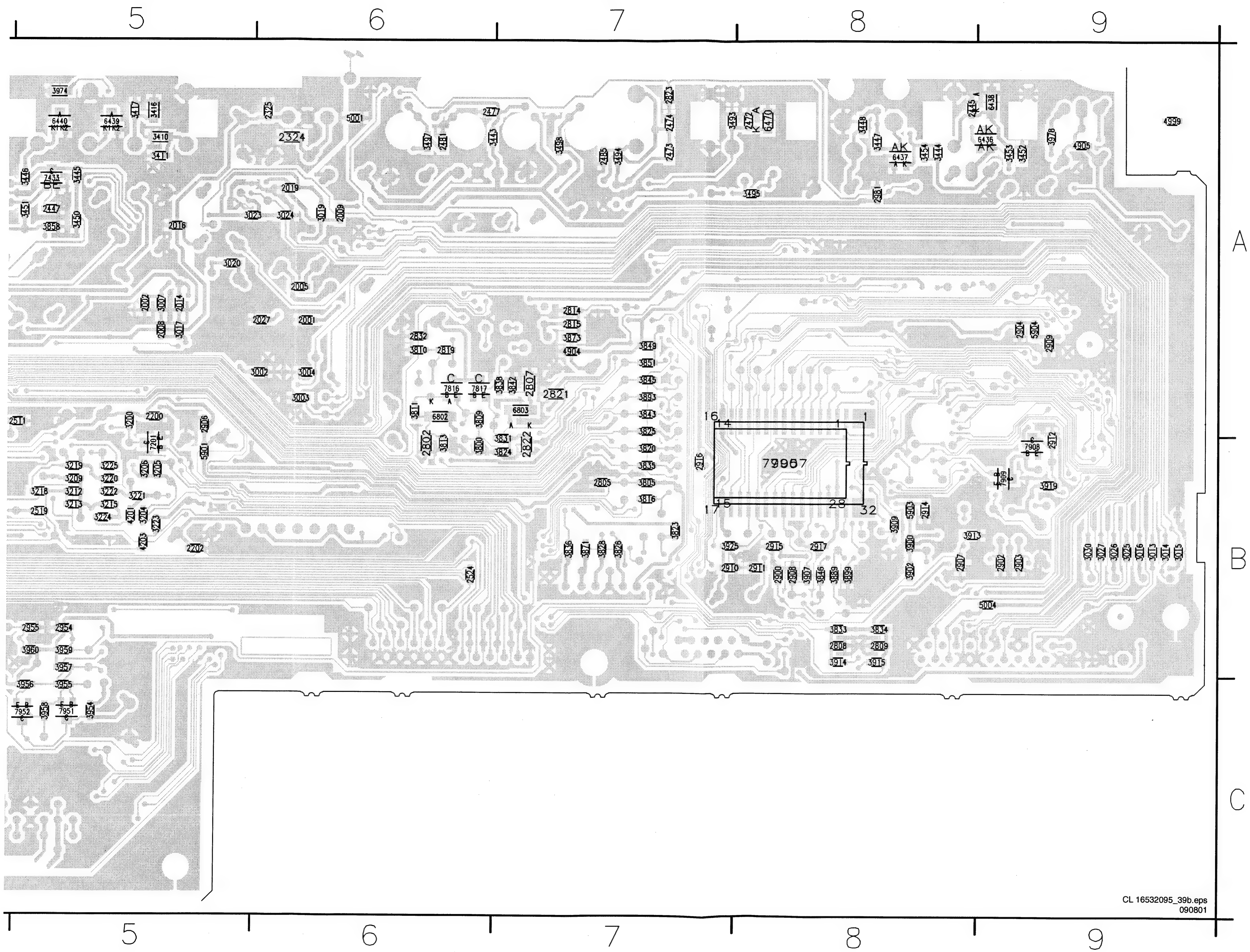
4601	B3	6436	A9	6802	A6	7700	B1
4701	C1	6437	A8	6803	A7	7701	B1
4702	B1	6438	A9	7100	C7	7702	C1
4904	A7	6439	A5	7101	C7	7704	B2
4905	A9	6440	A5	7201	B5	7705	B1
4999	A9	6460	A3	7322	C2	7706	B2
5001	A6	6462	A3	7324	C2	7707	B1
5004	B9	6464	A3	7329	C2	7708	B1
5700	A1	6465	A3	7330	C1	7816	A6
5901	B5	6466	A2	7331	C1	7817	A6
5903	B8	6470	A8	7433	A5	7903	B8
5904	A9	6500	A1	7460	A4	7907	B8
5991	C4	6501	A3	7461	A3	7908	B9
6100	C7	6502	A3	7463	A3	7909	B9
6101	C7	6503	A3	7464	A2	7951	C5
6102	C6	6505	A2	7503	A4	7952	C5
6103	C6	6506	A3	7504	A1	35336	A3
6104	C6	6507	A3	7505	A4		
6402	A2	6508	A2	7506	A4		
6403	A2	6600	B2	7508	A3		
6405	A1	6700	C1	7510	A3		
6430	A2	6701	C1	7511	A3		
6431	A2	6702	B1	7512	A3		
6432	A1	6703	C1	7513	A2		



Layout Analog Board (Part 1 Bottom View)

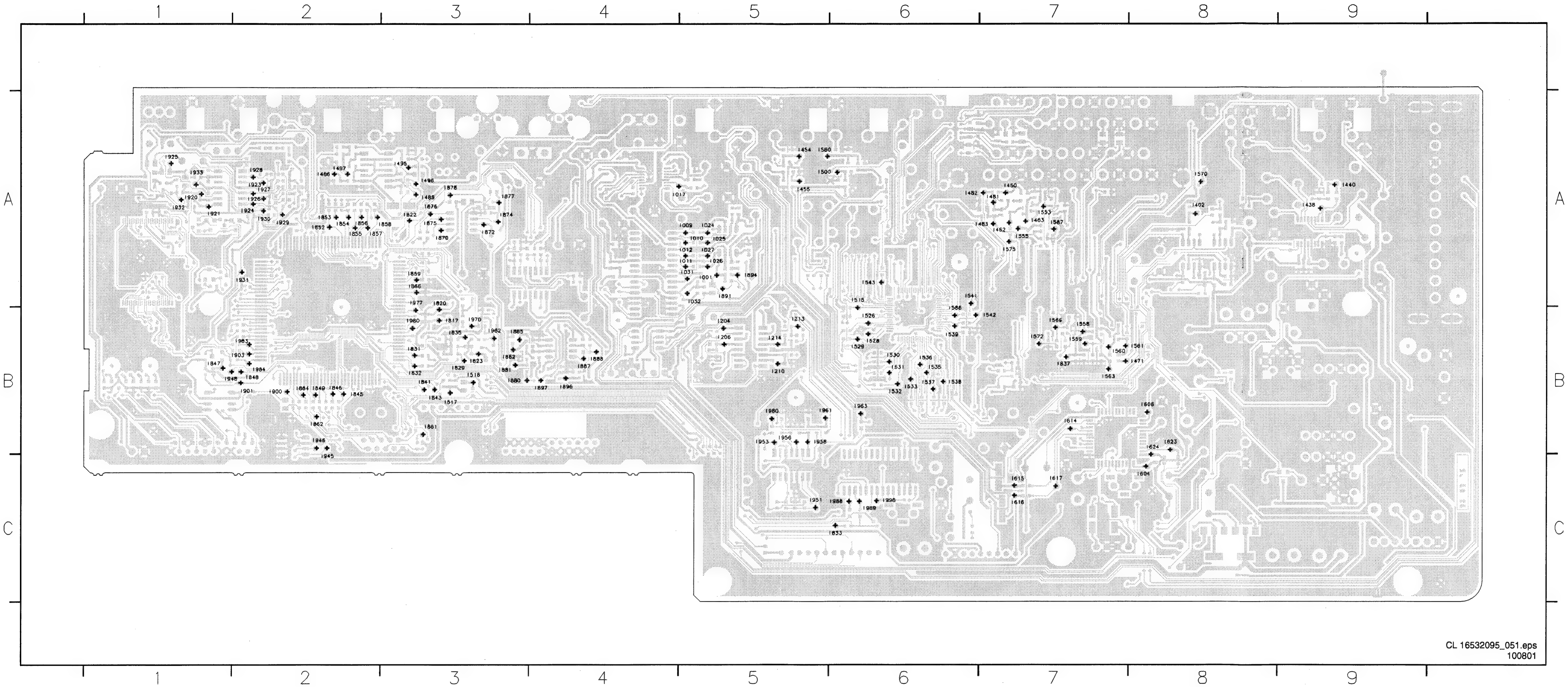


Layout Analog Board (Part 2 Bottom View)



Layout Analog Board (Testlands Top View)

1001 A5	1024 A5	1204 B5	1438 A9	1463 A7	1486 A2	1517 B3	1531 B6	1538 B6	1555 A7	1566 B7	1587 A7	1617 C7	1823 B3	1837 B7	1848 B2	1856 A2	1864 B2	1876 A3	1885 B3	1897 B4	1923 A2	1929 A2	1946 B2	1960 B5	1982 B3
1009 A5	1025 A5	1206 B5	1440 A9	1471 B7	1495 A3	1518 B3	1532 B6	1539 B6	1558 B7	1570 A8	1604 C8	1623 B8	1829 B3	1841 B3	1849 B2	1857 A2	1866 A3	1877 A3	1887 B4	1900 B2	1924 A2	1930 A2	1948 B1	1961 B5	1983 B2
1010 A5	1026 A5	1210 B5	1454 A5	1481 A7	1496 A3	1526 B6	1533 B6	1541 A6	1559 B7	1572 B7	1606 B8	1624 C8	1831 B3	1843 B3	1852 A2	1858 A2	1870 A3	1878 A3	1888 B4	1901 B2	1925 A1	1931 A2	1951 C5	1963 B6	1984 B2
1011 A5	1027 A5	1213 B5	1455 A5	1482 A7	1497 A2	1528 B6	1535 B6	1542 B6	1560 B7	1575 A7	1614 B7	1817 B3	1832 B3	1845 B2	1853 A2	1859 A3	1872 A3	1880 B3	1891 A5	1903 B2	1926 A2	1932 A1	1953 B5	1970 B3	1988 C6
1012 A5	1031 A5	1214 B5	1460 A7	1483 A7	1500 A6	1529 B6	1536 B6	1543 A6	1561 B7	1580 A5	1615 C7	1820 B3	1833 C6	1846 B2	1854 A2	1861 B3	1874 A3	1881 B3	1894 A5	1920 A1	1927 A2	1933 A1	1956 B5	1977 B3	1989 C6
1017 A4	1032 A5	1402 A8	1462 A7	1485 A3	1515 B6	1530 B6	1537 B6	1553 A7	1563 B7	1586 B6	1616 C7	1822 A3	1835 B3	1847 B1	1855 A2	1862 B2	1875 A3	1882 B3	1896 B4	1921 A1	1928 A2	1945 B2	1958 B5	1980 B3	1996 C6



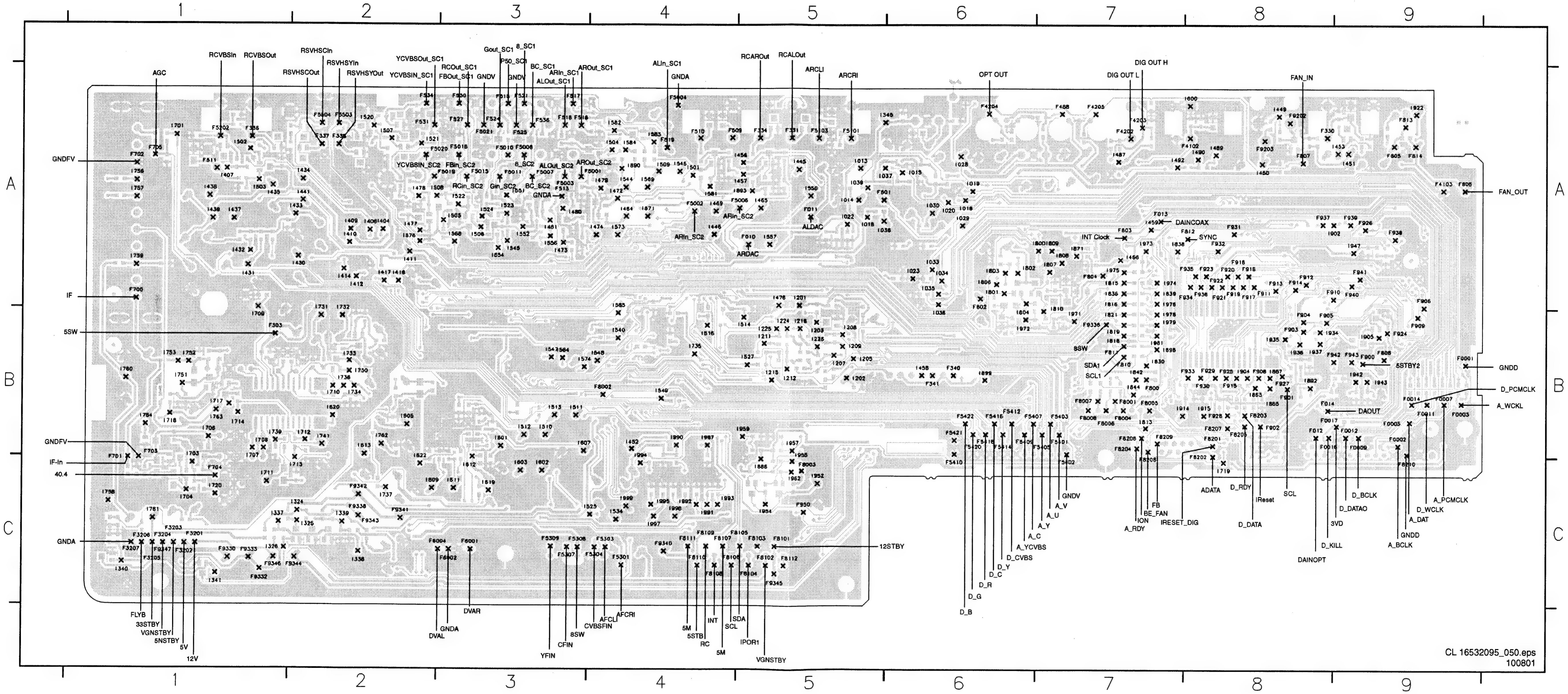
Layout Analog Board (Testlands Bottom View)

F0001	B9	F1008	C7	F336	A1	F5015	A3	F527	A3	F5416	B6
F0002	B9	F1101	C7	F337	A2	F5016	A3	F530	A3	F5418	B6
F0003	B9	F1103	C7	F338	A2	F5019	A2	F5301	C4	F5420	B6
F0005	B9	F1104	C7	F340	B6	F5020	A2	F5303	C4	F5421	B6
F0007	B9	F1105	C7	F341	B6	F5021	A3	F5304	C4	F5422	B6
F0009	B9	F1106	C7	F4102	A8	F509	A4	F5306	C3	F5503	A2
F0011	B9	F1107	C6	F4103	A9	F510	A4	F5307	C3	F5504	A2
F0012	B9	F1108	C6	F4202	A7	F5101	A5	F5309	C3	F6001	C3
F0014	B9	F1109	C6	F4203	A7	F5103	A5	F531	A2	F6002	C3
F0016	B8	F303	B1	F4204	A6	F511	A1	F534	A2	F6004	C3
F0017	B9	F3201	C1	F4205	A7	F513	A3	F536	A3	F700	A1
F010	A5	F3202	C1	F5001	A3	F515	A3	F5401	B7	F701	C1
F011	A5	F3203	C1	F5002	A4	F516	A3	F5402	B7	F702	A1
F012	B8	F3204	C1	F5003	A3	F517	A3	F5403	B7	F703	C1
F013	A7	F3205	C1	F5004	A4	F518	A3	F5405	B7	F704	C1
F014	B8	F3206	C1	F5006	A5	F519	A4	F5407	B6	F705	A1
F1001	C7	F3207	C1	F5007	A3	F5202	A1	F5409	B6	F800	B7
F1002	C6	F330	A8	F5008	A3	F521	A3	F5410	B6	F8002	B4
F1005	C7	F331	A5	F5010	A3	F524	A3	F5412	B6	F8003	C5
F1007	C7	F334	A5	F5011	A3	F525	A3	F5414	B6	F8004	B7

F8005	B7	F8109	C4	F902	B8	F921	A8	F9341	C2	1019	A6
F8006	B7	F811	B7	F903	B8	F922	A8	F9342	C2	1020	A6
F8008	B7	F8110	C4	F904	B8	F923	A8	F9344	C2	1022	A5
F801	A5	F8111	C4	F905	B8	F924	B9	F9345	C5	1023	A6
F802	A6	F8112	C5	F906	A9	F925	B8	F9346	C1	1028	A6
F803	A7	F812	A8	F908	B8	F926	A9	F935	A8	1029	A6
F804	A7	F813	A9	F909	B9	F927	B8	F936	A8	1030	A6
F805	A9	F814	A9	F910	A8	F928	B8	F937	A8	1033	A6
F806	A9	F8201	B8	F911	A8	F929	B8	F938	A9	1034	A6
F807	A8	F8202	B8	F912	A8	F930	B8	F939	A9	1035	A6
F808	B9	F8203	B8	F913	A8	F931	A8	F940	A9	1036	A6
F810	B7	F8204	B7	F914	A8	F932	A8	F941	A9	1037	A5
F8101	C5	F8205	B8	F915	B8	F933	B8	F942	B9	1038	A5
F8102	C5	F8207	B8	F916	A8	F9330	C1	F943	B9	1039	A5
F8103	C5	F8208	B7	F917	A8	F9332	C1	F950	C5	1100	C7
F8104	C5	F8209	B7	F918	A8	F9333	C1	1013	A5	1101	C7
F8105	C5	F8210	B9	F919	A8	F9336	B7	1014	A5	1102	C7
F8106	C4	F8211	B7	F920	A8	F9338	C2	1015	A6	1103	C7
F8107	C4	F900	B9	F9202	A8	F934	A8	1016	A5	1104	C6
F8108	C4	F901	B8	F9203	A8	F9340	C4	1018	A6	1201	A5

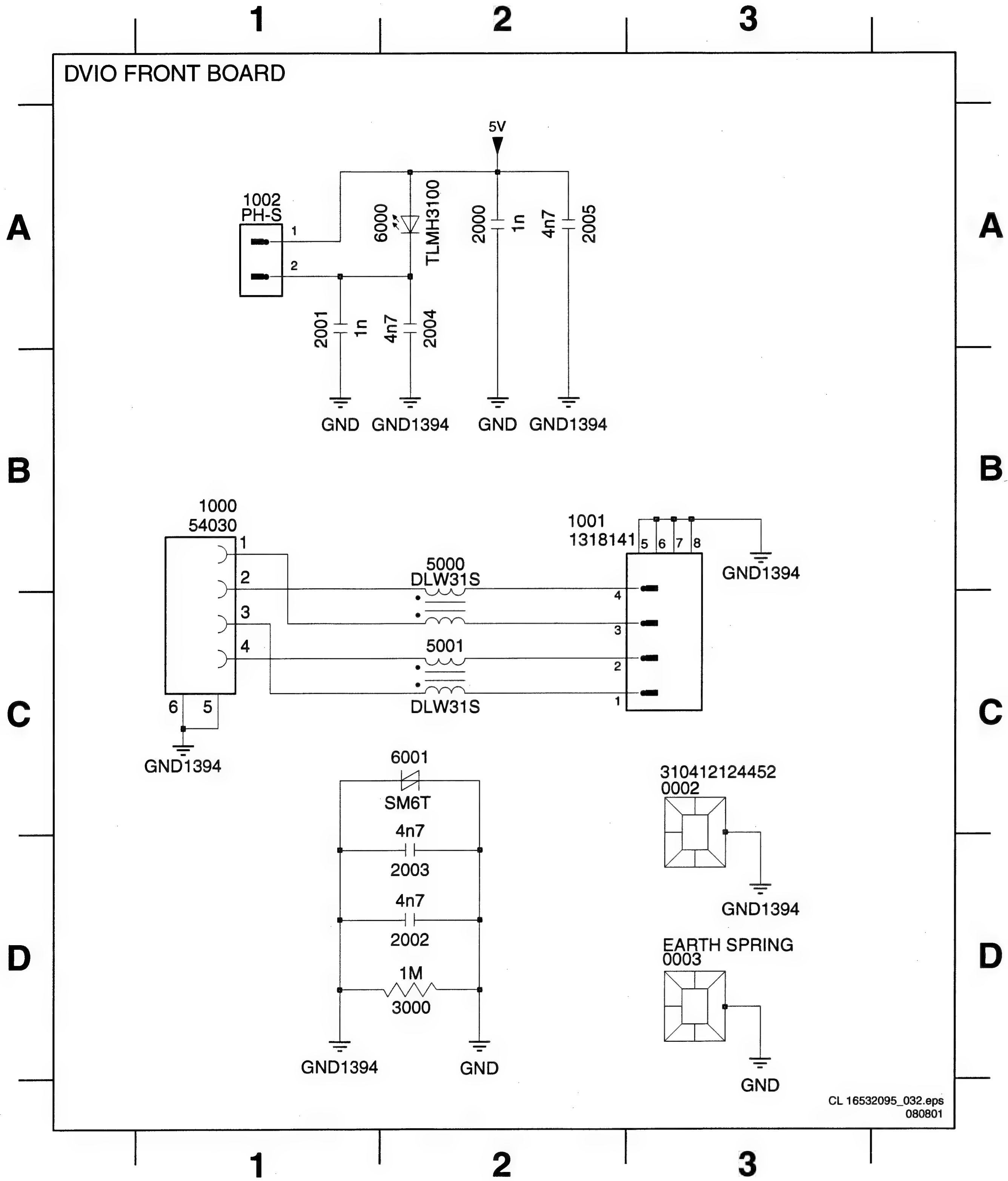
1202	B5	1341	C1	1439	A1	1474	A4	1511	B3	1550	A5
1203	B5	1345	A5	1441	A2	1476	A5	1512	B3	1551	A3
1205	B5	1404	A2	1445	A5	1477	A2	1513	B3	1552	A3
1207	B5	1406	A2	1446	A4	1478	A2	1514	B5	1554	A3
1208	B5	1407	A1	1449	A8	1479	A4	1516	B4	1556	A3
1209	B5	1409	A2	1450	A8	1480	A3	1520	A2	1557	A5
1211	B5	1410	A2	1451	A9	1487	A7	1521	A2	1564	B3
1212	B5	1411	A2	1452	B4	1489	A8	1522	A3	1568	A3
1215	B5	1412	A2	1453	A9	1490	A8	1523	A3	1569	A4
1216	B5	1414	A2	1456	A5	1492	A7	1524	A3	1571	A4
1224	B5	1416	A2	1457	A5	1501	A4	1525	C4	1573	A4
1225	B5	1417	A2	1458	B6	1502	A1	1527	B5	1574	B3
1226	B5	1430	A2	1459	A7	1503	A1	1534	C4	1576	A2
1324	C2	1431	A1	1461	A3	1504	A4	1540	B4	1581	A4
1325	C2	1432	A1	1464	A4	1505	A3	1544	A4	1582	A4
1326	C1	1433	A2	1465	A5	1506	A3	1545	A3	1583	A4
1337	C1	1434	A2	1466	A7	1507	A2	1546	A4	1584	A4
1338	C2	1435	A1	1469	A4	1508	A2	1547	B3	1585	B4
1339	C2	1436	A1	1472	A4	1509	A4	1548	B4	1600	A8
1340	C1	1437	A1	1473	A3	1510	B3	1549	B4	1601	B3

1602	C3	1712	B2	1756	A1	1815	A7	1899	B6	1971	B7
1603	C3	1713	C2	1757	A1	1816	A7	1902	A8	1972	B6
1605	B2	1714	B1	1758	C1	1818	B7	1904	B8	1973	A7
1607	B3	1717	B1	1759	A1	1819	B7	1905	B9	1974	A7
1609	C2	1718	B1	1760	B1	1821	B7	1914	B7	1975	A7
1611	C3	1719	C8	1761	C1	1830	B7	1915	B8	1976	A7
1612	B3	1720	C1	1762	B2	1836	A7	1922	A9	1978	B7
1613	B2	1730	B2	1763	B1	1838	A7	1934	B8	1979	B7
1619	C3	1731	B2	1764	B1	1839	A7	1935	B8	1981	B7
1620	B2	1732	B2	1800	A7	1842	B7	1936	B8	1987	B4
1622	C2	1733	B2	1801	A6	1844	B7	1937	B8	1990	B4
1701	A1	1734	B2	1802	A6	1863	B8	1942	B9	1991	C4
1703	C1	1735	B4	1803	A6	1865	B8	1943	B9	1992	C4
1704	C1	1736	B2	1804	A6	1867	B8	1947	A9	1993	C4
1706	B1	1737	C2	1806	A6	1871	A7	1952	C5	1994	C4
1707	B1	1739	B1	1807	A7	1886	C5	1954	C5	1995	C4
1708	B1	1741	B2	1808	A7	1890	A4	1955	C5	1997	C4
1709	A1	1751	B1	1809	A7	1892	B8	1957	B5	1998	C4
1710	B2	1752	B1	1810	B7	1893	A5	1959	B5	1999	C4
1711	C1	1753	B1	1813	B7	1898	B7	1962	C5		

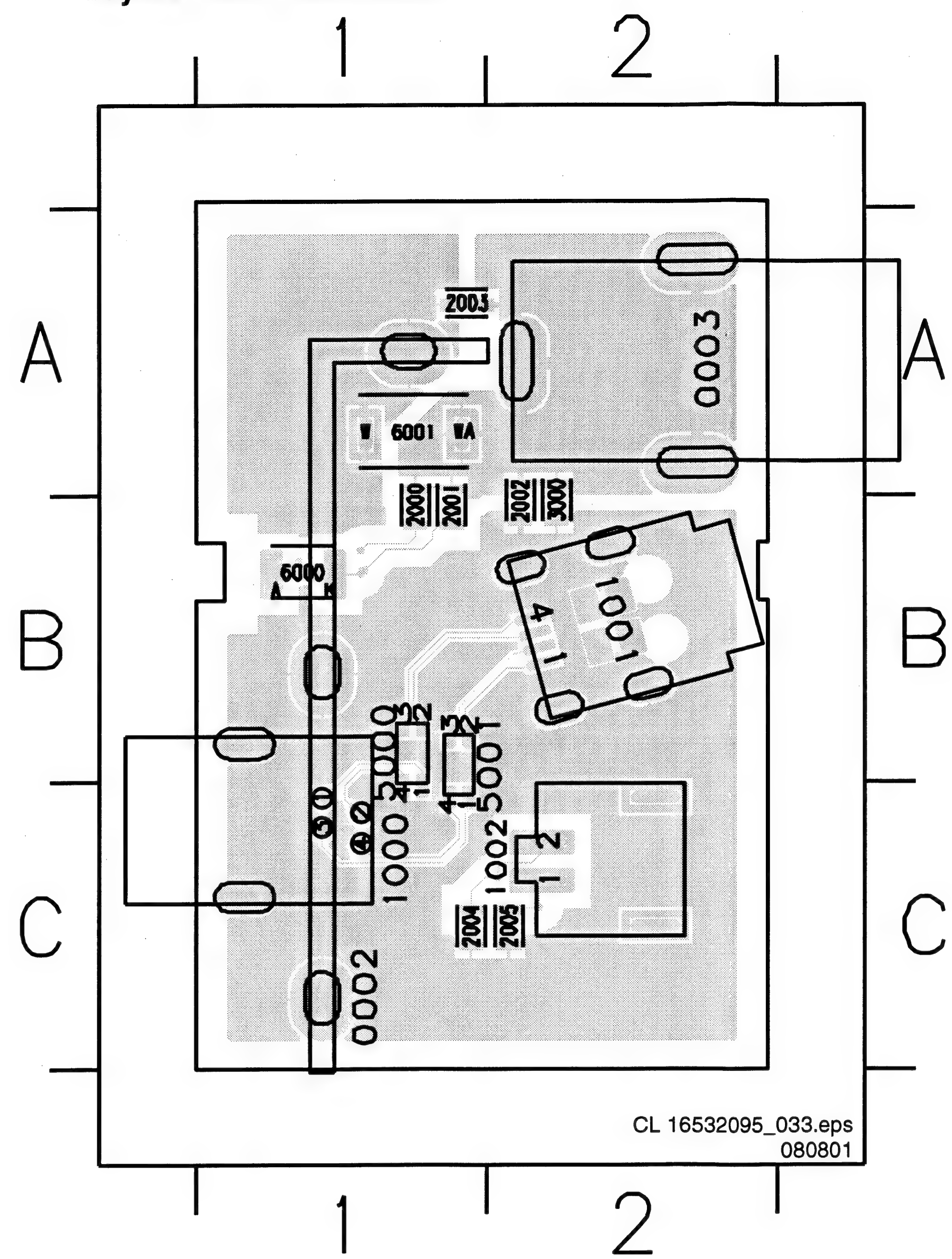


DVIO Front Board

0002 C3	1000 B1	1002 A1	2001 A1	2003 D2	5000 B2	6000 A2
0003 D3	1001 B2	2000 A2	2002 D2	3000 D2	5001 C2	6001 C2

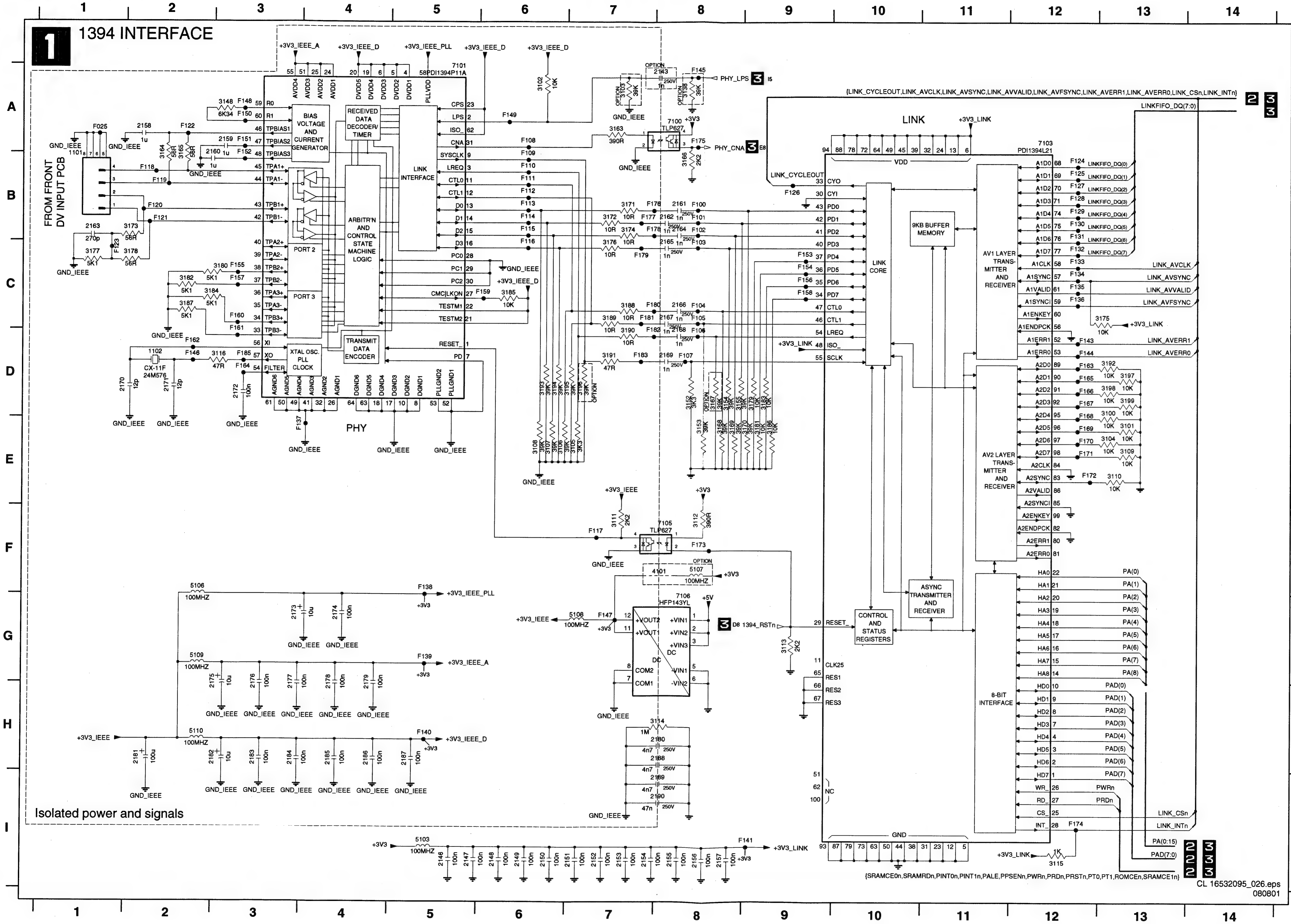


Layout DVIO Front Board



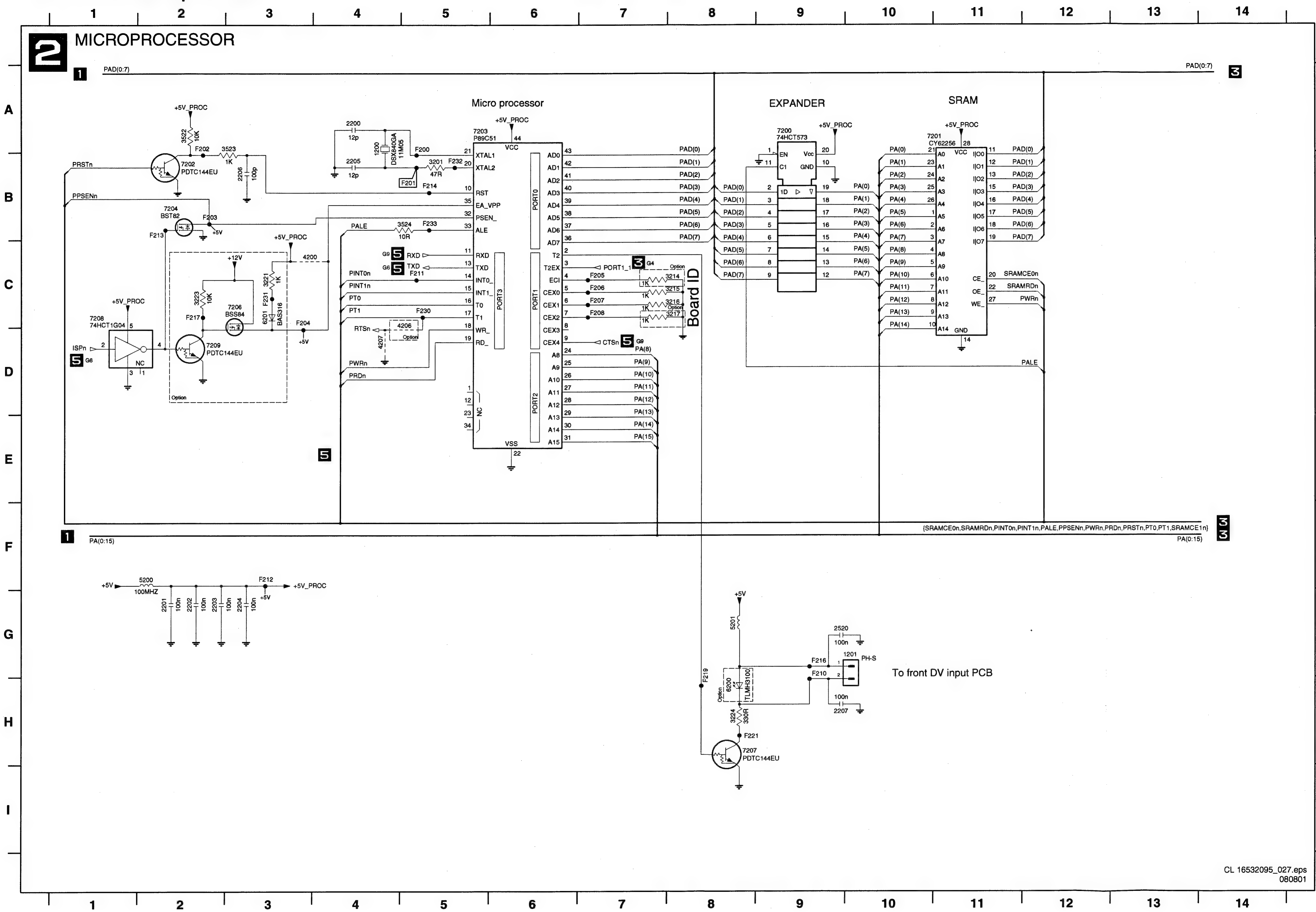
0002	C1
0003	A2
1000	C1
1001	B2
1002	C2
2000	B1
2001	B1
2002	B2
2003	A1
2004	C1
2005	C2
3000	B2
5000	B2
5001	B2
6000	B1
6001	A1

DVIO Board: 1394 Interface



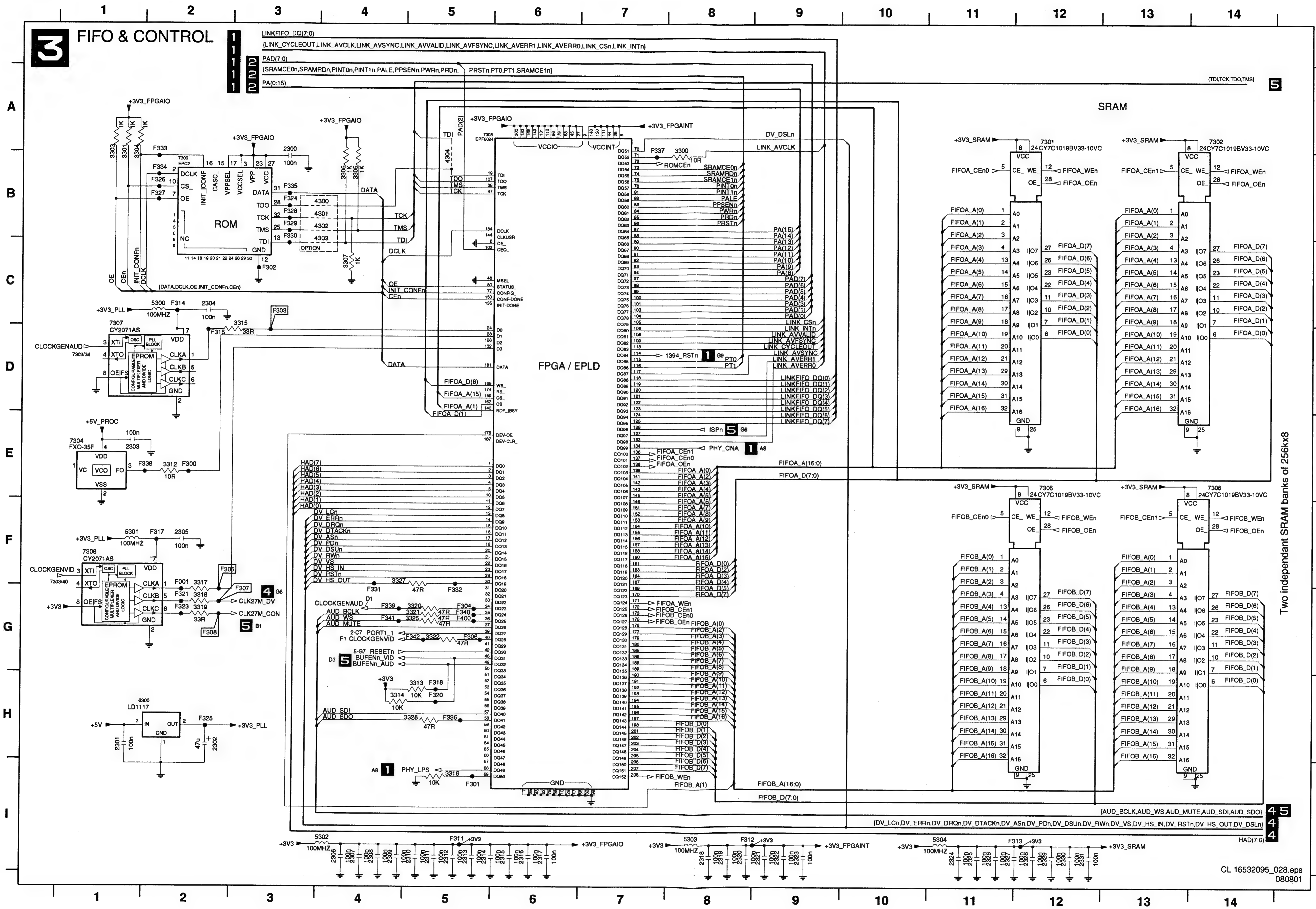
1101	A1	7105	F8
1102	D2	7106	G8
2143	A8	F025	A1
2146	I5	F100	B8
2147	I5	F101	B8
2148	I6	F102	B8
2149	I6	F103	C8
2150	I6	F104	C8
2151	I7	F105	C8
2152	I7	F106	D8
2153	I7	F107	D8
2154	I7	F108	A6
2155	I8	F109	B6
2156	I8	F110	B6
2157	I8	F111	B6
2158	A2	F112	B6
2159	A3	F113	B6
2160	B2	F114	B6
2161	B8	F115	B6
2162	B8	F116	C6
2163	B1	F117	F7
2164	B8	F118	B2
2165	C8	F119	B2
2166	C8	F120	B2
2167	C8	F121	B2
2168	D8	F122	A2
2169	D8	F123	C1
2170	D1	F124	B12
2171	D2	F125	B12
2172	D3	F126	B9
2173	G3	F127	B12
2174	G4	F128	B12
2175	H3	F129	B12
2176	H3	F130	B12
2177	H3	F131	B12
2178	H4	F132	C12
2179	H4	F133	C12
2180	H8	F134	C12
2181	H2	F135	C12
2182	H3	F136	C12
2183	H3	F137	E3
2184	H3	F138	F5
2185	H4	F139	G5
2186	H4	F140	H5
2187	H5	F141	I9
2188	H8	F143	D12
2189	I8	F144	D12
2190	I8	F145	A8
3100	D13	F146	D2
3101	E13	F147	G7
3102	A6	F148	A3
3103	A7	F149	A6
3104	E13	F150	A3
3105	E7	F151	A3
3106	E6	F152	B3
3107	E6	F153	C9
3108	E6	F154	C9
3109	E13	F155	C3
3110	E13	F156	C9
3111	F7	F157	C3
3112	F8	F158	C9
3113	G9	F159	C6
3114	H8	F160	C3
3115	I12	F161	D3
3116	D3	F162	D2
3138	A8	F163	D12
3148	A3	F164	D3
3152	D8	F165	D12
3153	E8	F166	D12
3154	D8	F167	D12
3155	D8	F168	D12
3163	A7	F169	E12
3164	B2	F170	E12
3165	B2	F171	E12
3166	B8	F172	E12
3167	D8	F173	F8
3168	E8	F174	I12
3169	E8	F175	A8
3170	E9	F176	B7
3171	B7	F177	B7
3172	B7	F178	B7
3173	B2	F179	C7
3174	B7	F180	C7
3175	C13	F181	C7
3176	C7	F182	D7
3177	C1	F183	D7
3178	C2	F185	D3
3179	D9		
3180	C3		
3181	E9		
3182	C2		
3183	D9		
3184	C2		
3185	C6		
3186	E9		
3187	C2		
3188	C7		
3189	C7		
3190	D7		
3191	D7		
3192	D13		
3193	D6		
3194	D6		
3195	D6		
3196	D7		
3197	D13		
3198	D13		
3199	D13		
4101	F8		
5103	I5		
5106	F2		
5107	F8		
5108	G7		
5109	G2		
5110	H2		
7100	A8		
7101	A5		
7103	A12		

DVIO Board: Microprocessor



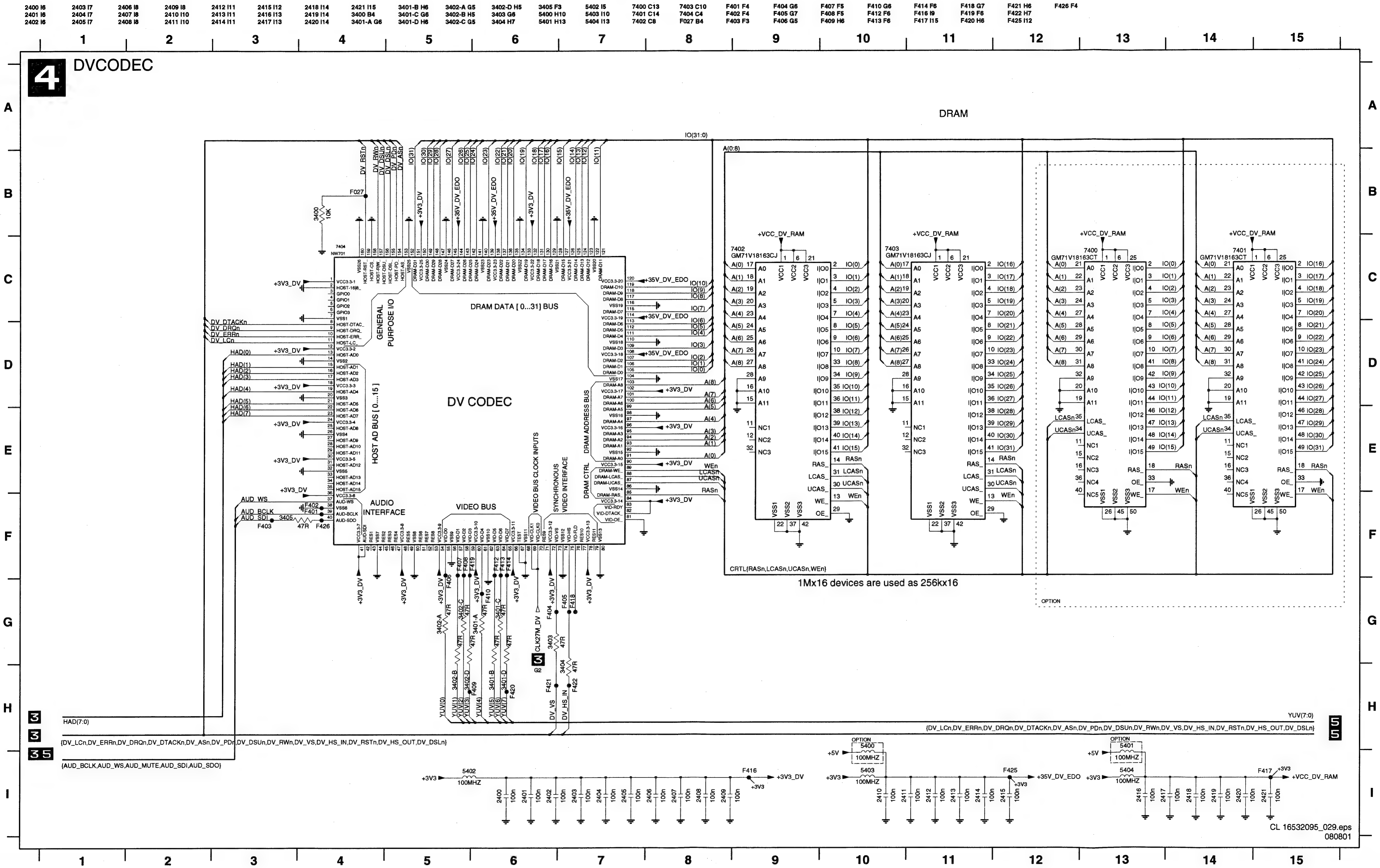
1200	A4
1201	G9
2200	A4
2201	G2
2202	G2
2203	G2
2204	G3
2205	B4
2206	B3
2207	H9
2520	G9
3201	B5
3214	C8
3215	C8
3216	C8
3217	C8
3221	C3
3223	C2
3224	H8
3522	A2
3523	A3
3524	B5
4200	C3
4206	D5
4207	D4
5200	F2
5201	G8
6200	H8
6201	C3
7200	A9
7201	A10
7202	B2
7203	A5
7204	B2
7206	C3
7207	H8
7208	C1
7209	D2
F200	A5
F201	B5
F202	A2
F203	B2
F204	D3
F205	C7
F206	C7
F207	C7
F208	C7
F210	G9
F211	C5
F212	F3
F213	B2
F214	B5
F216	G9
F217	C2
F219	G8
F221	H8
F230	C5
F231	C3
F232	B5
F233	B5

DVIO Board: Fifo & Control

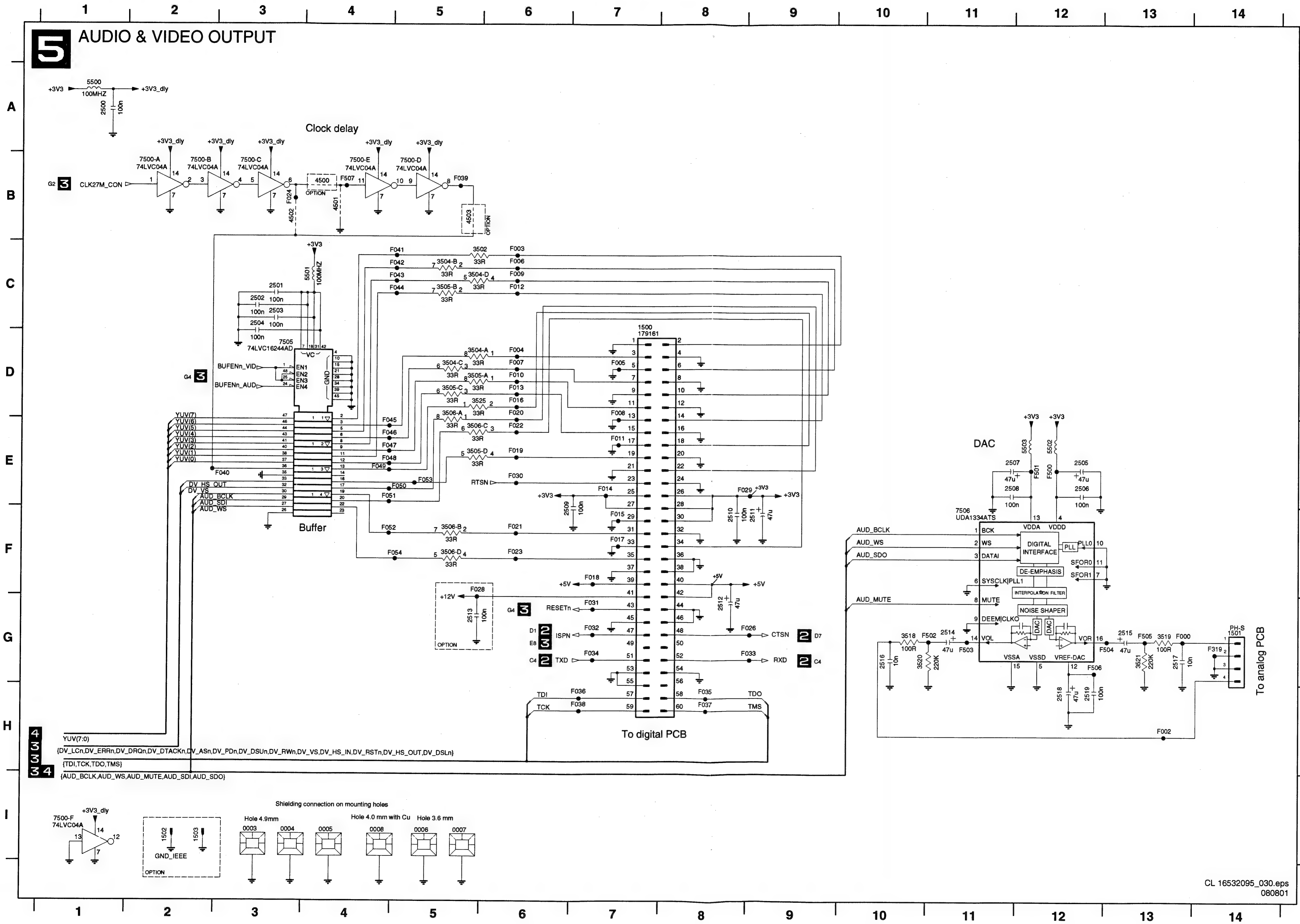


2300	A3
2301	H1
2302	H2
2303	E1
2304	C2
2305	F2
2306	I4
2307	I4
2308	I4
2309	I4
2310	I5
2311	I5
2312	I5
2313	I5
2314	I5
2315	I6
2316	I6
2317	I6
2318	I8
2319	I8
2320	I8
2321	I9
2322	I9
2323	I9
2324	I11
2325	I11
2326	I11
2327	I11
2328	I12
2329	I12
2330	I12
2331	I12
3300	B8
3301	B1
3303	B1
3304	B1
3305	B4
3306	B4
3307	C4
3312	E2
3313	H5
3314	H4
3315	D3
3316	I5
3317	G2
3318	G2
3319	G2
3320	G5
3321	G5
3322	G5
3325	G5
3327	F4
3328	H5
4300	B4
4301	B4
4302	B4
4303	C4
4304	B5
5300	C2
5301	F1
5302	I4
5303	I8
5304	I11
6300	H1
7300	B2
7301	A12
7302	A14
7303	A5
7304	E1
7305	E12
7306	E14
7307	D1
7308	F1
F001	F2
F300	E2
F301	I5
F302	C3
F303	C3
F304	G5
F305	G2
F306	G5
F307	G2
F308	G2
F311	I5
F312	I9
F313	I12
F314	C2
F315	D2
F317	F2
F318	H5
F320	H5
F321	G2
F323	G2
F324	B3
F325	H2
F326	B2
F327	B2
F328	B3
F329	B3
F330	B3
F331	G4
F332	G5
F333	A2
F334	B2
F335	B3
F336	H5
F337	A7
F338	E2
F339	G4
F340	G5
F341	G4
F342	G5
F400	G5

DVIO Board: DVCODEC

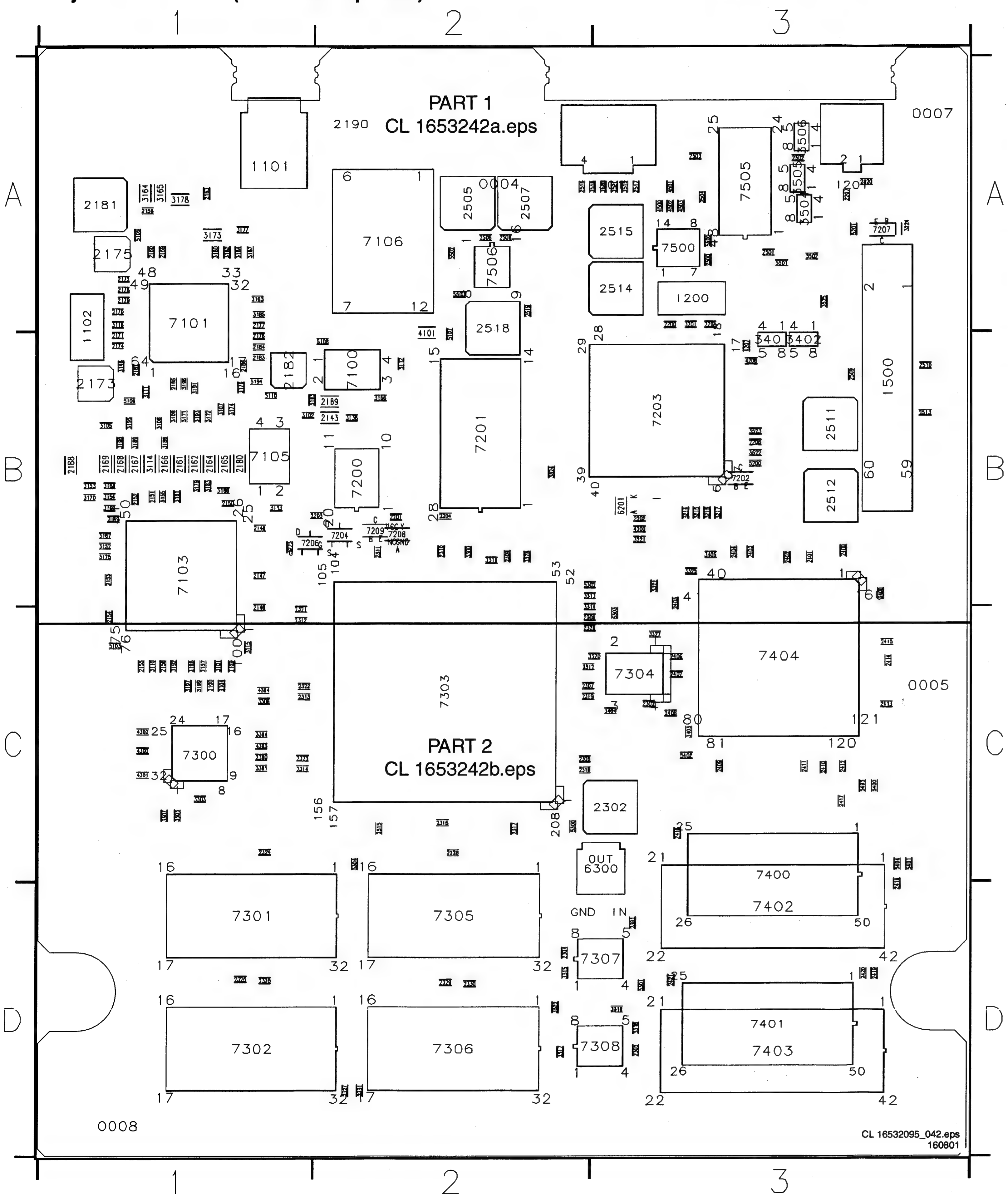


DVIO Board: Audio & Video Output



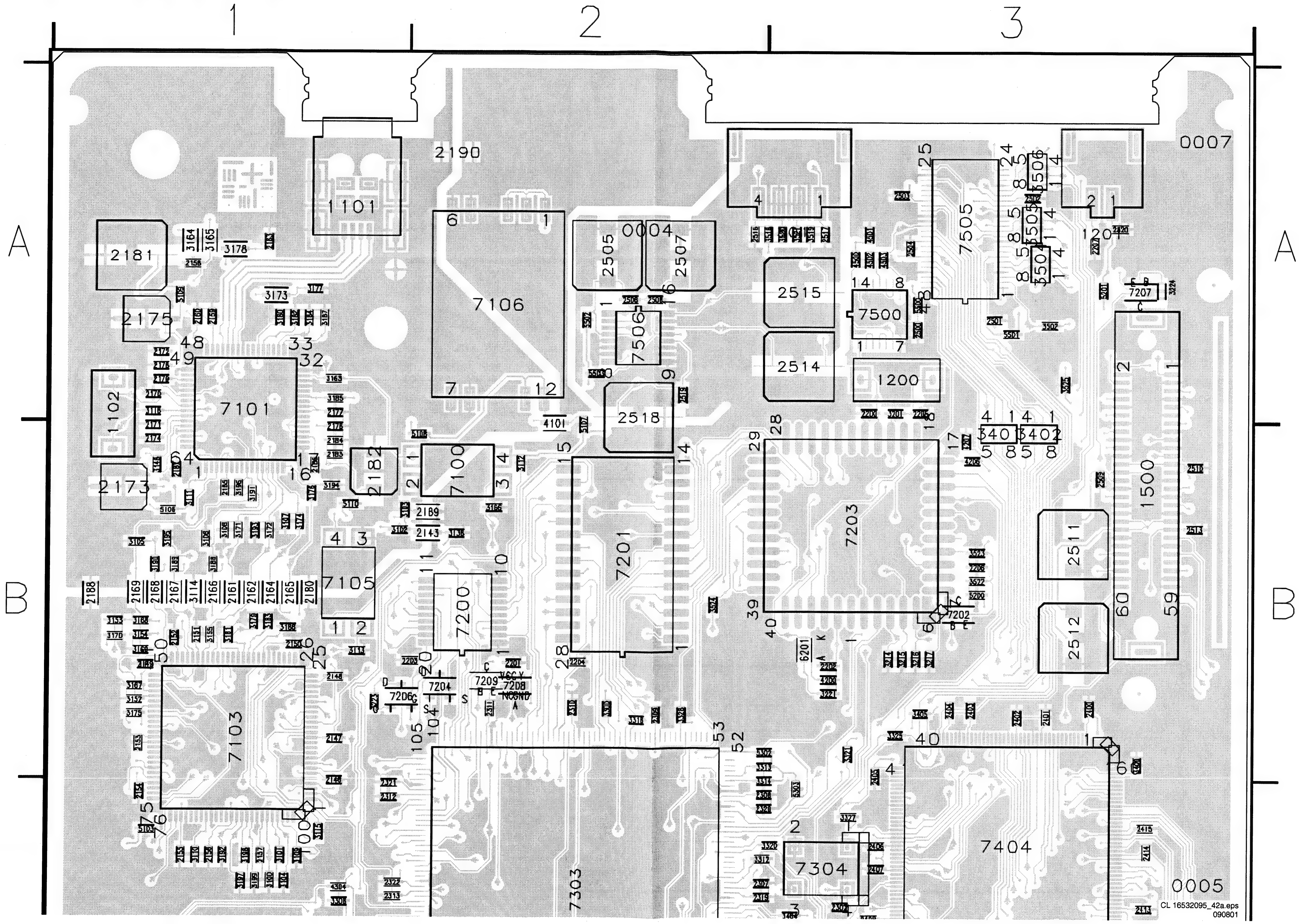
0003 I3
0004 I3
0005 I4
0006 I5
0007 I5
0008 I4
1500 C7
1501 G14
1502 I2
1503 I2
2500 A1
2501 C3
2502 C3
2503 C3
2504 C3
2505 E12
2506 E12
2507 E11
2508 E11
2509 F6
2510 F8
2511 F9
2512 G8
2513 G5
2514 G11
2515 G13
2516 G10
2517 G13
2518 H12
2519 H12
3502 C5
3504-A D5
3504-B C5
3504-C D5
3504-D C5
3505-A D5
3505-B C5
3505-C D5
3505-D E5
3506-A D5
3506-B F5
3506-C E5
3506-D F5
3518 G10
3519 G13
3520 G10
3521 G13
3525 D5
4500 B4
4501 B4
4502 B3
4503 B5
5500 A1
5501 C4
5502 E12
5503 E12
7500-A B2
7500-B B2
7500-C B3
7500-D B5
7500-E B4
7500-F I1
7505 D3
7506 F11
F000 G13
F002 H13
F003 C6
F004 D6
F005 D7
F006 C6
F007 D6
F008 D7
F009 C6
F010 D6
F011 E7
F012 C6
F013 D6
F014 E7
F015 F7
F016 D6
F017 F7
F018 F7
F019 E6
F020 D6
F021 F6
F022 E6
F023 F6
F024 B3
F026 G9
F028 F5
F029 E9
F030 E6
F031 G7
F032 G7
F033 G9
F034 G7
F035 H8
F036 H7
F037 H8
F038 H7
F039 B5
F040 E3
F041 C5
F042 C5
F043 C5
F044 C5
F045 E4
F046 E4
F047 E4
F048 E4
F049 E4
F050 E5
F051 E4
F052 F4
F053 E5
F054 F5
F319 G14
F500 E12
F501 E12
F502 G11
F503 G11
F504 G13
F505 G13
F506 G12
F507 B4

Layout DVIO Board (Overview Top View)

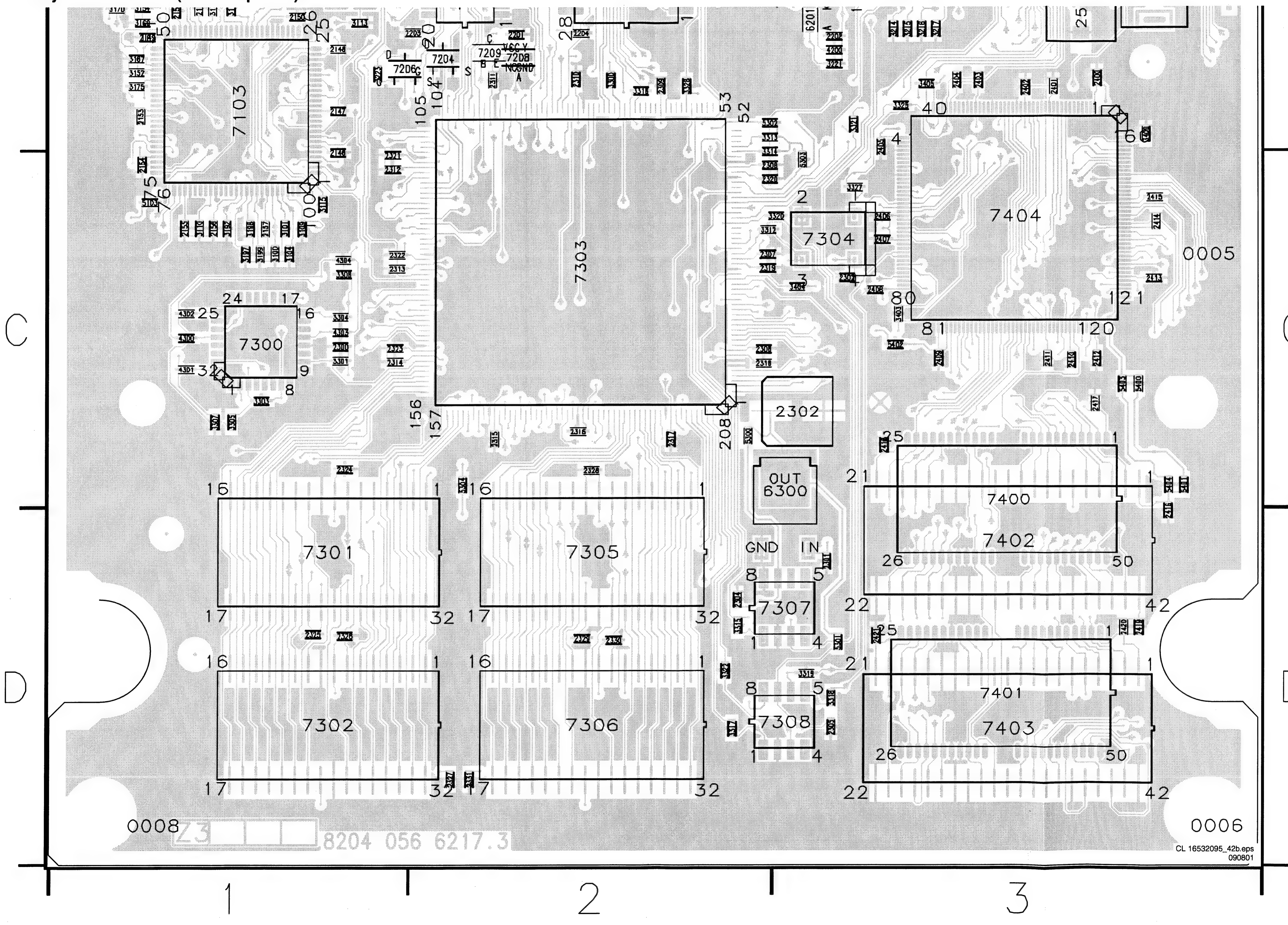


1101	A1	2313	C1	3111	B1	3321	B3
1102	A1	2314	C1	3112	B2	3322	D2
1200	A3	2315	C2	3113	B1	3325	B3
1201	A3	2316	C2	3114	B1	3327	C3
1500	B3	2317	C2	3115	C1	3328	B2
1501	A3	2318	C2	3116	A1	3400	B3
2143	B2	2319	C2	3138	B2	3401	B3
2146	C1	2320	C2	3148	B1	3402	B3
2147	B1	2321	C1	3152	B1	3403	C3
2148	B1	2322	C1	3153	B1	3404	C3
2149	B1	2323	C1	3154	B1	3405	B3
2150	B1	2324	C1	3155	B1	3502	A3
2151	B1	2325	D1	3163	A1	3504	A3
2152	B1	2326	D1	3164	A1	3505	A3
2153	B1	2327	D2	3165	A1	3506	A3
2154	C1	2328	C2	3166	B2	3518	A2
2155	C1	2329	D2	3167	B1	3519	A3
2156	C1	2330	D2	3168	B1	3520	A3
2157	C1	2331	D2	3169	B1	3521	A3
2158	A1	2400	B3	3170	B1	3522	B3
2159	A1	2401	B3	3171	B1	3523	B3
2160	A1	2402	B3	3172	B1	3524	B2
2161	B1	2403	B3	3173	A1	3525	A3
2162	B1	2404	B3	3174	B1	4101	B2
2163	A1	2405	B3	3175	B1	4200	B3
2164	B1	2406	C3	3176	B1	4206	B3
2165	B1	2407	C3	3177	A1	4207	B3
2166	B1	2408	C3	3178	A1	4300	C1
2167	B1	2409	C3	3179	B1	4301	C1
2168	B1	2410	C3	3180	A1	4302	C1
2169	B1	2411	C3	3181	B1	4303	C1
2170	A1	2412	C3	3182	A1	4304	C1
2171	B1	2413	C3	3183	B1	4500	A3
2172	A1	2414	C3	3184	A1	4501	A3
2173	B1	2415	C3	3185	A1	4502	A3
2174	B1	2416	D3	3186	B1	4503	A3
2175	A1	2417	C3	3187	A1	5103	C1
2176	B1	2418	C3	3188	B1	5106	B1
2177	A1	2419	D3	3189	B1	5107	B2
2178	A1	2420	D3	3190	B1	5108	B2
2179	A1	2421	D3	3191	B1	5109	A1
2180	B1	2500	A3	3192	C1	5110	B1
2181	A1	2501	A3	3193	B1	5200	B3
2182	B1	2502	A3	3194	B1	5201	A3
2183	B1	2503	A3	3195	B1	5300	C2
2184	B1	2504	A3	3196	B1	5301	D3
2185	B1	2505	A2	3197	C1	5302	B2
2186	B1	2506	A2	3198	C1	5303	C3
2187	B1	2507	A2	3199	C1	5304	C2
2188	B1	2508	A2	3201	A3	5400	C3
2189	B2	2509	B3	3214	B3	5401	C3
2190	A2	2510	B3	3215	B3	5402	C3
2200	A3	2511	B3	3216	B3	5403	C3
2201	B2	2512	B3	3217	B3	5404	C3
2202	B3	2513	B3	3221	B3	5500	A3
2203	B2	2514	A3	3223	B1	5501	A3
2204	B2	2515	A3	3224	A3	5502	A2
2205	A3	2516	A2	3300	B2	5503	A2
2206	B3	2517	A3	3301	C1	6201	B3
2207	A3	2518	A2	3303	C1	6300	C3
2300	C1	2519	A2	3304	C1	7100	B2
2301	D3	2520	A3	3305	C1	7101	A1
2302	C3	3100	C1	3306	C1	7103	B1
2303	C3	3101	C1	3307	C1	7105	B1
2304	D2	3102	B1	3312	C2	7106	A2
2305	D3	3103	B1	3313	B2	7200	B2
2306	C2	3104	C1	3314	C2	7201	B2
2307	C2	3105	B1	3315	D2	7202	B3
2308	C2	3106	B1	3316	B2	7203	B3
2309	B2	3107	B1	3317	D2	7204	B2
2310	B2	3108	B1	3318	D3	7206	B1
2311	B2	3109	C1	3319	D3	7207	A3
2312	C1	3110	C1	3320	C3	7208	B2

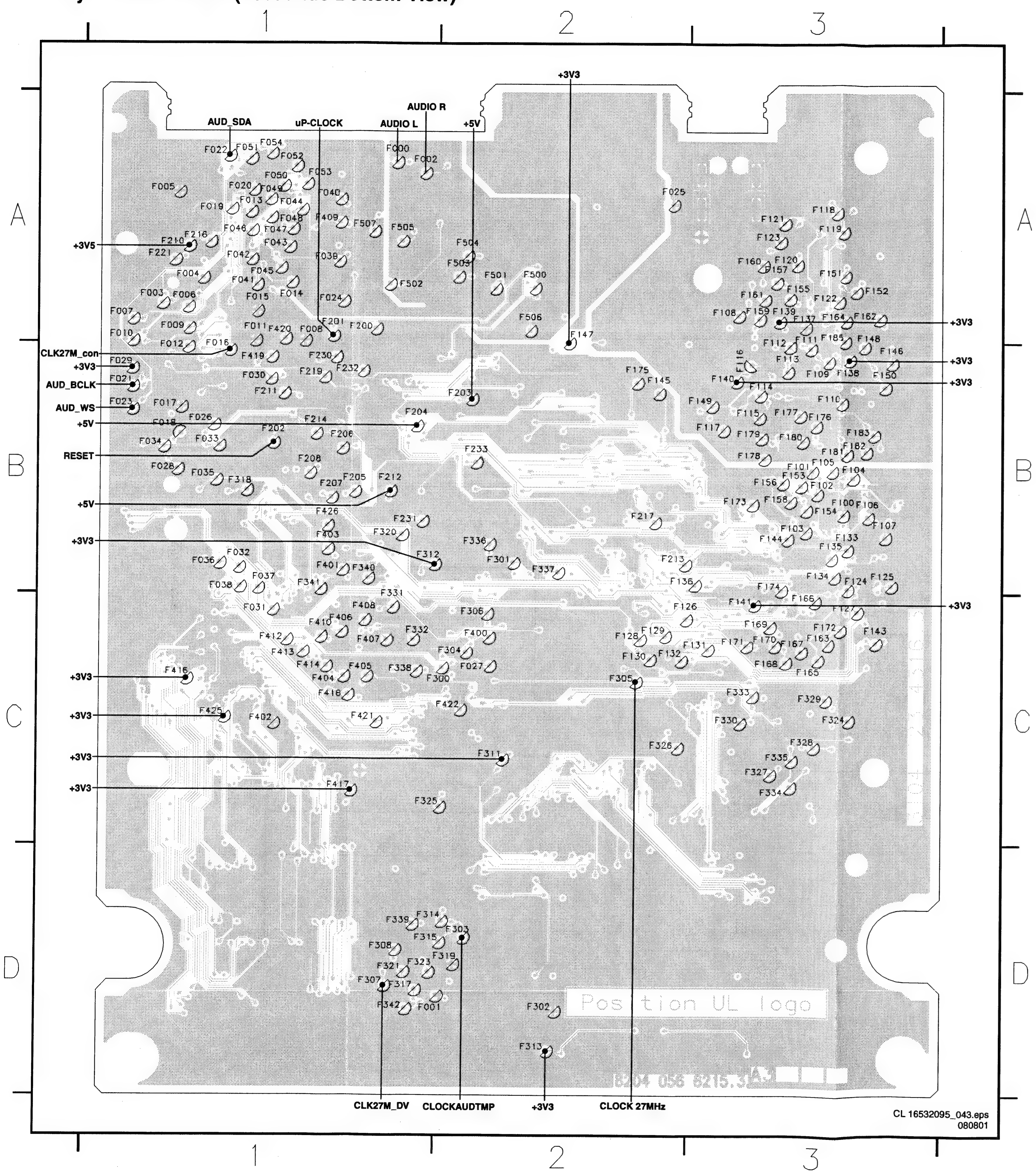
Layout DVIO Board (Part 1 Top View)



Layout DVIO Board (Part 2 Top View)



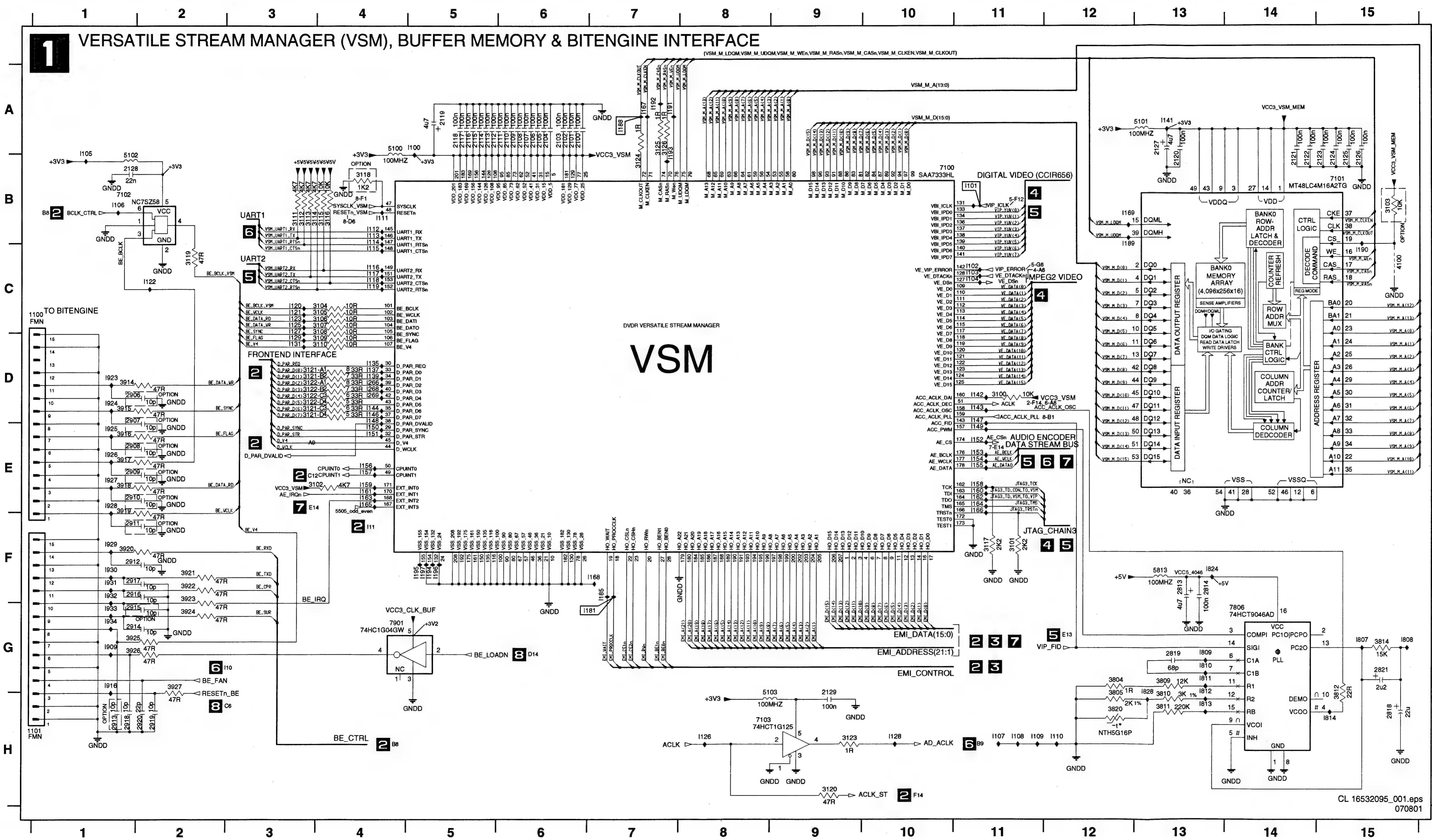
Layout DVIO Board (Testlands Bottom View)



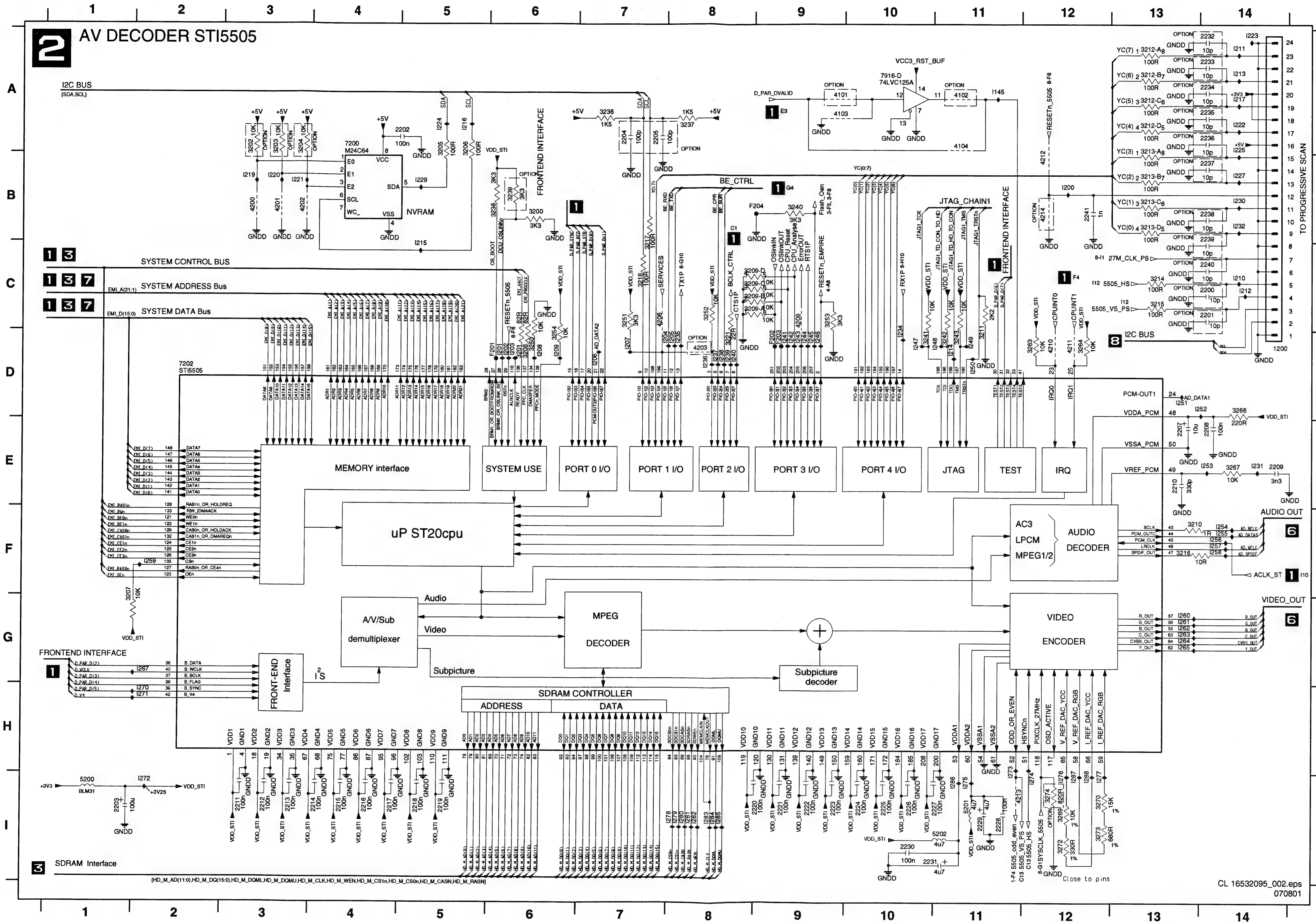
F001	D2	F114	B3	F185	A3	F407	C1
F0010	A1	F115	B3	F200	A1	F408	C1
F002	A1	F116	B3	F201	A1	F409	A1
F003	A1	F117	B3	F202	B1	F410	C1
F004	A1	F118	A3	F203	B2	F412	C1
F005	A1	F119	A3	F204	B1	F413	C1
F006	A1	F120	A3	F205	B1	F414	C1
F007	A1	F121	A3	F206	B1	F416	C1
F008	A1	F122	A3	F207	B1	F417	C1
F009	A1	F123	A3	F208	B1	F418	C1
F010	A1	F124	B3	F210	A1	F419	B1
F011	A1	F125	B3	F211	B1	F420	A1
F012	B1	F126	C2	F212	B1	F421	C1
F013	A1	F127	C3	F213	B2	F422	C2
F014	A1	F128	C2	F214	B1	F425	C1
F015	A1	F129	C2	F216	A1	F426	B1
F016	B1	F130	C2	F217	B2	F500	A2
F017	B1	F131	C3	F219	B1	F501	A2
F018	B1	F132	C2	F221	A1	F502	A1
F019	A1	F133	B3	F230	B1	F503	A2
F020	A1	F134	B3	F231	B1	F504	A2
F021	B1	F135	B3	F232	B1	F505	A1
F022	A1	F136	B3	F233	B2	F506	A2
F023	B1	F137	A3	F300	C2	F507	A1
F024	A1	F138	B3	F301	B2		
F025	A2	F139	A3	F302	D2		
F026	B1	F140	B3	F303	D2		
F027	C2	F141	C3	F304	C2		
F028	B1	F143	C3	F305	C2		
F029	B1	F144	B3	F306	C2		
F030	B1	F145	B2	F307	D1		
F031	C1	F146	B3	F308	D1		
F032	B1	F147	A2	F311	C2		
F033	B1	F148	B3	F312	B1		
F034	B1	F149	B3	F313	D2		
F035	B1	F150	B3	F314	D2		
F036	B1	F151	A3	F315	D2		
F037	B1	F152	A3	F317	D1		
F038	B1	F153	B3	F318	B1		
F039	A1	F154	B3	F319	D2		
F040	A1	F155	A3	F320	B1		
F041	A1	F156	B3	F321	D1		
F042	A1	F157	A3	F323	D1		
F043	A1	F158	B3	F324	C3		
F044	A1	F159	A3	F325	C2		
F045	A1	F160	A3	F326	C2		
F046	A1	F161	A3	F327	C3		
F047	A1	F162	A3	F328	C3		
F048	A1	F163	C3	F329	C3		
F049	A1	F164	A3	F330	C3		
F050	A1	F165	C3	F331	C1		
F051	A1	F166	C3	F332	C1		
F052	A1	F167	C3	F333	C3		
F053	A1	F168	C3	F334	C3		
F054	A1	F169	C3	F335	C3		
F100	B3	F170	C3	F336	B2		
F101	B3	F171	C3	F337	B2		
F102	B3	F172	C3	F338	C1		
F103	B3	F173	B3	F339	D1		
F104	B3	F174	B3	F340	B1		
F105	B3	F175	B2	F341	B1		
F106	B3	F176	B3	F342	D1		
F107	B3	F177	B3	F400	C2		
F108	A3	F178	B3	F401	B1		
F109	B3	F179	B3	F402	C1		
F110	B3	F180	B3	F403	B1		
F111	B3	F181	B3	F404	C1		
F112	B3	F182	B3	F405	C1		
F113	B3	F183	B3	F406	C1		

Digital Board: VSM, Buffer Memory and Bit Engine Interface

1100 C1	2106 A6	2114 A5	2122 B14	2813 F13	2909 E1	2917 F1	3104 C4	3112 B3	3120 H9	3122-D D3	3810 H13	3917 E1	3925 G1	5813 F13	I101 B11	I109 H11	I117 C4	I126 H8	I141 A13	I150 E4	I158 E11	I166 E11	I190 C15	I266 D4	I812 G13	I924 D1	I932 F1
1101 H1	2107 A6	2115 A5	2123 B15	2814 F13	2910 E1	2918 H1	3105 C4	3113 B3	3121-A D3	3123 H9	3811 H13	3918 E1	3926 G1	7100 B11	I102 C11	I110 H12	I118 C4	I127 C3	I142 D11	I151 E4	I159 E4	I167 A7	I191 A7	I268 D4	I813 H13	I925 E1	I933 G1
2100 A6	2108 A6	2116 A5	2124 B15	2818 H15	2911 F1	2919 H2	3106 C4	3114 B3	3121-B D3	3124 B7	3812 H15	3919 F1	3927 G2	7101 B15	I103 C11	I111 B4	I119 C4	I128 H10	I143 D11	I152 E11	I160 E11	I168 F7	I192 A7	I269 D4	I814 H15	I926 E1	I934 G1
2101 A6	2109 A6	2117 A5	2125 B15	2819 G13	2912 F1	2920 H2	3107 C4	3115 B4	3121-C D3	3125 A7	3814 G15	3920 F1	4100 C15	7102 B1	I104 C11	I112 B4	I120 C3	I129 D3	I144 D4	I153 E11	I161 E4	I169 B12	I193 A7	I807 G15	I824 F13	I927 E1	
2102 A6	2110 A6	2118 A5	2126 B15	2821 G15	2913 H1	3100 D11	3108 D4	3116 B4	3121-D D3	3126 A7	3820 H12	3921 F2	5100 A4	7103 H8	I105 A1	I113 B4	I121 C3	I131 D3	I146 D4	I154 E11	I162 E11	I181 G7	I194 F5	I808 G15	I828 G13	I928 E1	
2103 A6	2111 A5	2119 A5	2127 A13	2906 D1	2914 G1	3101 F11	3109 D4	3117 F11	3122-A D3	3804 G12	3914 D1	3922 F2	5101 A13	7806 G14	I106 B1	I114 B4	I122 C2	I135 D4	I147 D11	I155 E11	I163 E4	I185 G7	I195 F5	I809 G13	I909 G1	I929 F1	
2104 A6	2112 A5	2120 B13	2128 B1	2907 D1	2915 G1	3102 E3	3110 D4	3118 B4	3122-B D3	3805 H12	3915 D1	3923 F2	5102 B1	7901 G4	I107 H11	I115 C4	I123 C3	I137 D4	I148 D4	I156 E4	I164 E11	I188 A7	I196 F5	I810 G13	I916 G1	I930 F1	
2105 A6	2113 A5	2121 B14	2129 H9	2908 E1	2916 F1	3103 B15	3111 B3	3119 C2	3122-C D3	3809 G13	3916 E1	3924 G2	5103 H9	I100 A5	I108 H11	I116 C4	I125 C3	I139 D4	I149 E11	I157 E4	I165 E4	I189 C12	I197 F5	I811 G13	I923 D1	I931 F1	



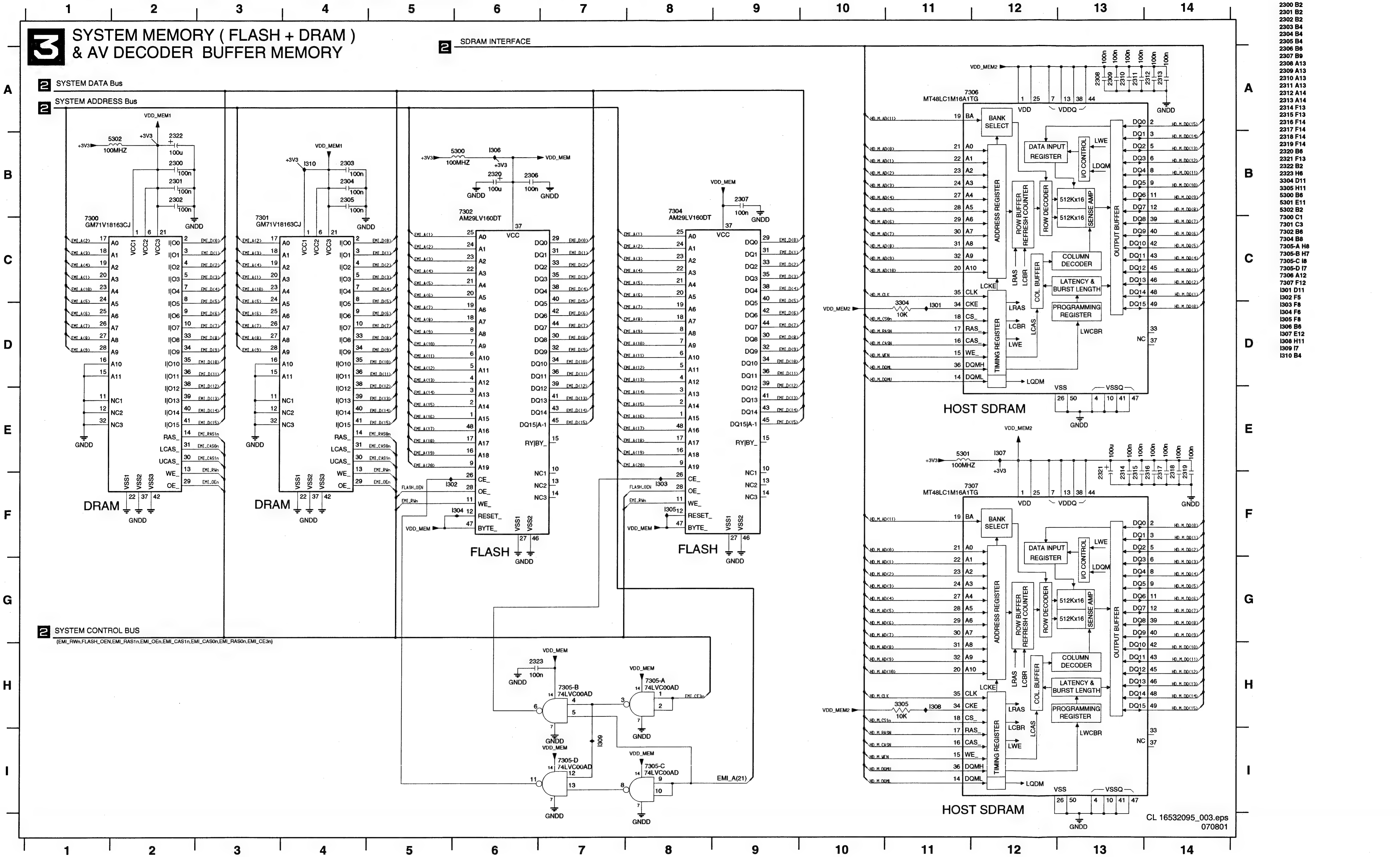
Digital Board: AV Decoder STI5505



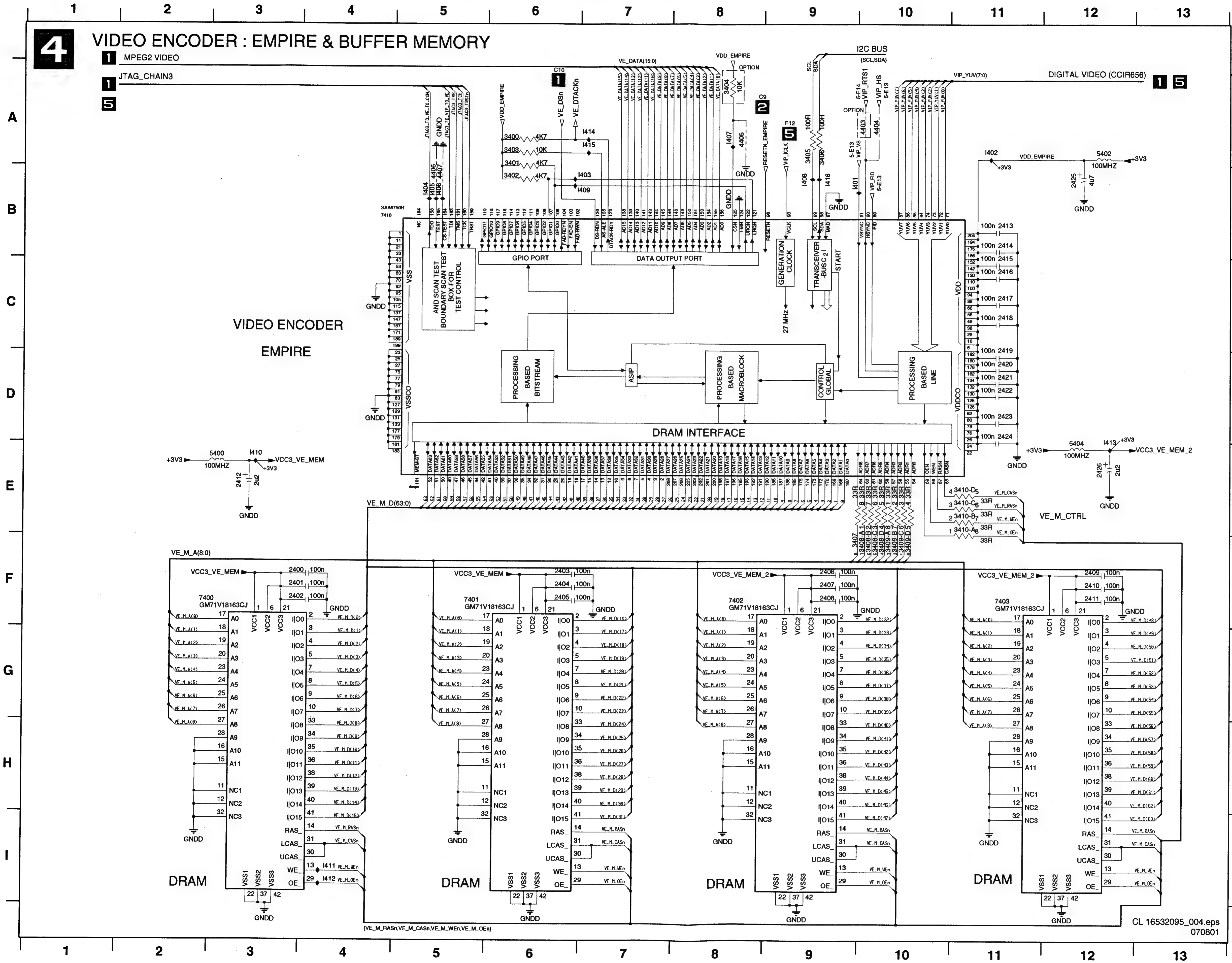
1200 D14
2200 C14
2201 C14
2202 A5
2203 I1
2204 A7
2205 A7
2207 E13
2208 E14
2209 E14
2210 E13
2211 I3
2212 I3
2213 I3
2214 I4
2215 I4
2216 I4
2217 I4
2218 I5
2219 I5
2220 I9
2221 I9
2222 I9
2223 I9
2224 I10
2225 I10
2226 I10
2227 I11
2228 I11
2229 I11
2230 I10
2231 I10
2232 A14
2233 A14
2234 A14
2235 A14
2236 A14
2237 B14
2238 B14
2239 B14
2240 C14
2241 B12
3200 B6
3201 D6
3202 A3
3203 A3
3204 A3
3205 A5
3206 A5
3207 G1
3208 D6
3209-A C8
3209-B C8
3209-C C8
3209-D C8
3210 F13
3211 D11
3212-A A13
3212-B A13
3212-C A13
3212-D A13
3213-A A13
3213-B B13
3213-C B13
3213-D B13
3214 C13
3215 C13
3216 F13
3217 C7
3218 C7
3221 D8
3236 A7
3237 A8
3238 B6
3239 B6
3240 B9
3241 D10
3242 D11
3243 D11
3250 D6
3251 C7
3252 C8
3253 C9
3254 D6
3263 D12
3264 D12
3266 D14
3267 E14
3269 I12
3270 I12
3272 I12
3273 I12
3274 I12
4101 A9
4102 A11
4103 A9
4104 A11
4200 B3
4201 B3
4202 B3
4203 D8
4206 C7
4209 C9
4210 D12
4211 D12
4212 B12
4213 I11
4214 B12
5200 I1
5201 I11
5202 I11
7200 A4
7202 D2
7916-D A10
F201 D6
F202 D9
F203 D9
F204 B9

I145 A11
I200 B12
I201 D6
I202 D6
I203 D6
I204 D7
I205 D8
I206 D7
I207 D7
I208 D6
I209 D6
I210 C14
I211 A14
I212 C14
I213 A14
I214 D11
I215 C5
I216 A5
I217 A14
I219 B3
I220 B3
I221 B3
I222 A14
I223 A14
I224 A5
I225 A14
I227 B14
I229 B5
I230 B14
I231 E14
I232 B14
I234 D10
I235 D8
I236 D8
I237 D8
I238 D8
I239 D8
I240 D8
I241 D9
I242 D9
I243 D9
I244 D9
I245 D9
I246 D9
I247 D10
I248 D11
I249 D11
I250 D11
I251 D13
I252 D14
I253 E14
I254 F14
I255 F14
I256 F14
I257 F14
I258 F14
I259 F2
I260 G13
I261 G13
I262 G13
I263 G13
I264 G13
I265 G13
I267 G2
I270 H2
I271 H2
I272 I2
I273 H11
I274 I12
I275 I11
I276 I12
I277 I12
I278 I8
I279 I8
I280 I8
I281 I8
I282 I8
I283 I8
I284 I8
I285 I8
I286 I11
I287 I12
I288 I12

Digital Board: System Memory & AV Decoder Buffer Memory

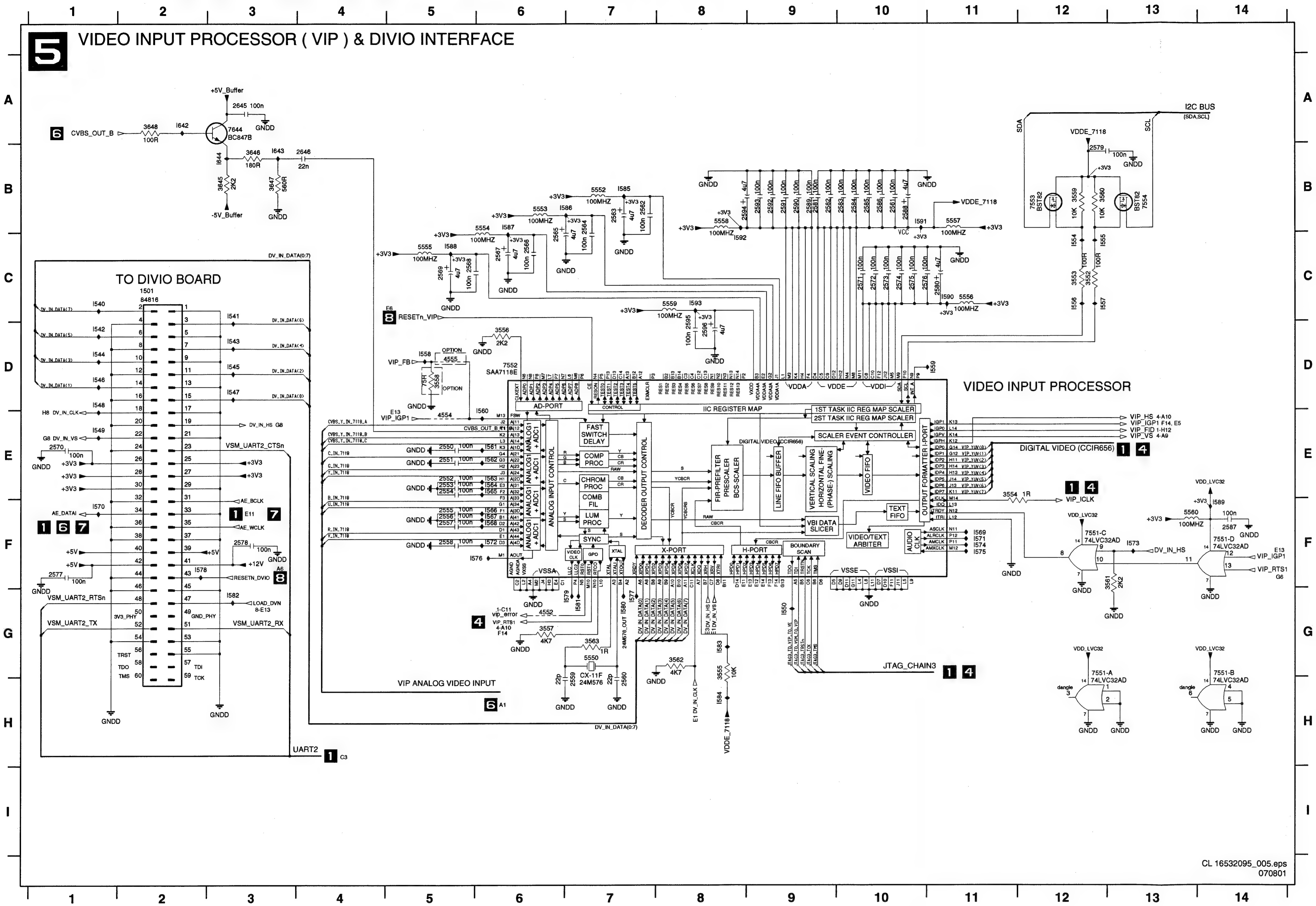


Digital Board: Video Encoder, Empire & Buffer Memory



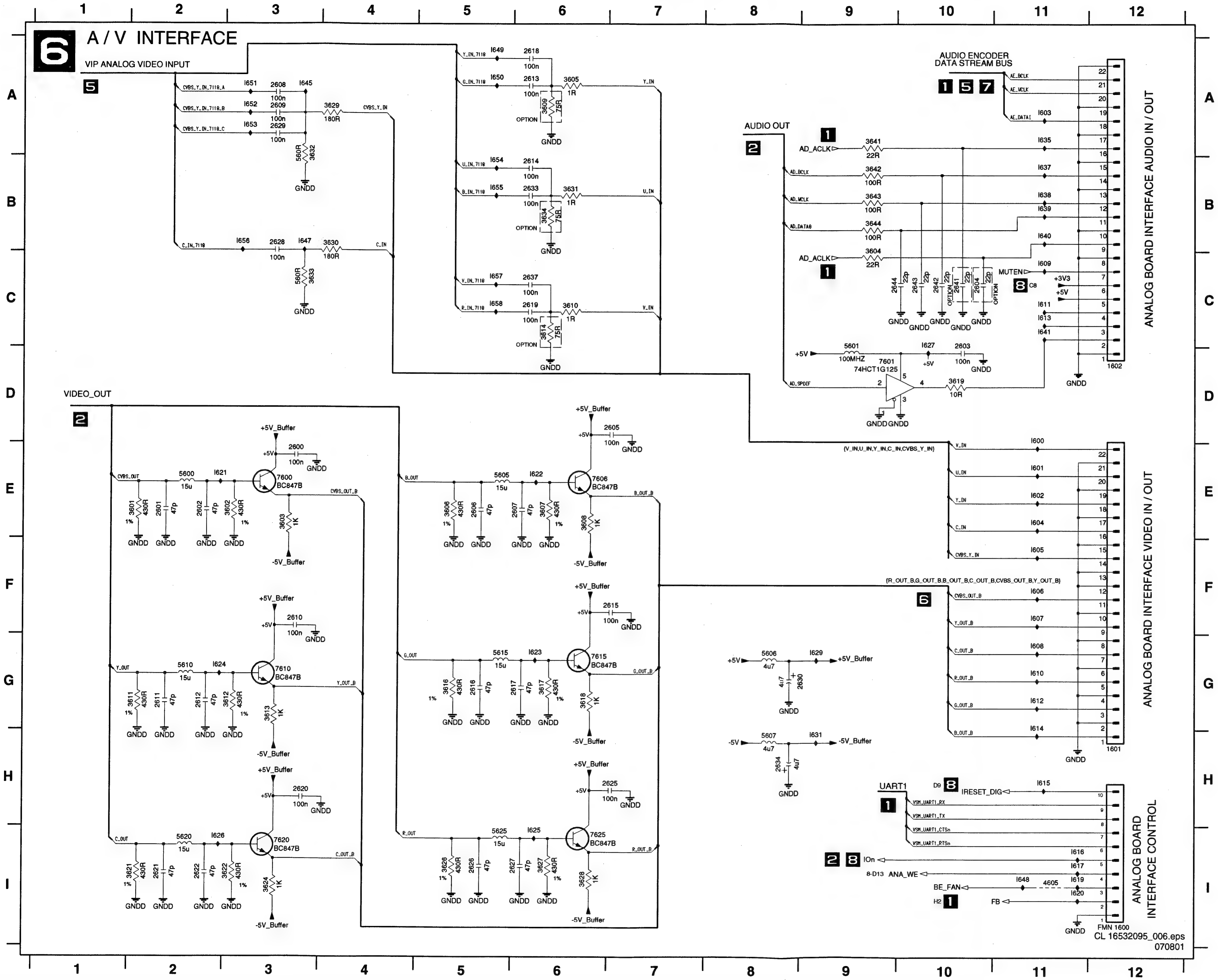
2400 F3
2401 F3
2402 F3
2403 F6
2404 F6
2405 F6
2406 F9
2407 F9
2408 F9
2409 F12
2410 F12
2411 F12
2412 E3
2413 B11
2414 B11
2415 C11
2416 C11
2417 C11
2418 C11
2419 D11
2420 D11
2421 D11
2422 D11
2423 D11
2424 D11
2425 B12
2426 E12
3400 A6
3401 A6
3402 B6
3403 A6
3404 A8
3405 A9
3406 A9
3407 F9
3408 F10
3408 F10
3408 F10
3408 F10
3409 F10
3409 F10
3409 F10
3409 F10
3410 E11
3410 E11
3410 E11
3410 E11
4403 A10
4404 A10
4405 A8
4406 B5
4407 B5
5400 E3
5402 A12
5404 E12
7400 F2
7401 F5
7402 F8
7403 F11
7410 B4
I401 B9
I402 A11
I403 B7
I404 B5
I405 B5
I406 B5
I407 A8
I408 B9
I409 B7
I410 E3
I411 I4
I412 I4
I413 D12
I414 A7
I415 A7
I416 B9

Digital Board: Video Input Processor (VIP) & DVIO Interface



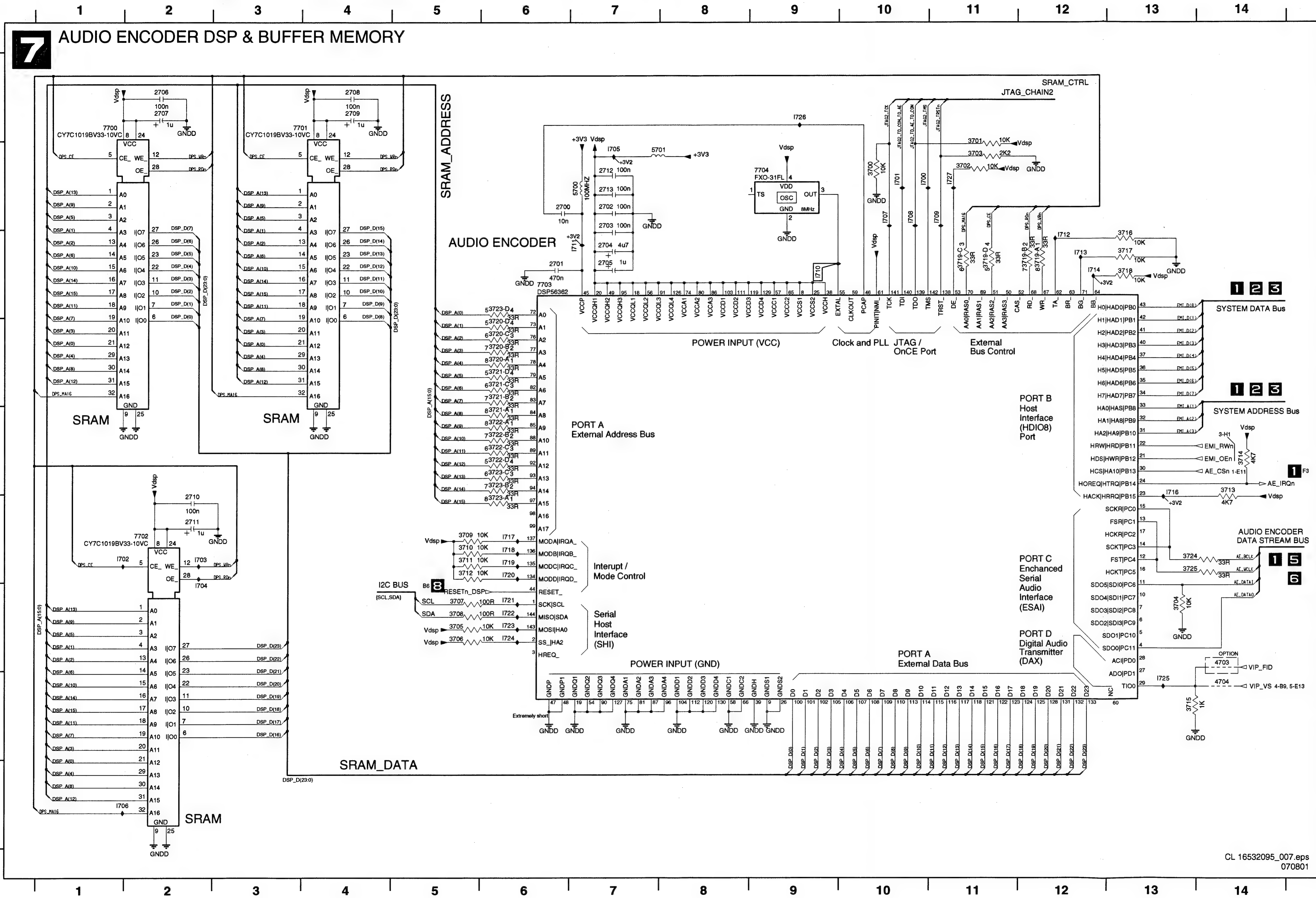
1501 C2	I571 F11
2550 E5	I572 F6
2551 E5	I573 F13
2552 E5	I574 F11
2553 E5	I575 F11
2554 E5	I576 F6
2555 F5	I577 G7
2556 F5	I578 F2
2557 F5	I579 G7
2558 F5	I580 G7
2559 H7	I581 G7
2560 H7	I582 G3
2561 B10	I583 G8
2562 B7	I584 H8
2563 B7	I585 B7
2564 B7	I586 B6
2565 C6	I587 B6
2566 C6	I588 C5
2567 C6	I589 F14
2568 C5	I590 C11
2569 C5	I591 B10
2570 E1	I592 C8
2571 C10	I593 C8
2572 C10	I642 A2
2573 C10	I643 B3
2574 C10	I644 B3
2575 C10	
2576 C10	
2577 F1	
2578 F3	
2579 B12	
2580 C11	
2581 B9	
2582 B9	
2583 B10	
2584 B10	
2585 B10	
2586 B10	
2587 F14	
2588 B10	
2589 B9	
2590 B9	
2591 B9	
2592 B9	
2593 B9	
2594 B8	
2595 D8	
2596 D8	
2645 A3	
2646 B4	
3552 C12	
3553 C12	
3554 E11	
3555 G8	
3556 D6	
3557 G6	
3558 D5	
3559 B12	
3560 B12	
3561 F13	
3562 G8	
3563 G7	
3645 B3	
3646 B3	
3647 B3	
3648 A2	
4552 G6	
4554 E5	
4555 D5	
5550 G7	
5552 B7	
5553 B6	
5554 B6	
5555 C5	
5556 C11	
5557 B11	
5558 B8	
5559 C8	
5560 F13	
7551-A G13	
7551-B G14	
7551-C F12	
7551-D F14	
7552 D6	
7553 B12	
7554 B13	
7644 A3	
I540 C1	
I541 C3	
I542 D1	
I543 D3	
I544 D1	
I545 D3	
I546 D1	
I547 D3	
I548 D1	
I549 E1	
I550 G9	
I554 C12	
I555 C12	
I556 C12	
I557 C12	
I558 D5	
I559 D11	
I560 E6	
I561 E6	
I562 E6	
I563 E6	
I564 E6	
I565 E6	
I566 F6	
I567 F6	
I568 F6	
I569 F11	
I570 F1	

Digital Board: A / V Interface



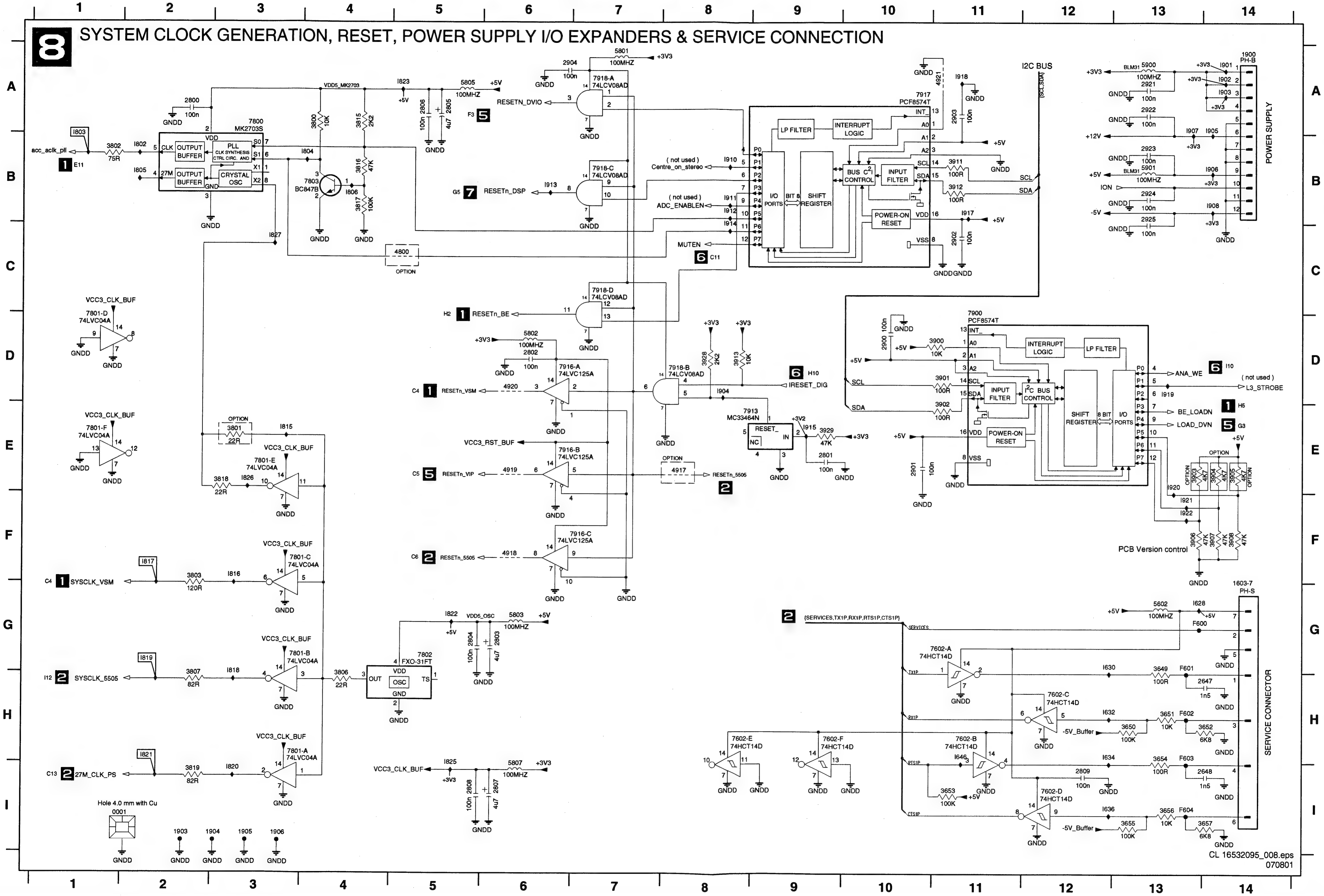
1600	I12	I627	C10
1601	H12	I629	G9
1602	D12	I631	H9
2600	E3	I635	A11
2601	E2	I637	B11
2602	E2	I638	B11
2603	D10	I639	B11
2604	C10	I640	B11
2605	D7	I641	C11
2606	E5	I645	A3
2607	E6	I647	B3
2608	A3	I648	I11
2609	A3	I649	A5
2610	F3	I650	A5
2611	G2	I651	A3
2612	G2	I652	A3
2613	A6	I653	A3
2614	B6	I654	B5
2615	F7	I655	B5
2616	G5	I656	B3
2617	G6	I657	C5
2618	A6	I658	C5
2619	C6		
2620	H3		
2621	I2		
2622	I2		
2625	H7		
2626	I5		
2627	I6		
2628	B3		
2629	A3		
2630	G8		
2633	B6		
2634	H8		
2637	C6		
2641	C10		
2642	C10		
2643	C10		
2644	C9		
3601	E2		
3602	E3		
3603	E3		
3604	C9		
3605	A6		
3606	E5		
3607	E6		
3608	E6		
3609	A6		
3610	C6		
3611	G2		
3612	G3		
3613	G3		
3614	C6		
3616	G5		
3617	G6		
3618	G6		
3619	D10		
3621	I2		
3622	I3		
3624	I3		
3626	I5		
3627	I6		
3628	I6		
3629	A4		
3630	B4		
3631	B6		
3632	A3		
3633	C3		
3634	B6		
3641	A9		
3642	B9		
3643	B9		
3644	B9		
4605	I11		
5600	E2		
5601	D9		
5605	E5		
5606	G8		
5607	H8		
5610	G2		
5615	G5		
5620	I2		
5625	I5		
7600	E3		
7601	D9		
7606	E6		
7610	G3		
7615	G6		
7620	I3		
7625	I6		
I600	D11		
I601	E11		
I602	E11		
I603	A11		
I604	E11		
I605	F11		
I606	F11		
I607	F11		
I608	G11		
I609	C11		
I610	G11		
I611	C11		
I612	G11		
I613	C11		
I614	G11		
I615	H11		
I616	I11		
I617	I11		
I619	I11		
I620	I11		
I621	E2		
I622	E6		
I623	G6		
I624	G2		
I625	I6		
I626	I2		

Digital Board: Audio Encoder DSP & Buffer Memory



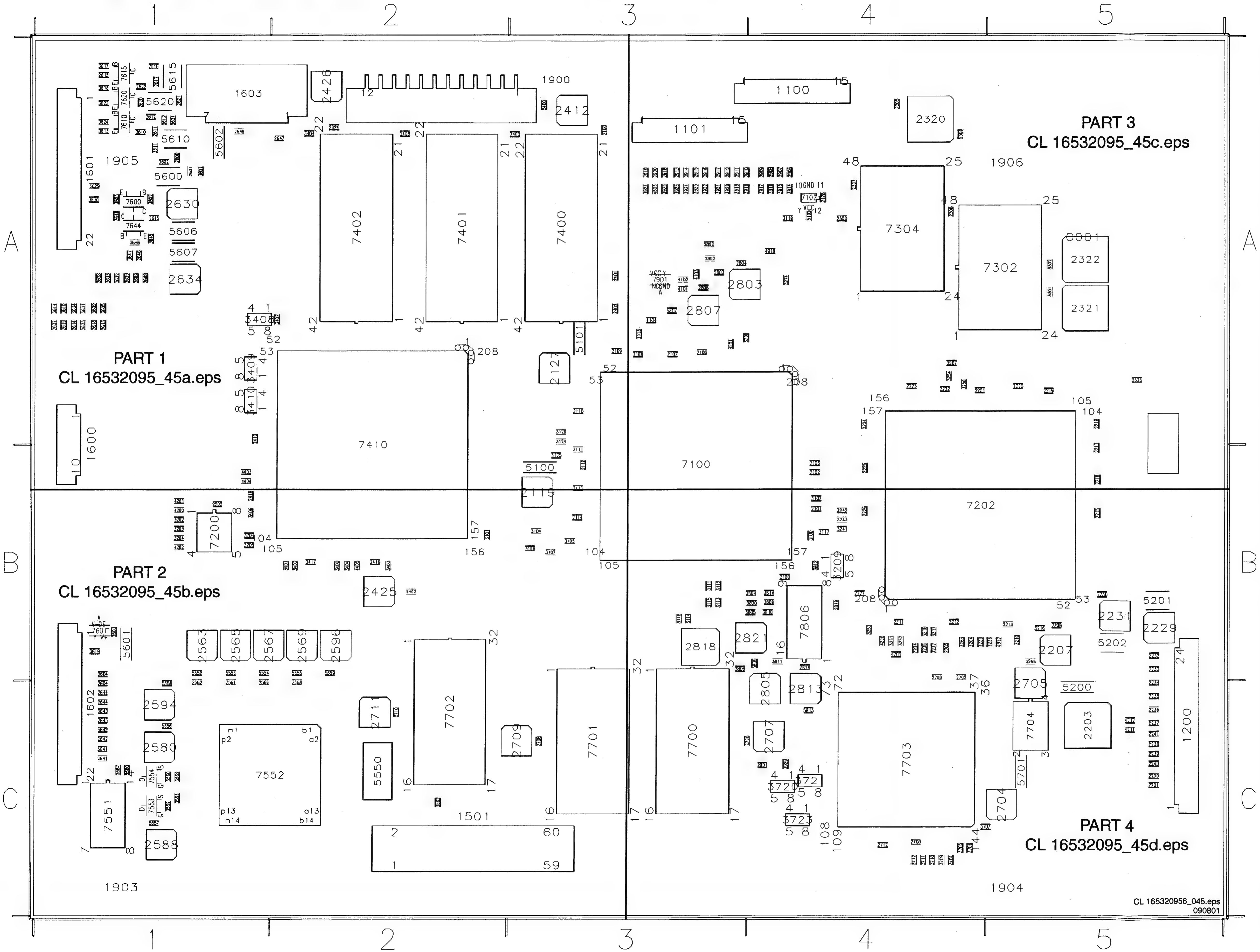
2700 B6
2701 C6
2702 B7
2703 B7
2704 C7
2705 C7
2706 A2
2707 A2
2708 A4
2709 A4
2710 F2
2711 F2
2712 B7
2713 B7
3700 B10
3701 B11
3702 B11
3703 B11
3704 G13
3705 G5
3706 G5
3707 G5
3708 G5
3709 F5
3710 F5
3711 F5
3712 F5
3713 E14
3714 E14
3715 H13
3716 C13
3717 C13
3718 C13
3719-A C12
3719-B C12
3719-C C11
3719-D C11
3720-A D6
3720-B D6
3720-C D6
3720-D D6
3721-A E6
3721-B D6
3721-C D6
3721-D D6
3722-A E6
3722-B E6
3722-C E6
3722-D E6
3723-A F6
3723-B E6
3723-C E6
3723-D C6
3724 F13
3725 F13
4703 G14
4704 H14
5700 B7
5701 B7
7700 A1
7701 A4
7702 F2
7703 C6
7704 B9
I700 B10
I701 B10
I702 F1
I703 F2
I704 G2
I705 B7
I706 I1
I707 B10
I708 B10
I709 B11
I710 C9
I711 C7
I712 C12
I713 C12
I714 C12
I716 E13
I717 F6
I718 F6
I719 F6
I720 F6
I721 G6
I722 G6
I723 G6
I724 G6
I725 H13
I726 A9
I727 B11

Digital Board: System Clock Generation, Reset, Power Supply I/O Expanders & Service Connection



0001 I1	I802 B2
1603-7 G14	I803 B1
1900 A14	I804 B4
1903 I2	I805 B2
1904 I3	I806 B4
1905 I3	I815 E3
1906 I3	I816 F3
2647 H14	I817 F2
2648 I14	I818 G3
2800 A2	I819 G2
2801 E9	I820 I3
2802 D6	I821 I2
2803 G6	I822 G5
2804 G5	I823 A5
2805 A5	I825 H5
2806 A5	I826 E3
2807 I6	I827 C3
2808 I5	I901 A14
2809 I12	I902 A14
2900 D10	I903 A14
2901 E10	I904 D8
2902 C11	I905 A14
2903 A11	I906 B14
2904 A6	I907 A13
2921 A13	I908 B14
2922 A13	I910 B8
2923 B13	I911 B8
2924 B13	I912 B8
2925 B13	I913 B6
3649 G13	I914 B8
3650 H13	I915 E9
3651 H13	I917 B11
3652 H14	I918 A11
3653 I11	I919 D13
3654 H13	I920 E13
3655 I13	I921 F13
3656 I13	I922 F13
3657 I14	
3800 A4	
3801 E3	
3802 B1	
3803 F2	
3806 H4	
3807 H2	
3815 A4	
3816 B4	
3817 B4	
3818 E3	
3819 I2	
3900 D11	
3901 D11	
3902 E11	
3903 E13	
3904 E14	
3905 E14	
3906 F13	
3907 F14	
3908 F14	
3911 B11	
3912 B11	
3913 D8	
3928 D8	
3929 E9	
4800 C5	
4917 E8	
4918 F6	
4919 E6	
4920 D6	
4921 A11	
5602 G13	
5801 A7	
5802 D6	
5803 G6	
5805 A5	
5807 I6	
5900 A13	
5901 B13	
7602-A G10	
7602-B H11	
7602-C H12	
7602-D I12	
7602-E H9	
7602-F H10	
7800 A3	
7801-A H4	
7801-B G4	
7801-C F4	
7801-D D1	
7801-E E3	
7801-F E1	
7802 G5	
7803 B4	
7900 D11	
7913 E9	
7916-A D7	
7916-B E7	
7916-C F7	
7917 A10	
7918-A A7	
7918-B D8	
7918-C B7	
7918-D C7	
F600 G13	
F601 G13	
F602 H13	
F603 H13	
F604 I13	
I628 G13	
I630 G12	
I632 H12	
I634 H12	
I636 I12	
I646 H11	

Layout Digital Board (Overview Top View)



1100	A4	2600	A1	3202	B1	3916	A4
1101	A3	2601	A1	3203	B1	3917	A4
1200	C5	2602	A1	3204	B1	3918	A3
1501	C2	2603	B1	3205	B1	3919	A3
1600	A1	2604	C1	3206	B1	3920	A3
1601	A1	2608	A1	3207	A4	3921	A3
1602	C1	2609	A1	3208	A3	3922	A3
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1900	A3	2611	A1	3210	B5	3924	A3
2100	B4	2612	A1	3216	B5	3925	A3
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2110	A3	2620	A1	3242	B4	4200	B1
2111	B3	2621	A1	3243	B4	4201	B1
2112	B3	2622	A1	3250	A4	4202	B1
2113	B3	2628	A1	3251	B4	4203	B4
2114	B3	2629	A1	3252	B4	4206	B4
2119	B3	2630	A1	3253	B4	4212	C5
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2205	B4	2645	A1	3402	B2	5100	B3
2207	B5	2646	A1	3403	B2	5101	A3
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2213	B5	2702	B4	3408	A1	5202	B5
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2216	B5	2704	C5	3410	A1	5301	A5
2217	B5	2705	C5	3552	C1	5302	A5
2218	A5	2706	C4	3553	C1	5400	A3
2219	A5	2707	C4	3559	C1	5402	B2
2220	A5	2708	C3	3560	C1	5404	A2
2221	A4	2709	C3	3562	C2	5550	C2
2222	A4	2710	C2	3601	A1	5552	B1
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2224	A4	2712	C4	3603	A1	5554	B1
2225	B4	2801	C4	3604	B1	5555	B2
2226	B4	2802	A3	3605	A1	5556	C1
2227	B4	2803	A3	3609	A1	5557	C1
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2230	B5	2805	C4	3611	A1	5559	B2
2231	B5	2806	B3	3612	A1	5560	C1
2232	B5	2807	A3	3613	A1	5600	A1
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2234	C5	2813	C4	3617	A1	5602	A1
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2239	C5	2906	A4	3624	A1	5620	A1
2240	C5	2907	A4	3629	A1	5701	C5
2241	C5	2908	A4	3630	A1	5802	A3
2300	A4	2909	A4	3631	A1	5803	A3
2305	A4	2910	A3	3632	A1	5805	B4
2306	A4	2911	A3	3633	A1	5807	A3
2307	A4	2912	A3	3634	A1	5813	C4
2320	A4	2913	A3	3641	C1	7100	B3
2321	A5	2914	A3	3642	C1	7102	A4
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2400	A3	2917	A3	3645	A1	7302	A5
2401	A3	2918	A3	3646	A1	7304	A4
2402	A3	2919	A3	3647	A1	7400	A3
2403	A3	2920	A3	3648	A1	7401	A2
2406	A2	2924	A2	3701	C4	7402	A2
2412	A3	3100	B4	3705	C4	7410	A2
2416	B2	3101	B2	3707	C4	7551	C1
2417	B2	3102	B4	3708	C4	7552	C2
2418	B1	3104	B3	3709	C4	7553	C1
2419	A1	3105	B3	3710	C4	7554	C1
2425	B2	3106	B3	3711	C4	7600	A1
2426	A2	3107	B3	3712	C4	7601	B1
2562	C1	3111	B3	3720	C4	7610	A1
2563	B1	3112	B3	3721	C4	7615	A1
2564	C1	3113	B3	3723	C4	7620	A1
2565	B1	3114	B3	3804	B4	7644	A1
2566	C1	3115	B3	3805	B4	7700	C3
2567	B1	3116	B3	3809	B4	7701	C3
2568	C2	3117	B4	3810	B4	7702	C2
2569	B2	3118	A3	3811	B4	7703	C4
2580	C1	3119	A4	3812	B4	7704	C5
2587	C1	3124	A3	3814	B4	7806	B4
2588	C1	3125	B3	3820	B4	7901	A3
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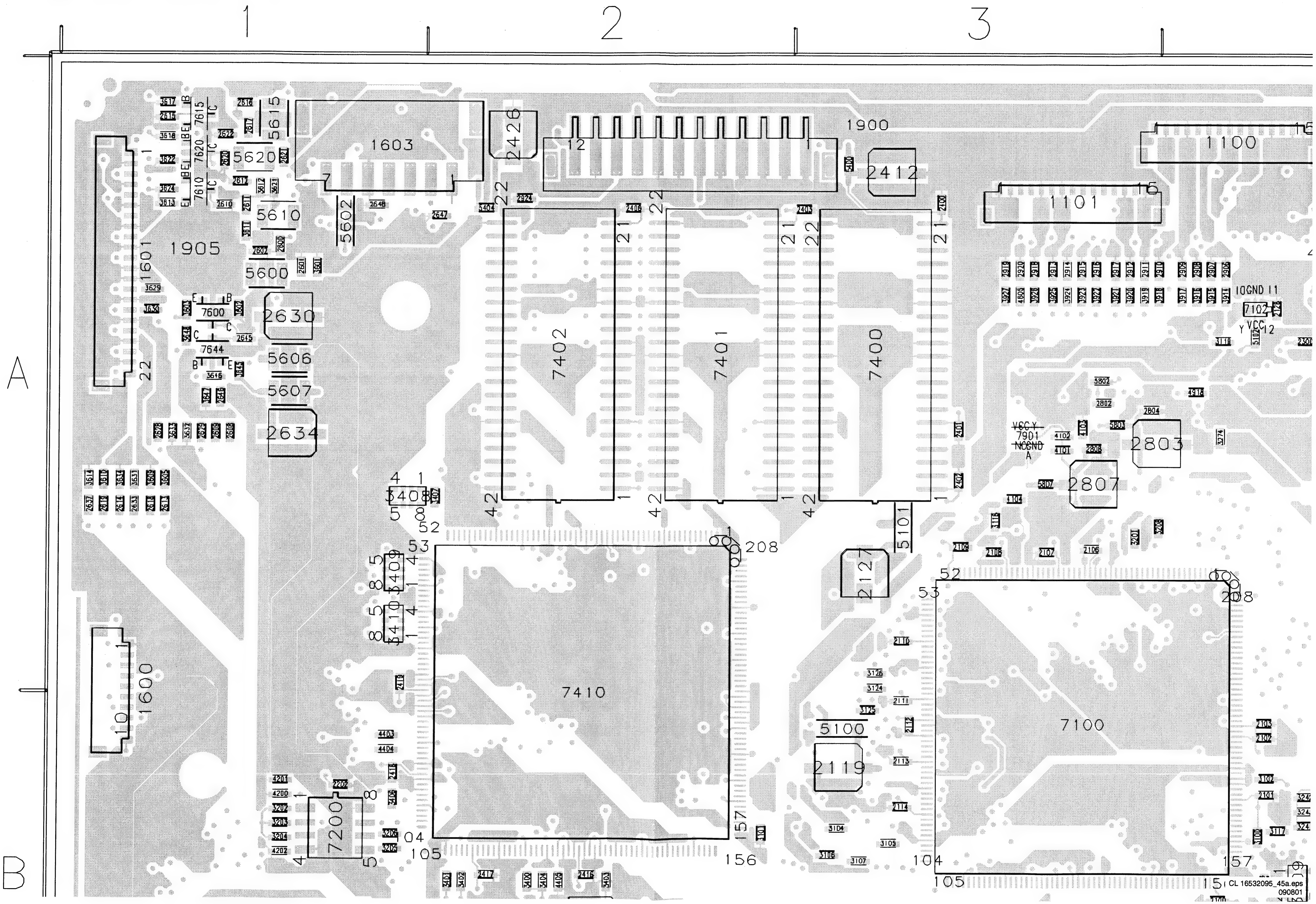
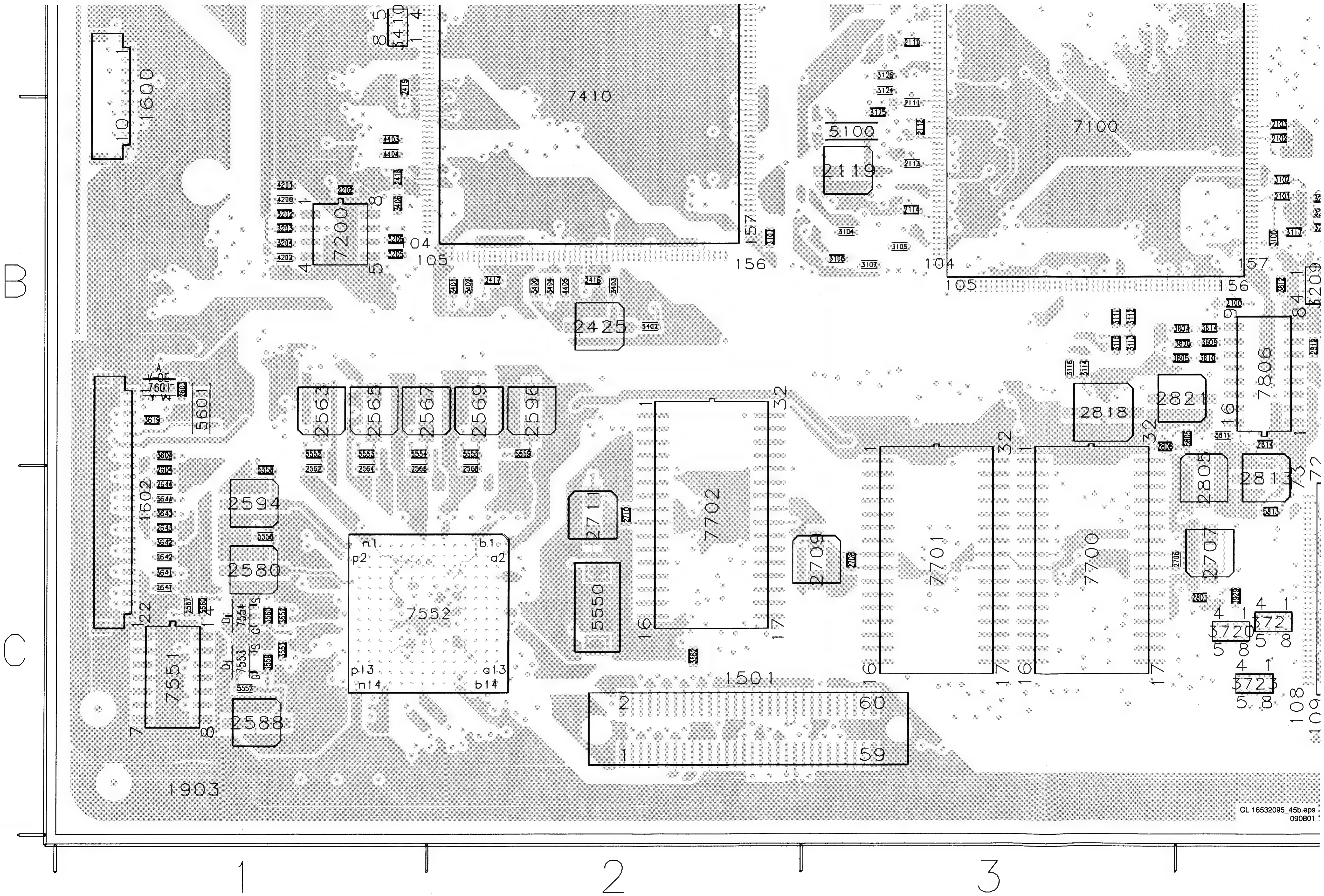
2596	B2	3201	A3	3915	A4		

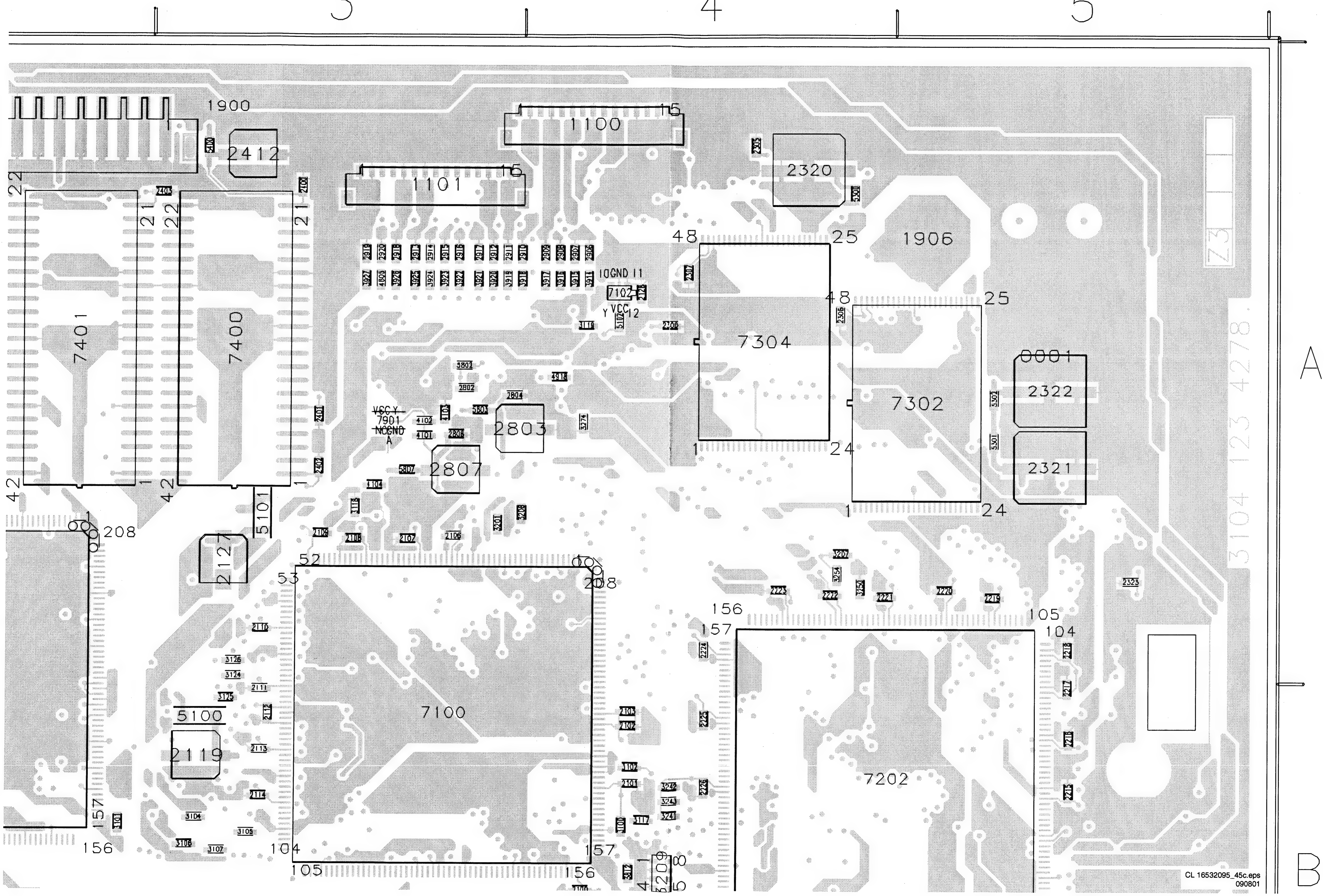
Layout Digital Board (Part 1 Top View)



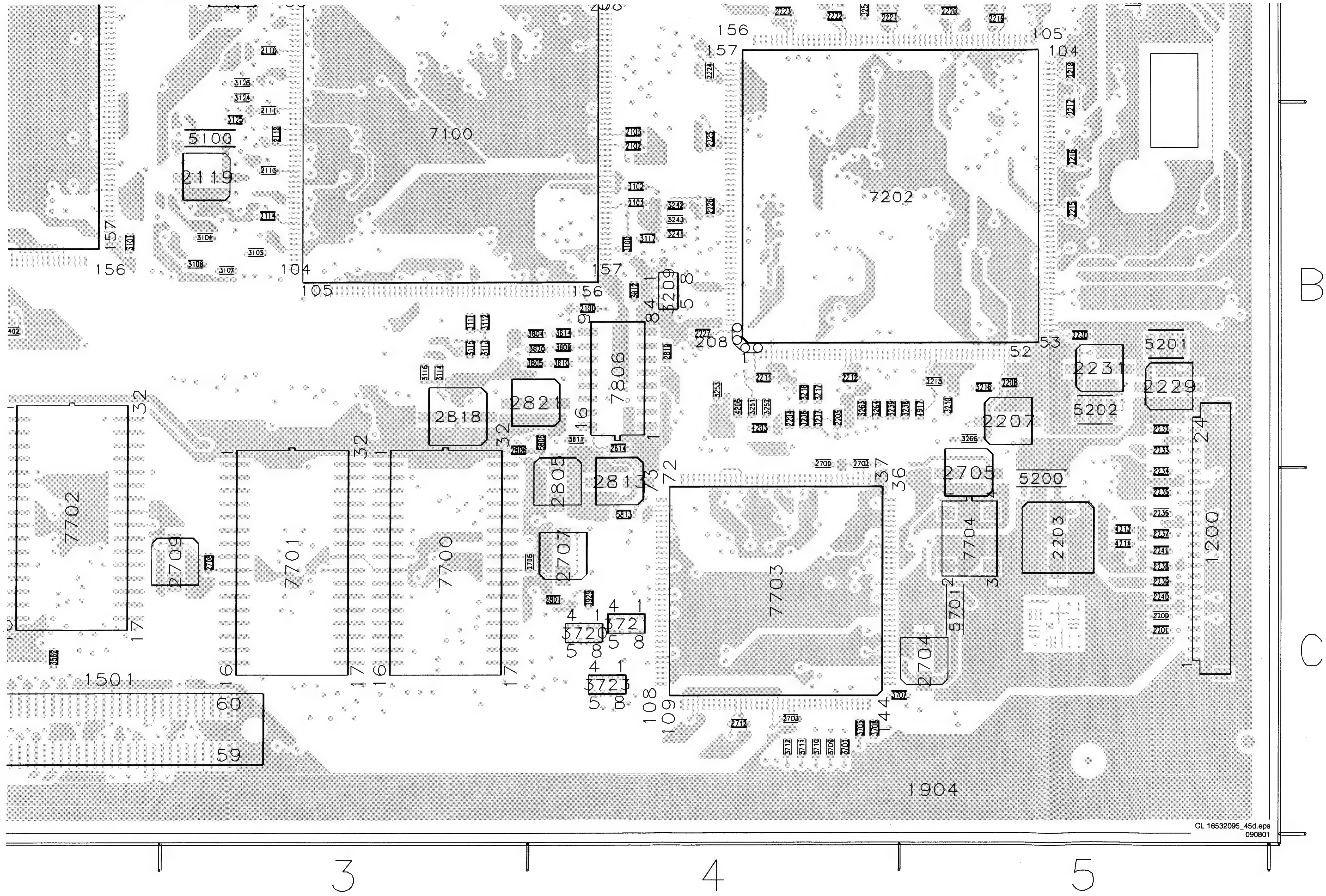
Layout Digital Board (Part 2 Top View)



Layout Digital Board (Part 3 Top View)



Layout Digital Board (Part 4 Top View)



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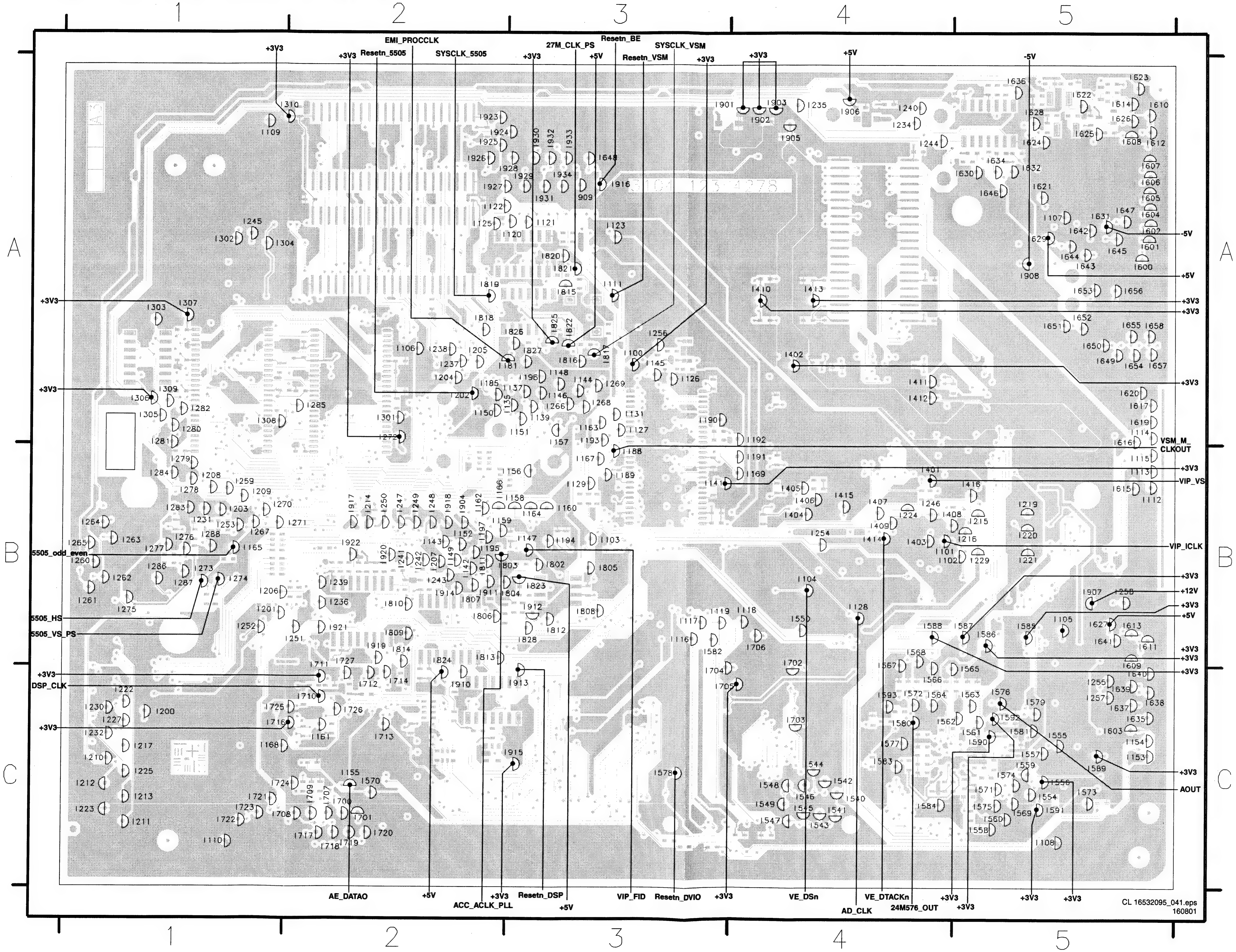
Layout Digital Board (Testlands Bottom View)



Layout Digital Board (Mapping Testlands)

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F604	A4
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I100	A3
I101	B4
I101	B4
I102	B4
I102	B5
I103	B3
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I104	B4
I104	B4
I105	B5
I105	B5
I106	A2
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I107	A5
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I925	A2
I926	A2
I926	A2
I927	A2
I927	A2
I928	A2
I928	A3
I929	A3
I929	A3
I930	A3
I930	A3
I931	A3
I931	A3
I932	A3
I932	A3
I933	A3
I933	A3
I934	A3
I934	A3

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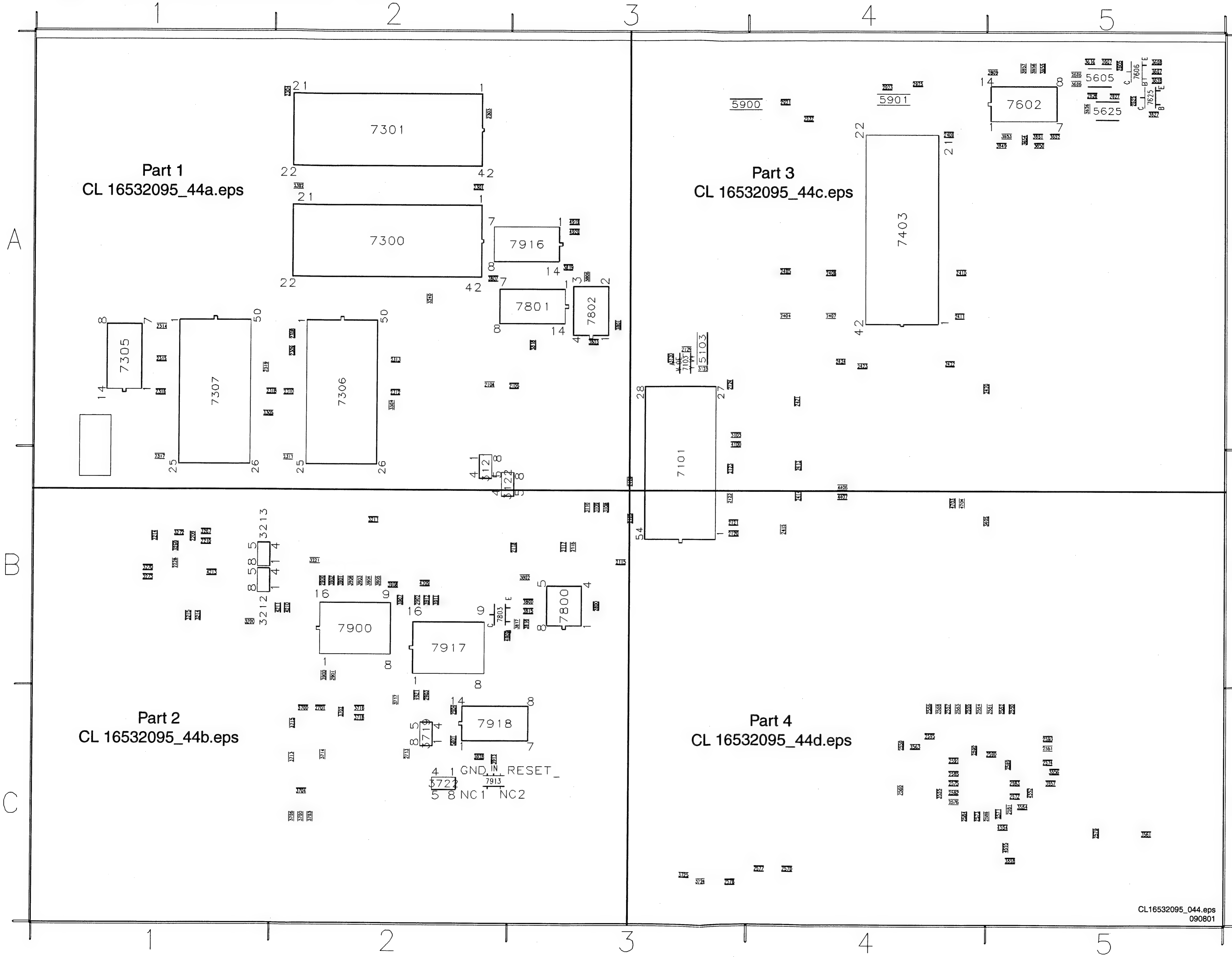
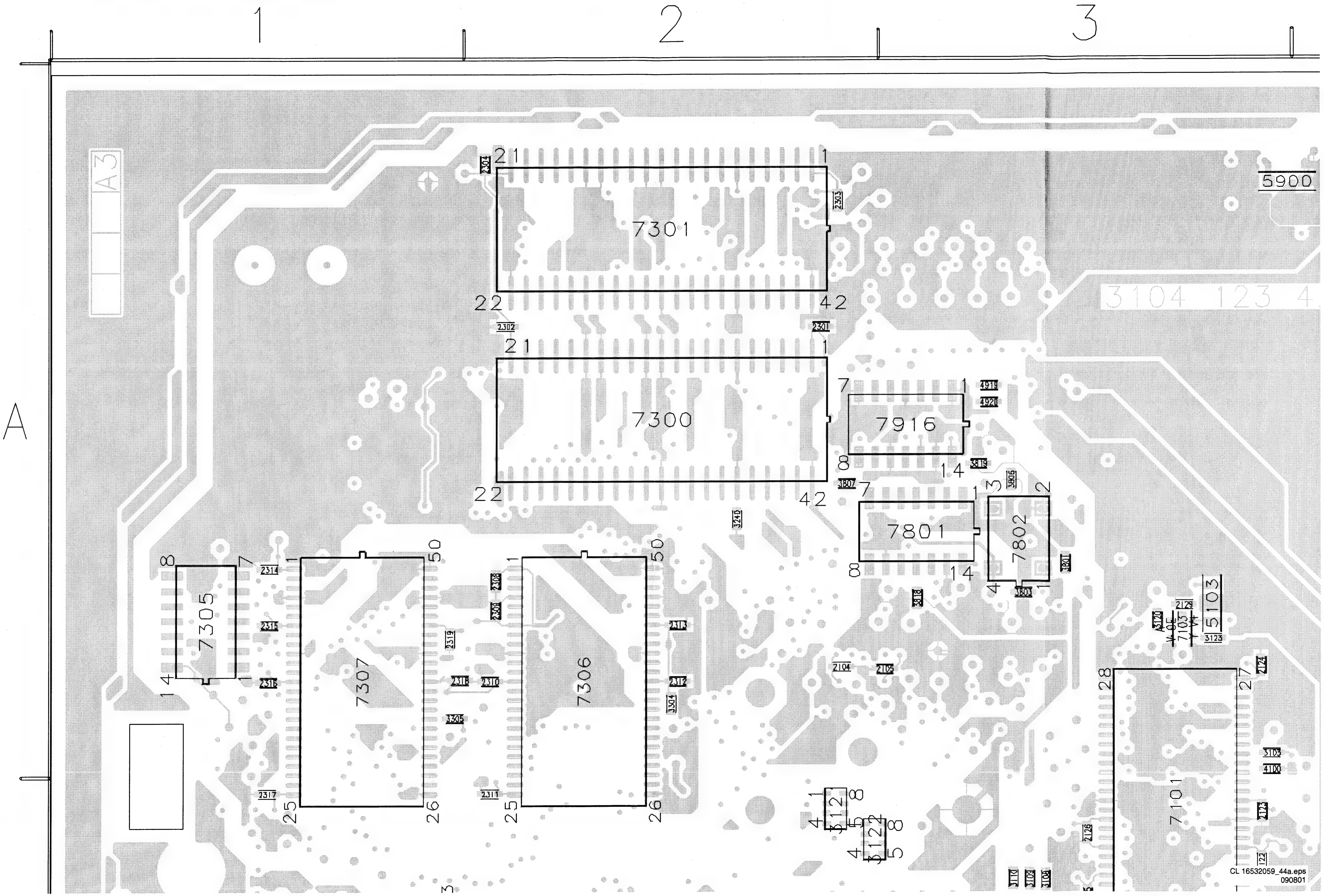
Layout Digital Board (Overview Bottom View)



2104	A2	2903	C2	4213	B1
2105	A3	2904	C2	4406	B4
2115	B3	2921	A4	4407	B4
2116	B3	2922	A4	4552	C5
2117	B3	2923	A4	4554	C5
2118	B3	2925	A4	4555	C5
2120	B3	3103	A3	4703	B4
2121	B3	3108	B3	4704	B4
2122	B3	3109	B3	4800	B2
2123	B3	3110	B3	4919	A3
2124	A3	3120	A3	4920	A3
2125	B3	3121	B2	4921	C2
2126	B3	3122	B2	5103	A3
2129	A3	3123	A3	5605	A5
2209	B1	3200	B1	5625	A5
2210	B1	3211	B2	5700	C2
2214	B1	3212	B1	5801	C2
2228	B1	3213	B1	5900	A3
2301	A2	3214	B1	5901	A4
2302	A2	3215	B1	7101	B3
2303	A2	3221	B2	7103	A3
2304	A2	3240	A2	7300	A2
2308	A2	3267	B1	7301	A2
2309	A2	3269	B1	7305	A1
2310	A2	3270	B1	7306	A2
2311	B2	3272	B1	7307	A1
2312	A2	3273	B1	7403	A4
2313	A2	3304	A2	7602	A5
2314	A1	3305	A1	7606	A5
2315	A1	3405	B4	7625	A5
2316	A1	3554	C5	7800	B3
2317	B1	3555	C4	7801	A3
2318	A1	3556	C5	7802	A3
2319	A1	3557	C5	7803	B2
2404	A4	3558	C5	7900	B2
2405	A4	3561	C5	7913	C2
2407	A4	3563	C4	7916	A3
2408	A4	3606	A5	7917	B2
2409	A4	3607	A5	7918	C2
2410	A4	3608	A5		
2411	A4	3616	A5		
2413	B4	3626	A5		
2414	B4	3627	A5		
2415	B4	3628	A5		
2420	A4	3649	A5		
2421	A4	3650	A5		
2422	A4	3651	A5		
2423	A4	3652	A5		
2424	A4	3653	A5		
2550	C5	3654	A5		
2551	C5	3655	A5		
2552	C5	3656	A5		
2553	C4	3657	A5		
2554	C4	3700	C2		
2555	C4	3702	C2		
2556	C4	3703	C2		
2557	C4	3704	C2		
2558	C4	3706	C2		
2559	C4	3713	C2		
2560	C4	3714	C2		
2561	C5	3715	C2		
2570	C4	3716	C2		
2571	C5	3717	C2		
2572	C5	3718	C2		
2573	C4	3719	C2		
2574	C5	3722	C2		
2575	C4	3724	C3		
2576	C4	3725	C3		
2577	C4	3800	B3		
2578	C3	3801	A3		
2579	C5	3802	B3		
2581	C5	3803	A3		
2582	C4	3806	A3		
2583	C5	3807	A2		
2584	C4	3815	B3		
2585	C4	3816	B3		
2586	C5	3817	B3		
2589	C5	3818	A3		
2590	C5	3819	A3		
2591	C4	3900	B2		
2592	C4	3901	B2		
2593	C5	3902	B2		
2595	C4	3903	B2		
2605	A5	3904	B2		
2606	A5	3905	B2		
2607	A5	3906	B2		
2625	A5	3907	B2		
2626	A5	3908	B2		
2627	A5	3911	B2		
2701	C2	3912	B2		
2713	C2	3913	C2		
2800	B3	3928	C2		
2809	A5	4100	A3		
2900	B2	4209	B2		
2901	B2	4210	B2		
2902	B2	4211	B2		

Layout Digital Board (Part 1 Bottom View)



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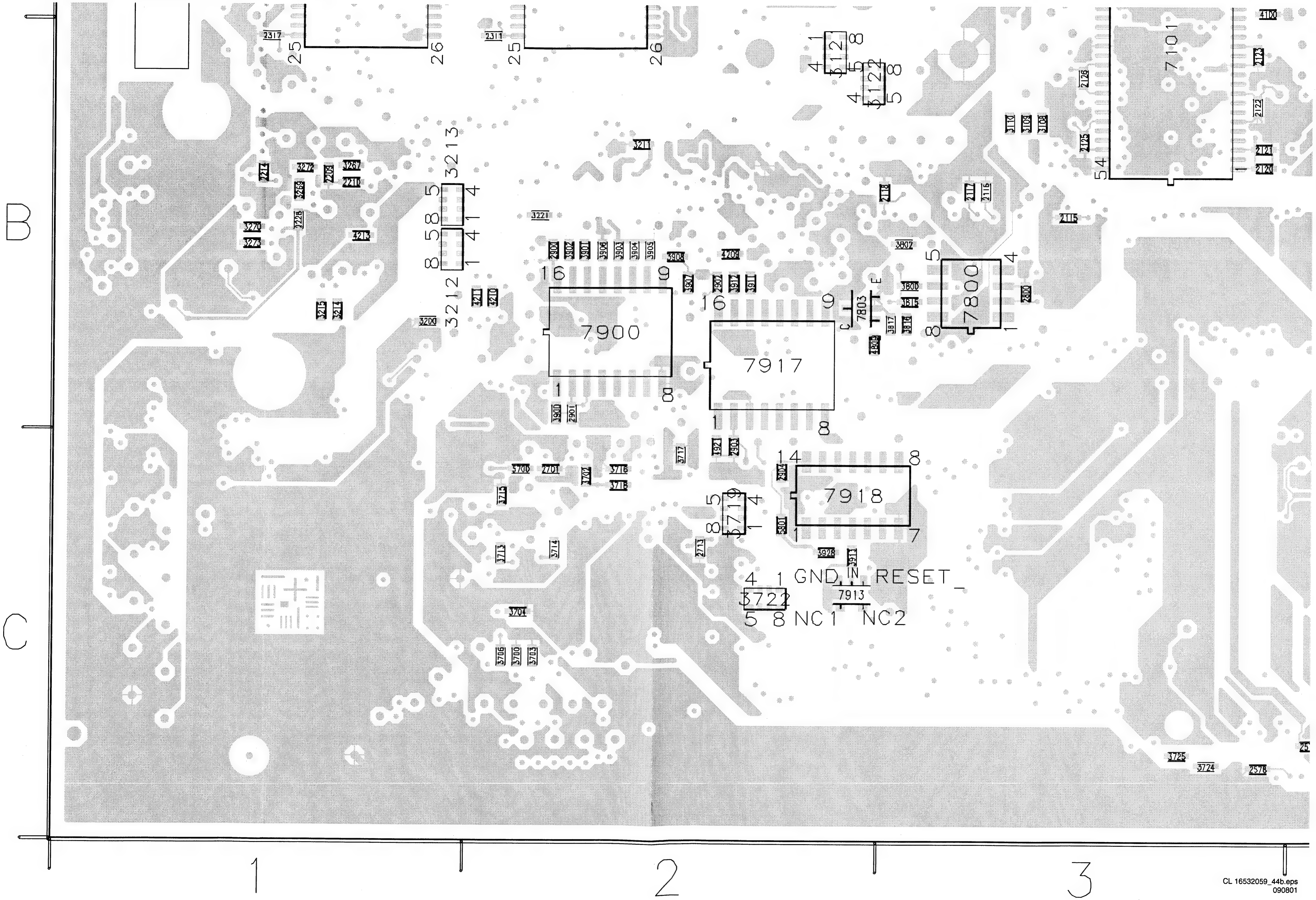
Layout Digital Board (Part 2 Bottom View)



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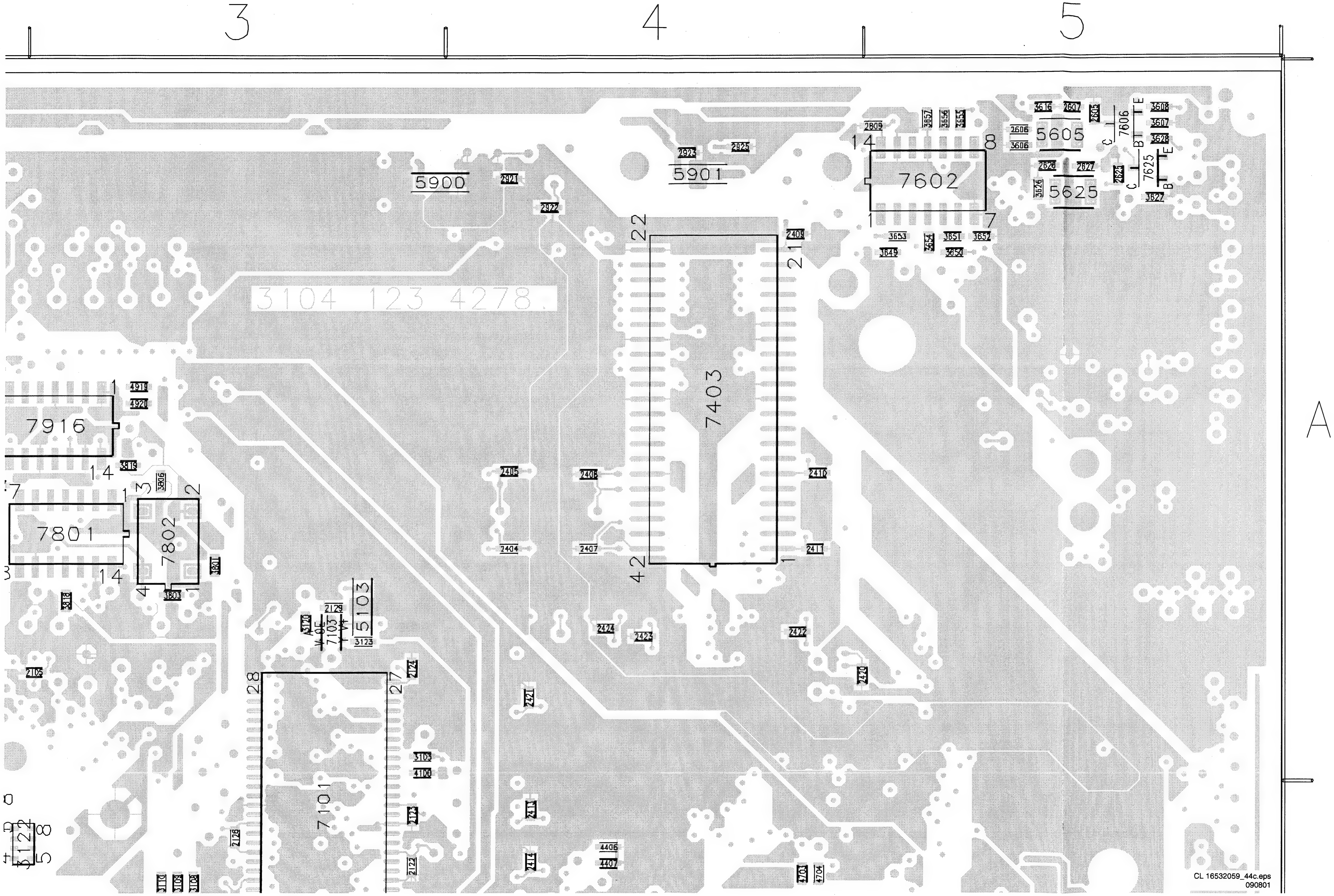
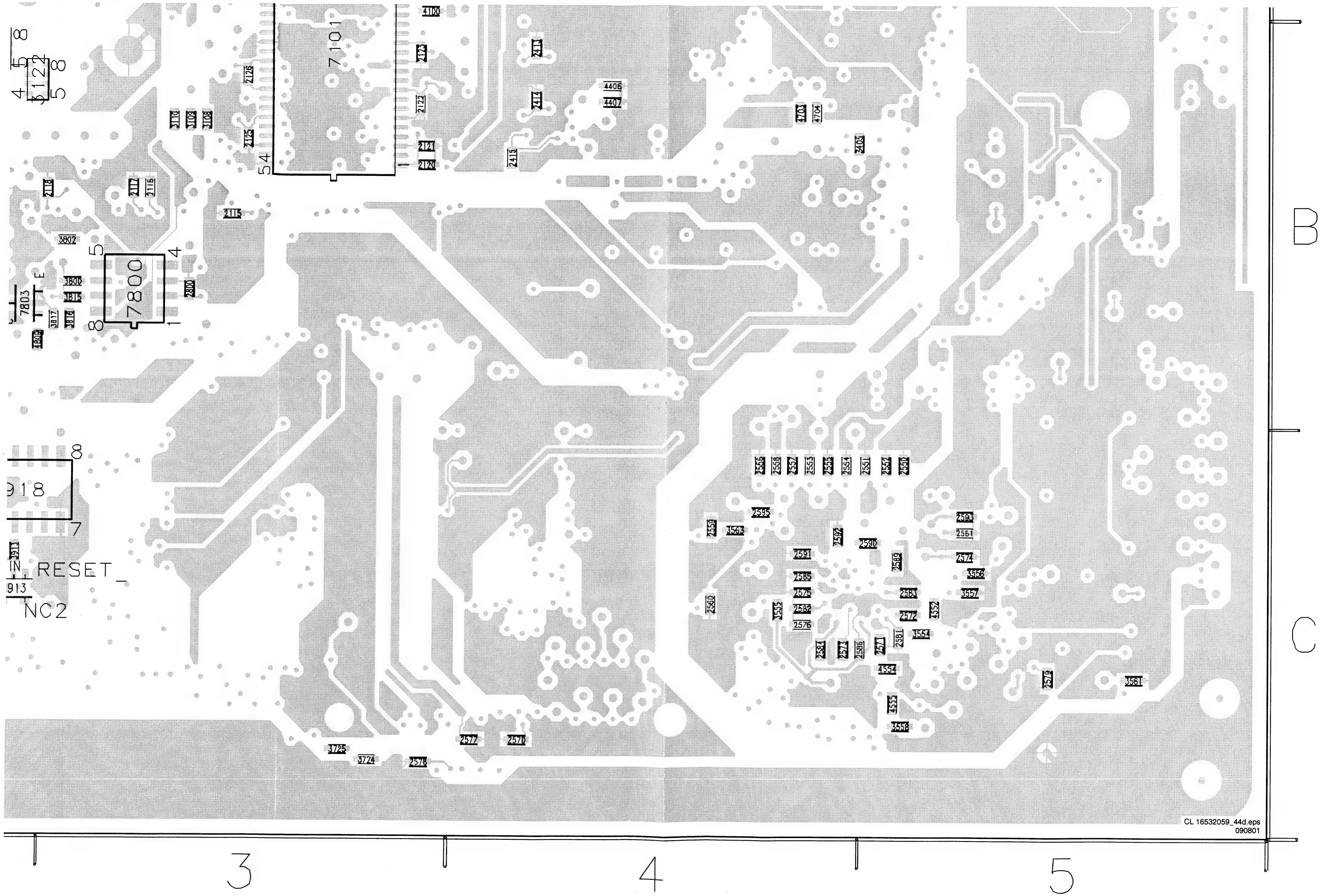
Layout Digital Board (Part 3 Bottom View)



Layout Digital Board (Part 4 Bottom View)



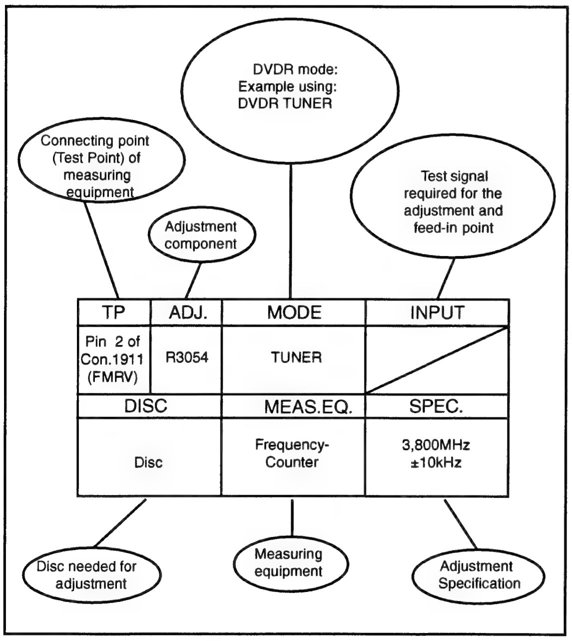
8. Alignments

ADJUSTMENT INSTRUCTIONS ANALOGUE BOARD

Test equipment:

1. Dual-trace oscilloscope
   Voltage range : 0.001 ~ 50 V/div
   Frequency : DC ~ 50 MHz
   Probe : 10:1, 1:1
2. DVM (Digital voltmeter)
3. Frequency counter
4. Sinus generator
   Sinus : 0 ~ 50 MHz
5. Test pattern generator

How to read the adjustment procedures:



Front End (FV)

Service tasks after replacement of IC 7703, coil L5702 and L5703:

1 AFC Adjustment:

Purpose: Correct adjustment of demodulator AFC - circuit

Symptom, if incorrectly set:
Bad or disturbed TV channel reception.

PAL - AFC adjustment [5703]:

TP	ADJ.	MODE	INPUT
IC 7703 Pin 17 (I976)	L5703	TUNER	38,9MHz 500mV$_{pp}$ at Tuner 1705, Pin 11 (F700, IF-out)
DISC		MEAS.EQ.	SPEC.
		DC Voltmeter Frequ. Generator	2,5V ±0,2V

2 HF - AGC adjustment [3707]:

Service tasks after replacement of IC 7703:

Purpose: Set amplifier control.

Symptom, if incorrectly set:
Picture jitter if input level is too low and picture distortion if input level is too high.

TP	ADJ.	MODE	INPUT
Tuner 1705 Pin 11 (F700, IF-out)	R3707	Set tuned to channel 27	4,5mV(74dBµV) on aerial input PAL white picture, audio IF on, no modulation
DISC		MEAS.EQ.	SPEC.
		Oscilloscope Video Pattern Generator	550mV$_{pp}$ +/-50mV (use a 10:1 probe)

3 Attenuating the 40.4 MHz [5702]: (SECAM only)

Service tasks after replacement of coil 5702:

Purpose: To attenuate the band I carrier rests.

Symptom, if incorrectly set:
Bad picture quality when the filter attenuates the picture carrier (38.9MHz).

TP	ADJ.	MODE	INPUT
OFW 1700 Pin 1 (F704)	L5702	TUNER	40.4 MHz, 300mV$_{rms}$ at Tuner 1705, Pin 11 (F700, IF-out)
DISC		MEAS.EQ.	SPEC.
		Oscilloscope, Sinus Generator, Counter	adjust minimum amplitude

If the adjustment is correct the signal at pin 1 of OFW [1700] must be smaller than the input signal amplitude by at least 5 dB.

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9. Circuit-, IC Descriptions and List of Abbreviations

9.1 Multi-Mode SOPS 50PS203

9.1.1 Why Multi-Mode SOPS?

Using ordinary SOPS results in a decrease of the efficiency at low output loads due to the increase of the switching frequency.
The Multi-Mode SOPS will reduce the switching frequency at low loads but still preserves valley switching.

9.1.2 Block Diagram

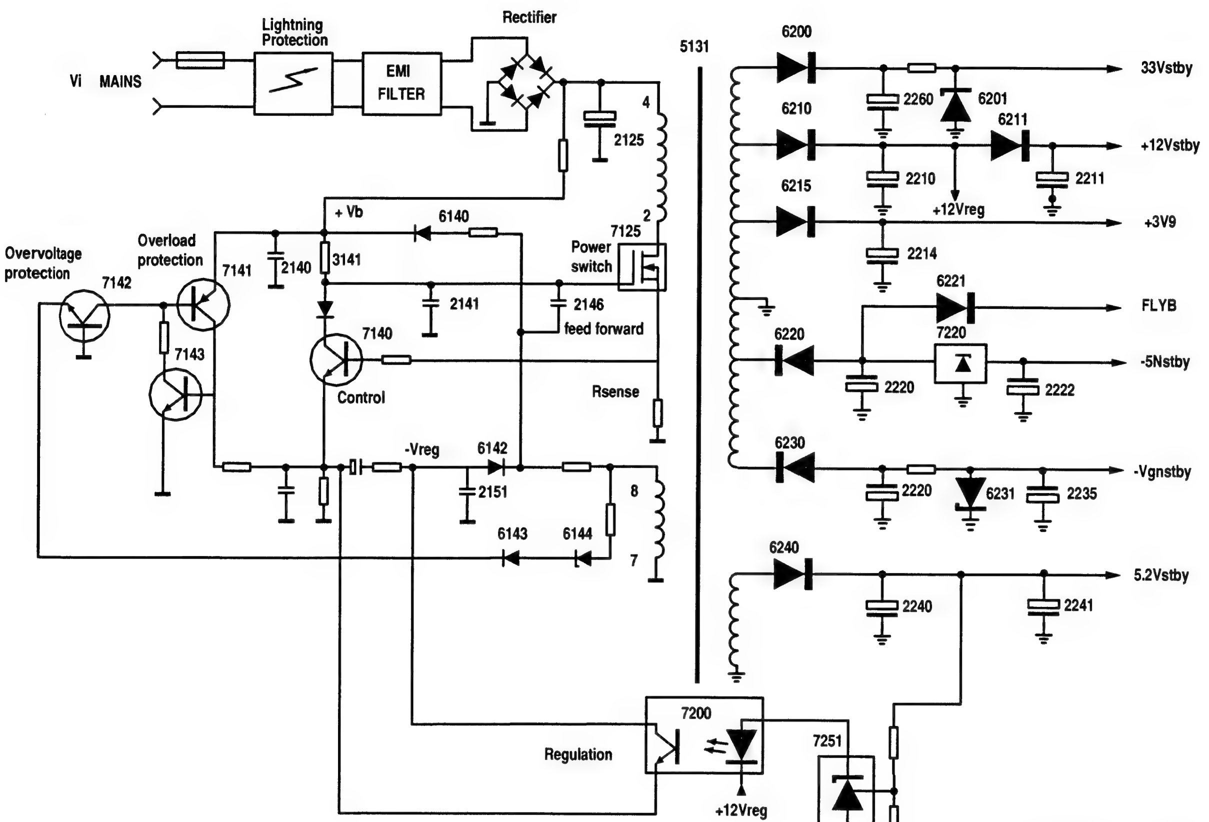

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Figure 9-1

9.1.3 Circuit Description

Input Circuit
The input circuit consists of a lightning protection circuit and an EMI filter.
The lightning protection comprises R3120, sparkgaps 1124 and 1125. D6128, 6129, C2127 and R3129 are optional. L5110, L5115, C2120 and L5120 form the EMI filter. It prevents inflow of noises into the mains.

Primary Rectifier/smoothing Circuit
The AC input is rectified by diodes 6151,6152, 6153, 6154 and smoothed into C2125. The voltage over C2125 is approximately 300V. It can vary from 200V to 390V.

Start Circuit
This circuit is formed by R3125, 3126, R3141, C2140 and R3132.

When the power plug is connected to the mains voltage, the MOSFET 7125 will start conducting as soon as the gate voltage reaches a treshold value. A current starts to flow in primary winding 2-4. The MOSFET will be fed forward via winding 7-8, R3150 and C2146.

+Vb Supply and Negative Regulation Voltage
The positive part of the voltage over winding 7-8 will be rectified via R3150, D6140 and charged via R3140 into C2140. The voltage over C2140 has a value of +30 till +40V. This value depends on the value of the mains voltage Vi and the load.
The negative part of the voltage over winding 7-8 will be rectified via R3150, D6142 and charged into C2151. The voltage over C2151 has a value of -15V and is used as regulation voltage.

Control Circuit
The control circuit exists of T7140, D6141, C2144 and 2145, C2147, R3147 and 3148.

This circuit is fed by supply voltage +Vb via R 3141. This circuit controls the conduction time and the switching frequency of the power switch circuit. It switches off the MOSFET as soon as the voltage over Rsense reaches a certain value. This value depends on the error voltage at the emittor of T7140, which can be positive or negative (+/- 0,66V). The voltage fed back by the regulation circuit defines this error voltage.

Power Switch Circuit

This circuit comprises MOSFET 7125, Rsense formed by R3133, 3134, 3135, 3136 and 3137, R3131, R3132, D6146. Diodes 6130, 6131 and 6132 protect the control circuit in case of failure of the MOSFET.

Regulation Circuit

The regulation circuit comprises opto-coupler 7200, which isolates the base voltage of transistor 7140 at the primary side from a reference component 7251 at the secondary side. The TL431(7251) can be represented by two components:

- a very stable and accurate reference diode
- a high gain amplifier

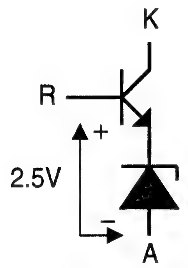

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Figure 9-2

TL431 will conduct from cathode to anode when the reference is higher than the internal reference voltage of about 2.5V. If the reference voltage is lower, the cathode current is almost zero.
The cathode current flows through the LED of the opto-coupler. The collector current of the opto-coupler will adjust the feedback level of the error voltage at the emittor of T7140.

Overload Protection Circuit

This circuit consists of R3145, C2143, a thyristor circuit formed by T7141 and T7143, R3143 and R3142. When the output is shortened, the thyristor circuit will start to conduct and switch off the supply voltage over C2140. This results in a switching of f of the drain current of the MOSFET 7125 and the output will be disabled. The start circuit will try to start up the power supply again. If the circuit is still shortened, the complete start and stop sequence will repeat. The power supply comes in a hiccup mode (is ticking).

Overvoltage Protection Circuit

This circuit consists of R3149, D6144, 6143, R3144, C2142 and T7142.
When the regulation circuit is interrupted due to an error in the control loop, the regulated output voltage will increase (overvoltage). This overvoltage is sensed on the primary winding 7-8.
When an overvoltage is detected, the circuit will start up the thyristor circuit T7141-7143. The power supply will come in a hiccup mode as long as the error in the control loop is present.

Secondary Rectifier/Smoothing Circuit

There are 6 rectifier/smoothing circuits on the secondary side. Each voltage depends on the number of windings of the transformer.
From these circuits a lot of voltages are derived and fed to 3 connectors. The following voltages are present at the output:
Connector 209
Functional use: to Digital board + Dvio board

1. +3V3(for dig pcb + DVio)
2. +3V3(for dig pcb + DVio)
3. +3V3(for dig pcb + DVio)
4. +3V3(for dig pcb + DVio)
5. GND(for dig pcb + DVio)
6. +12V(for dig pcb + DVio)
7. GND(for dig pcb + DVio)
8. GND(for dig pcb + DVio)
9. +5V(for dig pcb + DVio)
10. STBY control(for dig pcb + DVio)
11. GND(for dig pcb + DVio)
12. -5V(for dig pcb + DVio)

The +12V is switched off by the STBY_ctrl signal.
When the +12V is switched off, also the +3V3, +5V and -5V are switched off. All these voltages are low drop regulated.
Connector 0205
Functional use: to analogue board + display board + flap motor
'STBY' indicates that the voltage will not be switched off in the standby situation.

1. +12VSTBY(= +12V Standby, for display heating, 8Vstby)
2. +5VSTBY(= +5V Standby; general use)
3. -5NSTBY(= -5V Standby; neg. voltage for drivers)
4. VGNSTBY(= -32V Standby; for display grids)
5. +33STBY(= +33V Standby; for tuner)
6. FLYB(flyback pulse for power fail + measurement)
7. GNDA(Ground for the analogue board)

Connector 0207
Functional use: to engine

1. +3V3(for engine servo board)
2. +5V(for engine servo board)
3. GND(for engine servo board)
4. +4V6E(for engine analog part)
5. GND(for engine servo board)
6. -5V(for engine servo board)
7. GND(for engine motor currents)
8. +12V(for engine motor currents)

9.2 Display Board

9.2.1 Operation Unit DC (DC Part)

The core element of the operation unit DC is the microcontroller TMP88CU77ZF [7156]. The TMP88CU77ZF is an 8 bit microcontroller fitted with 96kB ROM and 3kB RAM and is responsible for following functions:

- Integrated VFD driver
- Timer
- Evaluation of the keyboard matrix
- Decoding the remote control commands from the infra-red receiver pos. 6170
- Activation of the display
- Motor driver

The system clock is generated with the 12MHz quartz (Pos. 1153).

9.2.2 Evaluation of the Keyboard Matrix

There are 15 different keys on the display board. A resistor network is used to generate a specific direct voltage value, depending on the key pressed, via the resistors 3145, 3171, 3183 and 3194 on the analog/digital (A/D) ports (7156 Pin 17, 18, 19, 20). Pressing keys simultaneously may lead to undesired functions!

9.2.3 IR Receiver and Signal Evaluation

The IR receiver [7140] contains a selectively controlled amplifier as well as a photo-diode. The photo-diode changes the received transmission (approx. 940nm) in electrical pulses, which are then amplified and demodulated. On the output of the IR receiver [7140], a pulse sequence with TTL-level, which corresponds to the envelope curve of the received IR remote control command, can be measured. This pulse sequence is input into the controller for further signal evaluation via input IRR [7156, pin 2].

9.2.4 Motor Driver Flap

The flap-motor is controlled via the 2 Port-Pins (MD1, MD2) of the P (7156, Pin 12, Pin 100). The motor driver part is constructed as a bridged dual power operational amplifier. Between the IC outputs (7120, Pin1, Pin3) and a Boucherot circuit (2121, 3126) suppresses a spurious 3MHz oscillation from the output stage. The two ports-pins (MD1, MD2) of the P are PWM-outputs and are controlled in the following way:

Flap Motor:

	MD1	MD2
off	H	L
open	H	PWM(H)
close	L	PWM(L)

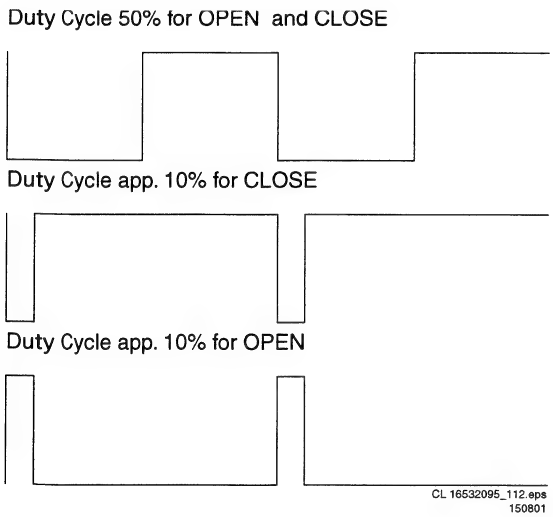

Figure 9-3

For the detection of the end-positions of the flap there are two switches (1178, 1179) installed and the information is evaluated from the P via the signals SW_1178 and SW_1179.

Flap Switches:

	SW1	SW2
open	L	H
closed	H	L
moving	H	H
error	L	L

9.2.5 Bi-Color LED (Standby and ON)

The STBY-LED is a red/green bi-color-LED and is controlled via the STBYLED-signal of the P (7156 Pin 10) in the following way:

Colour of STBY LED	Status of the Set
red	STBY
green	ON

9.3 Analogue Board Europe

9.3.1 Microprocessor TMP93C071F

The microcontroller „AIO“ TMP93C071F is a 16bit microcontroller with internal ROM and 8kB RAM. It includes the following functions:

- A/D converters
- composite sync input
- I^2C bus interface

Following connection to the mains, a positive pulse on the reset input on the P is generated by the reset-IC TL7705 (Pos.7900). The system clock is generated with the 20MHz quartz (Pos. 1994).

9.3.2 Bus Systems

The communication between the P and the other functional groups is via the I^2C-bus (SDA, SCL). The clock rate is approx. 95kHz.
Functional groups on the I^2C bus:

- E^2PROM ST24E16 (Pos. 7815)
- Tuner (Pos. 1705)
- Matrix-switch STV6410 (Pos. 7507)
- Audio IC / MSP (Pos. 7600)
- Display board (Pos. 1987)
- VPS-IC (Pos. 7990).

9.3.3 E^2PROM

The E^2PROM ST24E16 (Pos. 7815) is an electric erasable and programmable, non-volatile memory. The E^2PROM stores data specific to the device, such as the AFC-reference value, clock-correction-factor, etc. The data is accessed by the P via the I^2C-bus.

9.3.4 VPS, PDC, Teletext (Europe Only)

The STV5348 (Pos. 7990) is a VPS, PDC, and Teletext Decoder with an external 13,875Mhz quartz.
The following data formats are identified:

- VPS (Timer data and station name)
- PDC Format 2 (Timer data and station name)
- PDC Format 1 (station name and time)
- TXT header line (time for „time download“)

9.3.5 FOME

The FOME-circuit compares the video signal coming from the tuner and the one coming from the Scart-plug 1. If the video-signals are identical the output of the FOME-circuit is low.

9.3.6 Fan Control

The fan control circuit is necessary to control the speed of the cabinet fan (Pos. 1984) according to the requirements in temperature and noise. The temperature is measured via an NTC on the display board (Pos. 3145). When the temperature is lower than 25°C the fan-voltage is approx. 5V

and will reach approx. 10V at a temperature of 40°C. It is also possible to switch off the fan via the control line ION_FAN. The circuit generates also two control-signals: TEMP goes to the P and BE_FAN is the control-line for the basic engine fan.

9.3.7 Power Supply

The 5SW and 8SW supply are switched off in case of standby from the P via the ISTBY-line. This is possible for power-save. The ISTBY-line must be low in case of STBY. There is also a „power fail“ circuit on the PS-schematic which is necessary to mute AUDIO when IPFAIL is low.

9.3.8 Front End (TU, AP Part)

The Front End Comprises the Following Parts:

- Tuner [1705]
- IF amplifier & video demodulator IC TDA 9818 [7703]
- Sound processor MSP3415G [7600]

IF Selection

The IF frequency of the video carrier is 38.9 MHz for all systems except SECAM L' (33.9 MHz).
A quasi-split audio system is used. Separate surface-wave filters (SAW) are required. [1700], [1701] for video, [1702] for audio. [1700] Is switched into the signal path for DK/I-SECAM L/L' reception, if the signal SAWS is “high”. In this case the switches [7701], [7702] are open and the diode [6700] is conducting. [1701] Is switched into the signal path for BG reception, if the signal SAWS is “low”. Then the switch [7708] is open and the diode [6701] is conducting. For DK/I-SECAM L/L' reception, an additional circuit for suppressing the adjacent channel audio carrier is provided, which is set using coil [5702] to maximum suppression at 40.4MHz.

IF Demodulator

TDA 9818

The IF signal from the tuner is processed by the demodulator IC TDA 9818 [7703]. The signal PSS to pin3 switches between demodulation of positive SECAM or negative PAL modulated video carriers. A QSS-audio-IF signal SIF1 is generated for demodulation in the sound processor [7600]. The audio-IF carrier is selected in the audio SAW filter [1702]. This filter is switched for SECAM L’. If the signal SB1 is “high”, the switch [7707] is closed and the diode [6702] is not conducting. For all other standards the diode [6702] is conducting and the switch [7707] is open. The output signal from this SAW filter is first processed in the TDA 9818. Audio carriers are converted from the tuner IF level into the audio IF position and further processed in the audio demodulator [7600]. The AFC coil [5703] on the TDA 9818 is adjusted so that when a frequency of 38.90 MHz is supplied to the IF output of the tuner, the AFC voltage on pin 17 of the TDA 9818 is 2.5V. The setting of the picture carrier frequency for SECAM L in the TDA 9818 is achieved by connecting pin 7 of the IC via a resistor [3702] to earth. The switch [7700] and the signal SB1 "high" do this. The HF-AGC is set using the AGC controller [3707] so that, with a sufficiently large antenna input signal (74 dBV), the voltage at the IF output of the tuner [1705] pin 11 is 500 mVpp. This setting must be carried out, when the audio carrier is switched off. The demodulated video signal appears on pin 16 [7703]. The demodulator AGC voltage at pin4 is used to determine the antenna signal strength after a buffer [7705] with the signal AGC_MUTE. In the opposite direction this line may be used to mute the demodulator to avoid cross talk in all cases, where the tuner signal is not needed. In this case a „high“ signal is sent via AGC_MUTE and the conducting diode [6703] to pin4. The video trap [1703] reduces adjacent channel video and sound carrier remainders in the video for BG standards. For all other standards the switch [7704] and signal TS "low" bypass this trap. In this cases the selectivity of the SAW filter [1700] is sufficient. A frequency response correction is achieved by the inductance [5009] for not BG standards. This correction is not preferred for SECAM L' and therefore shorts circuited by [7709], if the signal SB1 is “high”. The demodulated video signal VFV is available after the buffer and limiting stage for noise peaks [7706]. The FM-PLL demodulator function of TDA 9818 is not used and deactivated by the resistor [3726].

Audio Demodulator

Sound processor MSP 3415G

The MSP 3415G [7600] is a multistandard sound processor which can demodulate FM Mono/Stereo, NICAM and AM signals. The incoming signal is first controlled and then digitised. The digital signal is then demodulated in 2 separate channels. In the first MSP channel, FM and NICAM (B/G/I/D/K) are demodulated, whereas in the second MSP channel, FM and are demodulated again (NICAM L corresponds to NICAM B/G). These demodulated signals are selected digitally in the I/O and switched to the D/A converter on the outputs. Amplitude and bandwidth of the demodulated audio signals can be determined in the MSP using the corresponding commands via the I2C bus. The audio signal from the tuner is available at the pins 30 AFER and 31 AFEL.

9.3.9 Input/Output Video-Routing (Europe-Version)

General Description:

The complete Video- I/O-switching is basically realised by the I/O switch STV6410A. It is controlled via IIC-Bus-0 (SDA/SCL) by the all in one C on the analogue board. The STV 6410 has three YCVBS switches, three chroma switches and one RGB switch. All switches have 6-dB amplification on the outputs. The YCVBS inputs have bottom clamp, the chroma inputs have average clamp, and the RGB inputs have bottom clamp circuits at the inputs. The R/C inputs can be switched to average clamp for chroma signals via I2C bus.
The IC has also one slow blanking monitor and one fast blanking switch for fast RGB insertion (see detailed description in chapter 1.5). Two pre-selectors BA 7652 are additionally used: One for switching between Rear CVBS, Y-Rear and Front, the second for switching between Chroma-Rear and Front signal. Both pre-selectors are controlled via IS1 and IS2 from the analogue board C.

CVBS Signals:

There are four CVBS input connection possibilities: Front chinch (E6), Rear Chinch (E4), Scart 1 (E1) and Scart 2 (E2). Rear Chinch In is routed via the pre selector BA 7652; the other signals are connected direct to the STV 6410. The selected CVBS signal is routed to Rear Chinch Out (via BA 7660, 6dB amplification, 75 Ohm driver) and to Scart 1. Independent of the input signal quality (CVBS, S-Video or RGB) the digital board supplies also S-Video and RGB signals to the corresponding socket.

S-Video Signals:

There are also four S-Video input connection possibilities: Front In (E5), Rear In (E3), Scart 1 and Scart 2. For S-Video from Scart this option has to be switched on in the OSD menu. The pre-selectors and the STV 6410 do the signal selection (for detailed routing see overview). Also the video quality will be S-Video, the digital board supplies also CVBS to the corresponding sockets. The S-Video signal that is coming from the digital board is routed via BA 7660 (6-dB amplification and 75-Ohm driver) to the S-Video Rear Out socket.

RGB Signals:

The Scart 2 RGB input signal (Decoder socket) is connected to the RGB switch of STV 6410 and to the digital board in parallel. The RGB from Scart 2 is routed to Scart 1 in low

power standby mode. The direct connection (not via STV 6410) is for loop through and REC. The RGB signal, which is coming from the digital board, is connected to the RGB encoder input of the STV 6410 and is routed to Scart 1 in all other modes.
As the Scart-connection can carry either RGB- or Y/C-signals it is necessary to define the available and selected signal-property. While Pin15 of Scart (Red or Chroma-upstream) is fully handled via STV6410A the Pin7 (Blue or Chroma-downstream) has to be extra set.

- Scart1: Pin42 of C (SC1YC_H-line):
  - Low (Blue-Out on SC1
  - High (Chroma-In on SC1
- Scart2: Pin41 of C (SC2RGB_H-line):
  - Low (Chroma-Out on SC2
  - High (Blue-In on SC2

Detection of Status-Information

Pin-8 (Slow-Blank):
Level-detection of Pin-8 (Scart-1 and -2) is realised by using STV6410A. It can be readout via IIC-Bus by the CC-C. To obtain the status of Scart1-Pin8, Bit 0 & 1 of register 06h must be set to 0 (Input-mode). The corresponding bits for verification of Scart2-Pin8-status are set to input-mode as default.
Meaning of Read-Register-Bits:

- Bit 7 & 6: not used
- Bit 5 & 4: Status Scart-2/Pin8:
  - 0 1 Low-level
  - 1 0 Medium-level (16:9)
  - 1 1 High-level (4:3)
- Bit 3 &2: not used
- Bit 1 & 0: Status Scart-1/Pin8:
  - 0 1 Low-level
  - 1 0 Medium-level (16:9)
  - 1 1 High-level (4:3)

Pin-16 (Fast Blank):
Only the status/level of Scart-2/Pin16 must be detected; this is realised by using PortC3/AIN14 (Pin25) of the CC-C as an Analogue-input.

- ADC-value lower or equal 24h (Pin16 low (no RGB-signals)
- ADC-value greater 24h (Pin16 high (RGB present on Scart-2)

To avoid misdetection a "software-integration" (result is first valid if it was 3-times the same) must be implemented, determination has to be done approx. every 47msec (no multiple of V-sync).

WSS on Y/C-Plug:
Picture-Ratio-Information (16:9 or 4:3) on SVHS-connections is coded via the average DC-level of the Chroma-signal-line, detection is realised by using an analogue-input-port of the CC-C.

- ADC- value lower or equal 40h (4:3-picture-ratio delivered
- ADC-value greater 40h (16:9-picture-ratio available on plug

Y/C-Rear is determined via Port40/AIN3 (Pin14) of CC (WSRI-line) and Port41/AIN4 (Pin15) is used for Y/C-Front (WSFI-line).

Generation of Status-Information

Pin-8 (Slow Blank):
Only on Scart-1 the Slow-Blank-Status (Level of Pin8) must be created, which is done via IIC-Bus-register 06h (Bits 0 & 1) of the STV6410A.

Pin-16 (Fast Blank):
Only the status/level of Pin16-Scart1 must be controlled; this is realised by using the FB-switch-capabilities of the STV6410A, which are set via IIC-Bus-register 04h (bits 4 & 5).

WSS on Y/C-Plug:
The appropriate DC-level on Chroma-signal-line for Y/C-Rear-Out is produced via Port57 (Pin10) of the CC-C (WSRO-line).

- 4:3 - Picture-ratio supported on Y/C-Plug: Port57 set to 0
- 16:9 - Picture-ratio supported on Y/C-Plug: Port57 set to 1

9.3.10 Audio Routing Analogue board (Europe / Nafta)

General Description:
The Audio- I/O switching is realised by the STV6410 I/O switch.
By I^2C Bus (SDA-0/SCL-0) it is possible to control all the Audio in- and outputs (for detailed Information we refer to the STV6410 routing overview).
Analog audio coming from DV-Board and second rear Cinch input is routed via MSP3415 to the STV 6410. After selecting the audio source via STV 6410, the signal must be transformed into the digital domain. For this, the UDA 1360TS (ADC) is responsible. An input-voltage of up to 2Vrms can be handled from the IC´s. For further processing, the UDA 1360TS (ADC) delivers the data-in I^2S format to the digital-board. After a certain delay the (processed) data come back from the digital board to the UDA 1328 (DAC). The UDA 1328 (DAC) transforms the I^2S data back into the analog domain and feeds the signals direct to the MC33078 (OPV). From the MC33078 (OPV) the signals are delivered back to the STV 6410 and also direct to the 2nd rear out Cinch. The other outputs (Scart, Cinch) are supported by the STV 6410.

Detailed Description STV 6410:
The STV 6410 is an I^2C bus controlled audio and video switch matrix, which is able to handle audio input signals up to 2 Vrms. The used outputs are equipped with internal level adjustment possibility. Low distortion and very good channel separation is a typical peculiarity of this IC. The output resistance is very low and the frequency bandwidth is up to 50 kHz.

Detailed Description UDA 1360:
The UDA 1360TS is a stereo Analog-to-Digital Converter employing bitstream conversion techniques.
The UDA supports the I^2S-bus data format and the MSB-justified data format with word lengths of up to 20 bits. The IC supports also 2Vrms input signals and is designed for 3V3 supply voltage.
The device is able to handle system clocks of 256fs and 384fs.
Typical THD+N at 0dB is -85dB and a S/N performance up to 97dB is possible.

Detailed Description UDA 1328:
The UDA1328 is a 6 channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.
The UDA 1328 supports the I^2S-bus data format with word lengths of up to 24 bits.
Digital sound features can be controlled with the L3 interface.
System clock can be set to 256fs or 384fs.
The Device also provides 2 high quality differential outputs.
Typical THD+N at 0dB is -95dB and a S/N of up to 106dB is possible.
Supply voltage is 3V3.

Detailed Description MC 33078:
The MC33078 is a dual operational amplifier for audio applications.
It offers low voltage noise (4,5nV/√Hz) and high frequency performances (15MHz Gain Bandwidth product, 7V/s slew rate).
In addition the MC33078 has a very low distortion (0,002%).

BLOCK DIAGRAM VIDEO IN/OUT EUROPE-VERSION

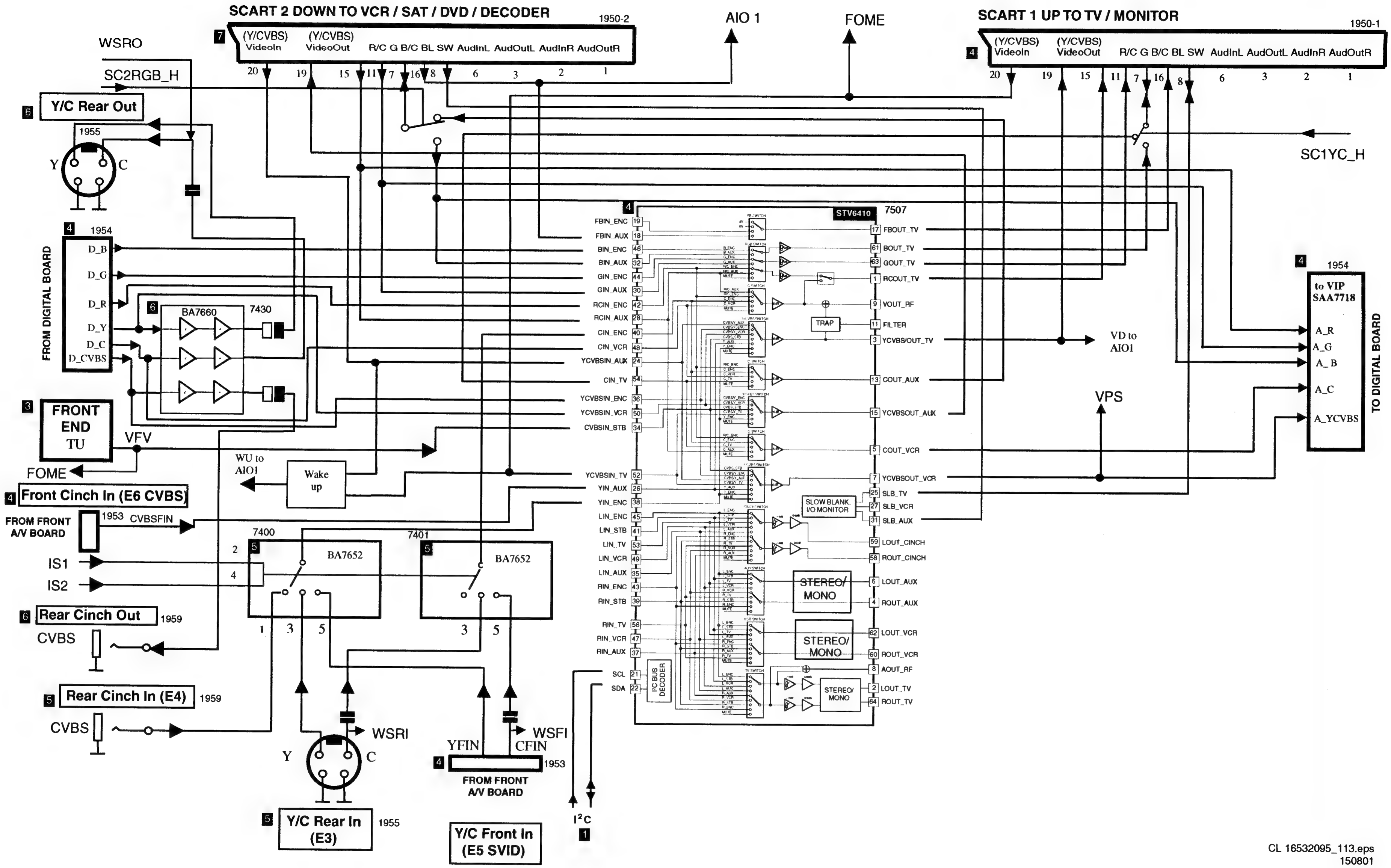

Figure 9-4

BLOCK DIAGRAM AUDIO IN/OUT EUROPE-VERSION

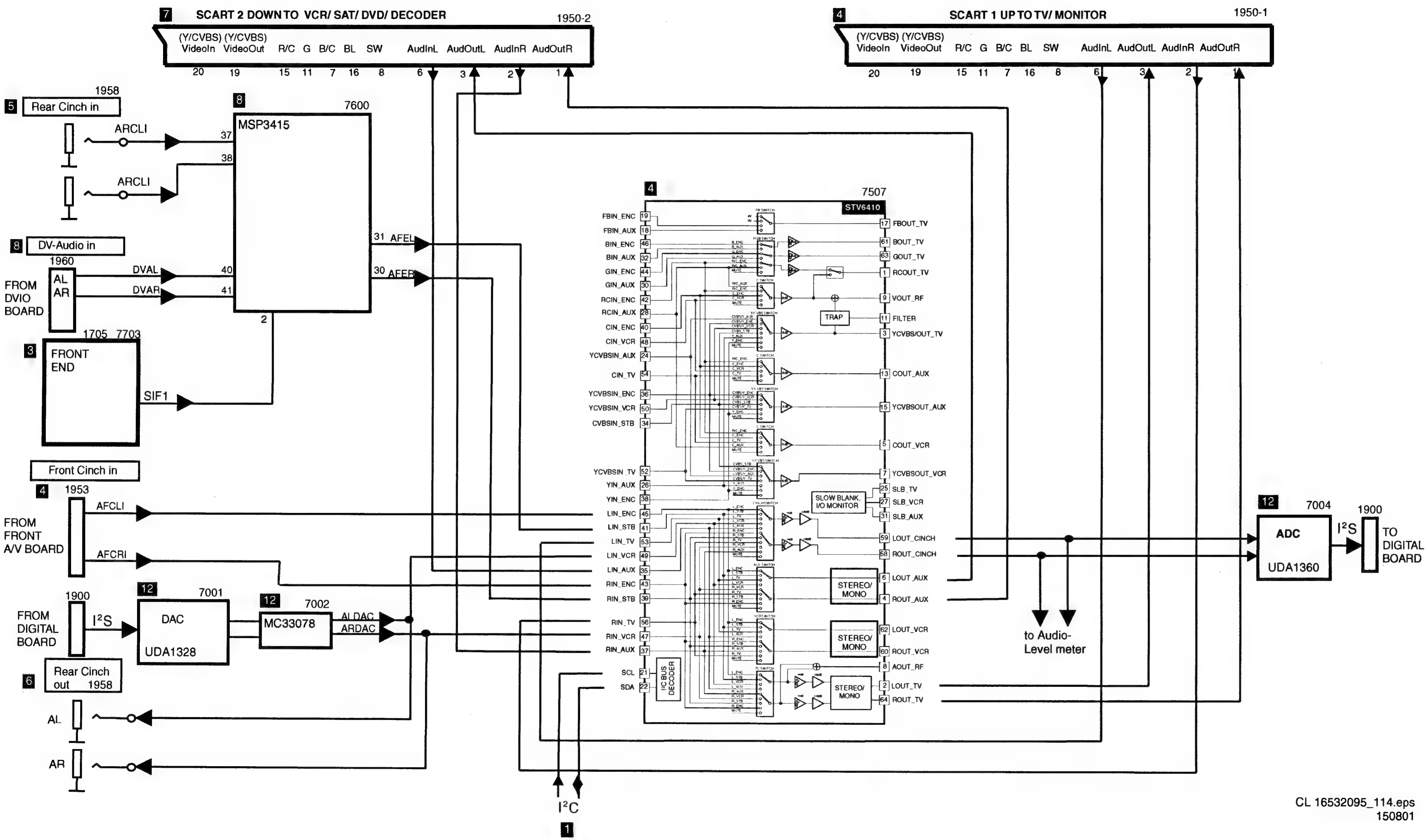

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Figure 9-5

9.4 Analog Board Nafta version

9.4.1 Microprocessor TMP93C071F

The microcontroller „AIO“ TMP93C071F is a 16bit microcontroller with internal ROM and 8kB RAM. It includes the following functions:

- A/D converters
- composite sync input
- I^2C bus interface

The following connection to the mains, a positive pulse on the reset input on the P is generated by the reset-IC TL7705 (Pos.7900).
The system clock is generated with the 20MHz quartz (Pos. 1994).

9.4.2 Bus Systems

The communication between the P and the other functional groups is via the I^2C-bus (SDA, SCL). The clock rate is approx. 95kHz.
Functional groups on the I^2C bus:

- E^2PROM ST24E16 (Pos. 7815)
- Tuner (Pos. 1705)
- Matrix-switch STV6410 (Pos. 7507)
- Audio IC / MSP (Pos. 7600)
- Display board (Pos. 1987)

9.4.3 E^2PROM

The E^2PROM ST24E16 (Pos. 7815) is an electric erasable and writeable, non-volatile memory. The E^2PROM stores data specific to the device, such as the AFC-reference value, clock-correction-factor, etc. The data is accessed by the P via the I^2C-bus.

9.4.4 FOME

The FOME (Follow Me) -circuit compares the video signal coming from the tuner and the one coming from the Scart-plug 1. If the video-signals are identical the output of the FOME-circuit is low.

9.4.5 Fan Control

The fan control circuit is necessary to control the speed of the cabinet fan (Pos. 1984) according to the requirements in temperature and noise. The temperature is measured via an NTC on the display board (Pos. 3145). When the temperature is lower than 25°C the fan-voltage is approx. 5V and will reach approx. 10V at a temperature of 40°C. It is also possible to switch off the fan via the control line ION_FAN. The circuit generates also two control-signals: TEMP goes to the P and BE_FAN is the control-line for the basic engine fan.

9.4.6 Power Supply

The 5SW and 8SW supply are switched off in case of Stby from the P via the ISTBY-line. This is possible for power-save. The ISTBY-line must be low in case of STBY. There is also a „power fail“ circuit on the PS-schematic which is necessary to mute AUDIO when IPFAIL is low.

9.4.7 Front End (TU, AP Part)

The front end comprises the following parts:

- Tuner [1705]
- IF amplifier & video demodulator IC TDA 9817 [7703]
- Sound processor MSP3445G [7600]

IF Selection

The IF frequency of the video carrier is 45.75 MHz. A quasi-split audio system is used. Separate surface-wave filters (SAW) are required. [1701] for video, [1702] for audio.

IF Demodulator

TDA 9817

The IF signal from the tuner is processed by the demodulator IC TDA 9817 [7703]. A QSS-audio-IF signal SIF1 is generated for demodulation in the sound processor [7600]. Audio carriers are converted from the tuner IF level into the audio IF position and further processed in the audio demodulator [7600]. The AFC coil [5703] on the TDA 9817 is adjusted so that when a frequency of 45.75 MHz is supplied to the IF output of the tuner, the AFC voltage on pin 17 of the TDA 9817 is 2.5V. The HF-AGC is set using the AGC controller [3707] so that, with a sufficiently large antenna input signal (74 dBV) the voltage at the IF output of the tuner [1705] pin 11 is 500 mVpp. This setting must be carried out, when the audio carrier is switched off. The demodulated video signal appears on pin 16 [7703]. The demodulator AGC voltage at pin4 is used to determine the antenna signal strength after a buffer [7705] with the signal AGC_MUTE. In the opposite direction this line may be used to mute the demodulator to avoid crosstalk in all cases, where the tuner signal is not needed. In this case a „high“ signal is sent via AGC_MUTE and the conducting diode [6703] to pin4. The video trap [1703] reduces adjacent channel video and sound carrier remainders in the video. The demodulated video signal VFV is available after the buffer and limiter stage for noise peaks [7706]. The FM-PLL demodulator function of TDA 9817 is not used and deactivated by the resistor [3726].

Audio Demodulator

Sound processor MSP 3445G

The MSP 3445G [7600] is a NTSC sound processor. Amplitude and bandwidth of the demodulated audio signals can be determined in the MSP using the corresponding commands via the I2C bus. The audio signal from the tuner is available at the pins 30 AFER and 31 AFEL.

9.4.8 Video-Routing (Nafta Version)

General Description:

The complete Video- I/O-switching is basically realised by the I/O switch STV6410A, which is controlled via IIC-Bus-0 (SDA/SCL) by the all in one C on the analogue board. The STV 6410 has three YCVBS, three chroma, and one RGB switch which is not used in the Nafta I/O. All switches have 6-dB amplification on the outputs. The YCVBS inputs have bottom clamp, the chroma inputs have average clamp, and the RGB switch has bottom clamp circuits at the inputs. The R/C inputs can be switched to average clamp for chroma signals via I2C bus.
Two pre-selectors BA 7652 are additionally used: One for switching between Y- Rear and Front, the second for switching between Chroma- Rear and Front signal. Both pre-selectors are controlled via IS1 and IS2 from the analogue board C.

CVBS Signals:

There are two CVBS input connection possibilities: Front chinch (E5) and Rear Chinch In (E3). Both CVBS sources are connected direct to the STV 6410 and routed to Rear Out 1 and Rear Out 2 via the 75-Ohm driver BA 7623. Both CVBS output sockets are connected to BA 7623 in parallel.
Independent of the input signal quality (CVBS, S-Video or Y/UV) the digital board supplies also S-Video and Y/UV signals to the corresponding sockets.

S-Video Signals:
There are also two S-Video input connection possibilities: Front (E4) and Rear (E2) S-Video In which are connected to the pre-selector IC's BA 7652. One is used for Y, the other for Chroma switching. The output of the pre-selector switches is connected to the STV 6410, and then the signal is routed via the 75-Ohm driver BA 7623 to the Rear Out S-Video socket. Also the video quality will be S-Video, the digital board supplies also CVBS and Y/UV to the corresponding sockets.

Y/UV Signals:
The Y/UV In signal is routed direct to the digital board, there is no Y/UV IN -> Y/UV Out loop through in low power standby. As the digital board supplies only RGB signals, a RGB Y/UV matrix is used. This matrix consists of the operational amplifier TSH95 which generates the U and V signals according the formulas: 2U=B-0,338R-0,661G, 2V=R-0,838G-0,161B. Then the signals are routed to the UV Output sockets via the 75-Ohm driver BA 7623. The corresponding Y signal is coming from the digital board via the STV 6410. The 75 Ohm Y socket is driven by the 75-Ohm driver BA 7623 and finally connected to the of the Y/UV Output.

Detection of Status-Information

WSS on Y/C-Plug:

- Picture-Ratio-Information (16:9 or 4:3) on SVHS-connections is coded via the average DC-level of the Chroma-signal-line, detection is realised by using an analogue-input-port of the CC-C.
- ADC- value lower or equal 40h (4:3-picture-ratio delivered
- ADC-value greater 40h (16:9-picture-ratio available on plug
- Y/C-Rear is determined via Port40/AIN3 (Pin14) of CC (WSRI-line) and Port41/AIN4 (Pin15) is used for Y/C-Front (WSFI-line).

Generation of Status-Information

WSS on Y/C-Plug:
The appropriate DC-level on Chroma-signal-line for Y/C-Rear-Out is produced via Port57 (Pin10) of the CC-C (WSRO-line).

- 4:3 - Picture-ratio supported on Y/C-Plug: Port57 set to 0
- 16:9 - Picture-ratio supported on Y/C-Plug: Port57 set to 1

9.4.9 Audio routing Analogue board (Europe / Nafta)

General Description:
The Audio- I/O switching is realised by the STV6410 I/O switch.
By I^2C Bus (SDA-0/SCL-0) it is possible to control all the Audio in- and outputs (for detailed Information we refer to the STV6410 routing overview).
Analog audio coming from DV-Board and second rear Cinch input is routed via MSP3415 to the STV 6410. After selecting the audio source via STV 6410, the signal must be transformed into the digital domain. For this, the UDA 1360TS (ADC) is responsible. An input-voltage of up to 2Vrms can be handled from the IC´s. For further processing, the UDA 1360TS (ADC) delivers the data-in I^2S format to the digital-board. After a certain delay the (processed) data come back from the digital board to the UDA 1328 (DAC). The UDA 1328 (DAC) transforms the I^2S data back into the analog domain and feeds the signals direct to the MC33078 (OPV). From the MC33078 (OPV) the signals are delivered back to the STV 6410 and also direct to the 2nd rear out Cinch. The other outputs (Scart, Cinch) are supported by the STV 6410.

Detailed Description STV 6410:
The STV 6410 is an I^2C bus controlled audio and video switch matrix, which is able to handle audio input signals up to 2 Vrms. The used outputs are equipped with internal level adjustment possibility. Low distortion and very good channel separation is a typical peculiarity of this IC. The output resistance is very low and the frequency bandwidth is up to 50 kHz.

Detailed Description UDA 1360:
The UDA 1360TS is a stereo Analog-to-Digital Converter employing bitstream conversion techniques.
The UDA supports the I^2S-bus data format and the MSB-justified data format with word lengths of up to 20 bits. The IC supports also 2Vrms input signals and is designed for 3V3 supply voltage.
The device is able to handle system clocks of 256fs and 384fs.
Typical THD+N at 0dB is -85dB and a S/N performance up to 97dB is possible.

Detailed Description UDA 1328:
The UDA1328 is a 6 channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.
The UDA 1328 supports the I^2S-bus data format with word lengths of up to 24 bits.
Digital sound features can be controlled with the L3 interface.
System clock can be set to 256fs or 384fs.
The Device also provides 2 high quality differential outputs.
Typical THD+N at 0dB is -95dB and a S/N of up to 106dB is possible.
Supply voltage is 3V3.

Detailed Description MC 33078:
The MC33078 is a dual operational amplifier for audio applications.
It offers low voltage noise (4,5nV/√Hz) and high frequency performances (15MHz Gain Bandwidth product, 7V/s slew rate).
In addition the MC33078 has a very low distortion (0,002%).

BLOCK DIAGRAM VIDEO IN/OUT NAFTA-VERSION

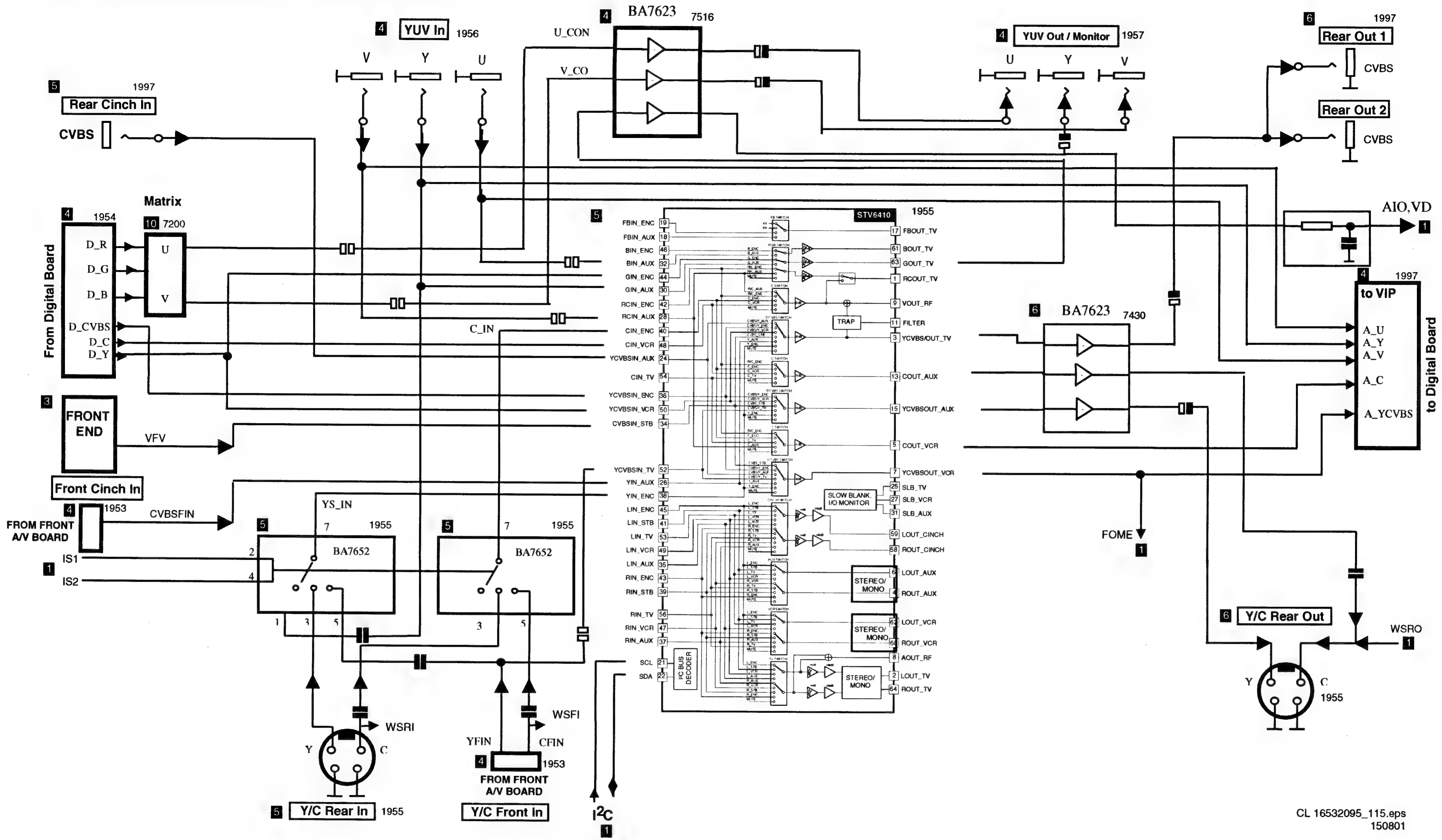

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Figure 9-6

BLOCK DIAGRAM AUDIO IN/OUT NAFTA-VERSION

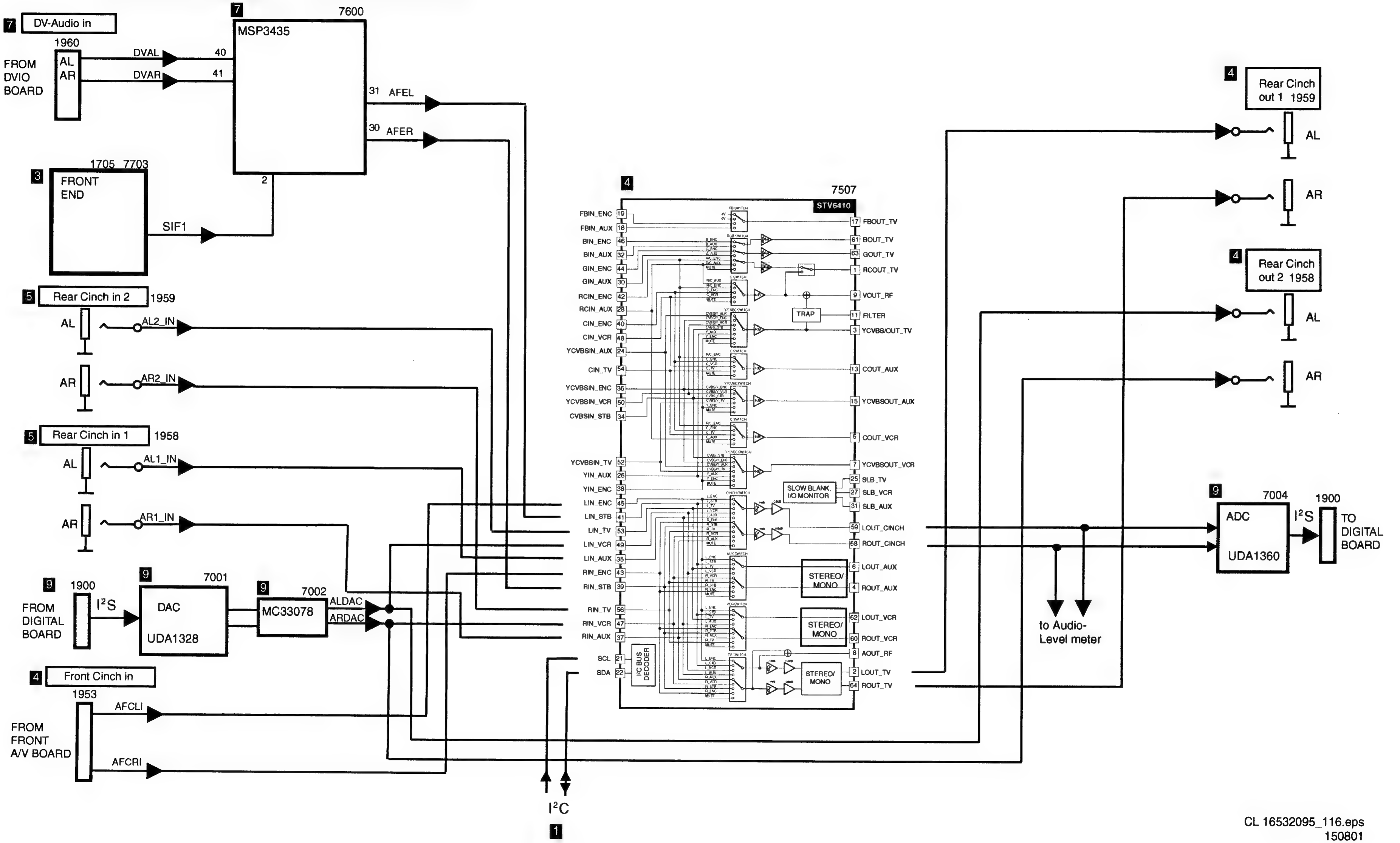

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Figure 9-7

9.5 Digital Board

9.5.1 Record Mode

Video Part

Analog Video input signals CVBS, YC and UV are routed via the analog board to connector 1601 and sent to IC7552 SAA7118 (Video Input Processor). Digital video input signals (DV_IN_DATA(7:0)) are sent from the DIVIO board through the connector 1501 and further also to IC7552.
IC7552 (VIP) decodes the analog video to digital video and processes the digital video to a digital video stream (CCIR656 format). This output stream (VIP_YUV[7:0]) goes to IC7410 SAA6750 (EMPIRE) and to IC7100 Versatile Stream Manager. The latter uses the data for VBI (vertical blanking interval) extraction.
IC7410 (EMPIRE) encodes the digital video stream into a MPEG2 video stream that is fed to IC7100 (VSM).

Audio Part

I2S audio are sent from the analog board to IC7703 DSP56362 (Audio Digital Signal Processor) via connector 1602. The DSP compresses I2S audio data into an AC3/ MPEG1 audio stream which is fed to IC7100 (VSM).

Front-End I2S

IC7100 (VSM) interfaces directly to the different hardware modules such as Basic Engine, MPEG encoder IC7410, MPEG decoder IC7202 (Sti5505) and buffers the data streams that are coming from or going to these hardware modules.
In IC7100 (VSM), the video MPEG2 stream and the audio AC3/MPEG1 stream are multiplexed into a I2S packetized stream. The serial data are sent to the Basic Engine to be recorded.

Loop-Through

The multiplexed audio and video stream in the VSM is fed back via the parallel front-end interface to IC7202 (Sti5505). This IC decodes the MPEG stream into analog video and I2S audio. The video and audio signals are routed to the analog board via connectors 1601 and 1602. During recording, the recorded signal is present at the outputs of the analog board.

9.5.2 Playback Mode

During playback, the serial data from the Basic Engine pass through the VSM and are sent to the Sti5505 via the serial front-end I2S interface.
The Sti5505 is a MPEG & Audio/video decoder and has the following outputs:
To the analog board:

- analog video RGB, YC, CVBS
- I2S audio (PCM format)
- SPDIF audio (digital audio output)

To the Progressive scan board:

- digital video YC(7:0).

9.5.3 S2B Interface

The S2B interface between the Host decoder Sti5505 and the Servo processor MACE3 controls the Basic Engine during record and playback mode.

9.5.4 System Clock

System clock of VSM and Sti5505 (27MHz) is generated by oscillator 7802.

9.5.5 Audio Clock

During record mode, the audio clock ACC_ACLK_OSC is generated by IC7806 (PLL) because then, the audio clock must be sychronized with the incoming video (VIP_FID) from the VIP.
During playback mode, the audio clock ACC_ACLK_PLL is generated by the clock synthesizer IC7800 (MK2703).
Both ACC_ACLK_OSC and ACC_ACLK_PLL are fed to the VSM. This IC selects the appropriate clock fo the audio decoder. From the incoming audio clocks, the VSM derives the I2S audio encoder clocks AE_BCLK and AE_WCLK.

9.5.6 ON/OFF

The digital board is not powered in standby mode. Control signal ION, coming from the analog board, will enable the PSU and power the digital board.

- ION = High: the digital board is in powered down standby mode
- ION = Low: the power supply to the digital board is enabled

9.5.7 RESET

Control signal IRESET_DIG, controlled by the microprocessor on the analog board is sent to the RESET LOGIC circuit.

- IRESET_DIG = Low in standby mode
- IRESET_DIG = High: the whole system is reset and the Digital board is waked up.

9.5.8 I2C Bus

Sti5505 is master of the I2C bus. The following IC's are controlled by the I2C bus:

- IC7200 NVRAM
- IC7703 DSP56362
- IC7410 EMPIRE
- IC7552 VIP
- IC7900 Programmed Input/Output: LOAD_BE, LOAD_DVN, ANA_WE, L3_STROBE.
- IC7917 Programmed Input/Output: CENTRE_ON_STEREO, ADC_ENABLEN

9.5.9 EMI Bus

The following IC's are connected to the External Memory Interface bus (EMI) which functions as system bus:

- IC7302 and 7304: Flash memories which contain the application and diagnostic software
- IC7300 and 7301: DRAM's .
- IC7100: VSM
- IC7703: DSP56362: only for downloading the microclock into the IC
- IC7202: MPEG AV Decoder

BLOCK DIAGRAM DIGITAL BOARD

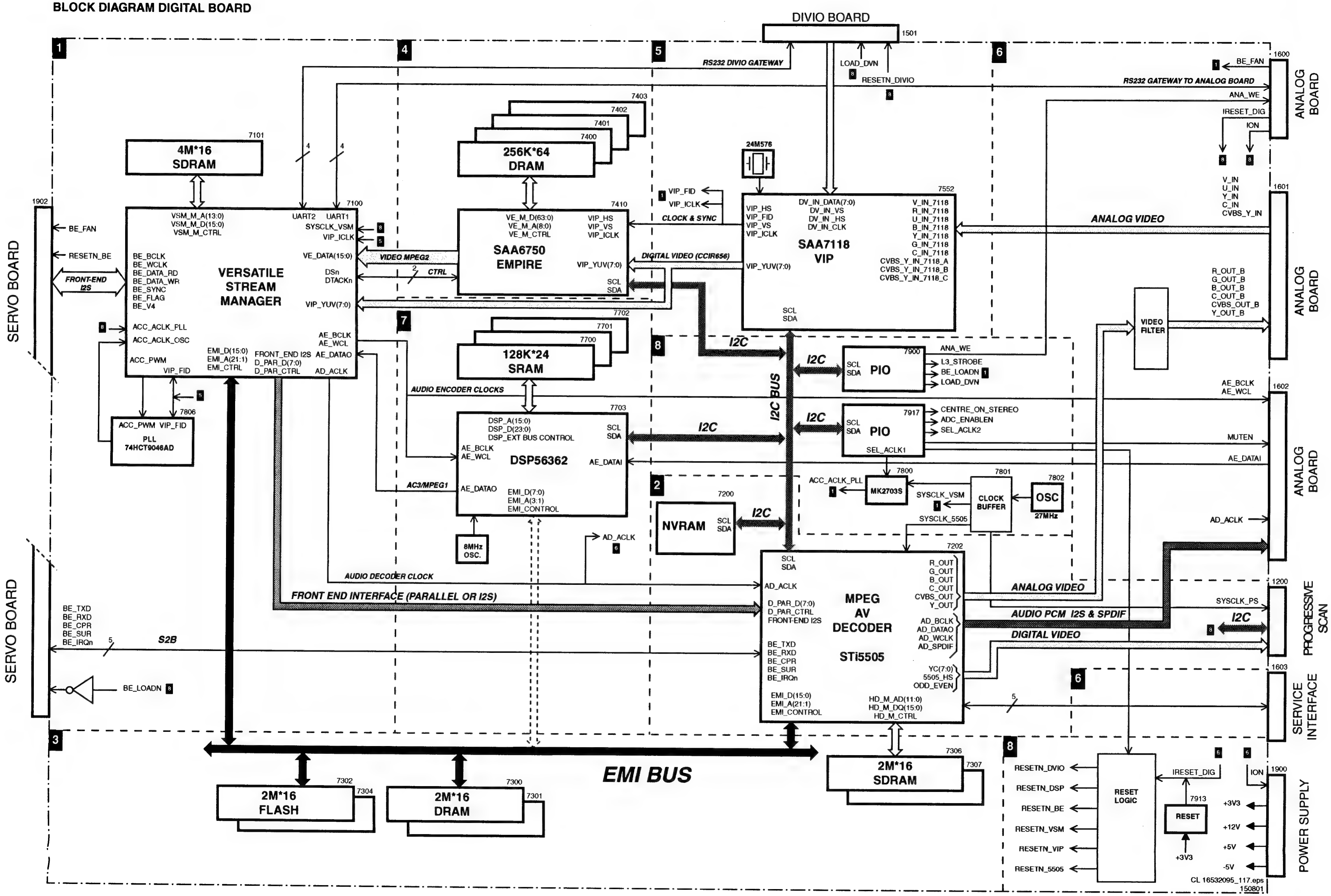

Figure 9-8

9.6 Divio Board

9.6.1 Short Description of the Module:

The DVIO Module is a decoder for DV streams. The module is intended for the Philips DVDR1000/001 en DVDR1000/171 DVD+RW recorders. Input is a stream from a DV-camcorder IEEE1394. Outputs are CCIR656 Video and Analog audio (L+R). A serial control interface is present. The following picture shows the location of the DVIO Module inside the DVDR set.

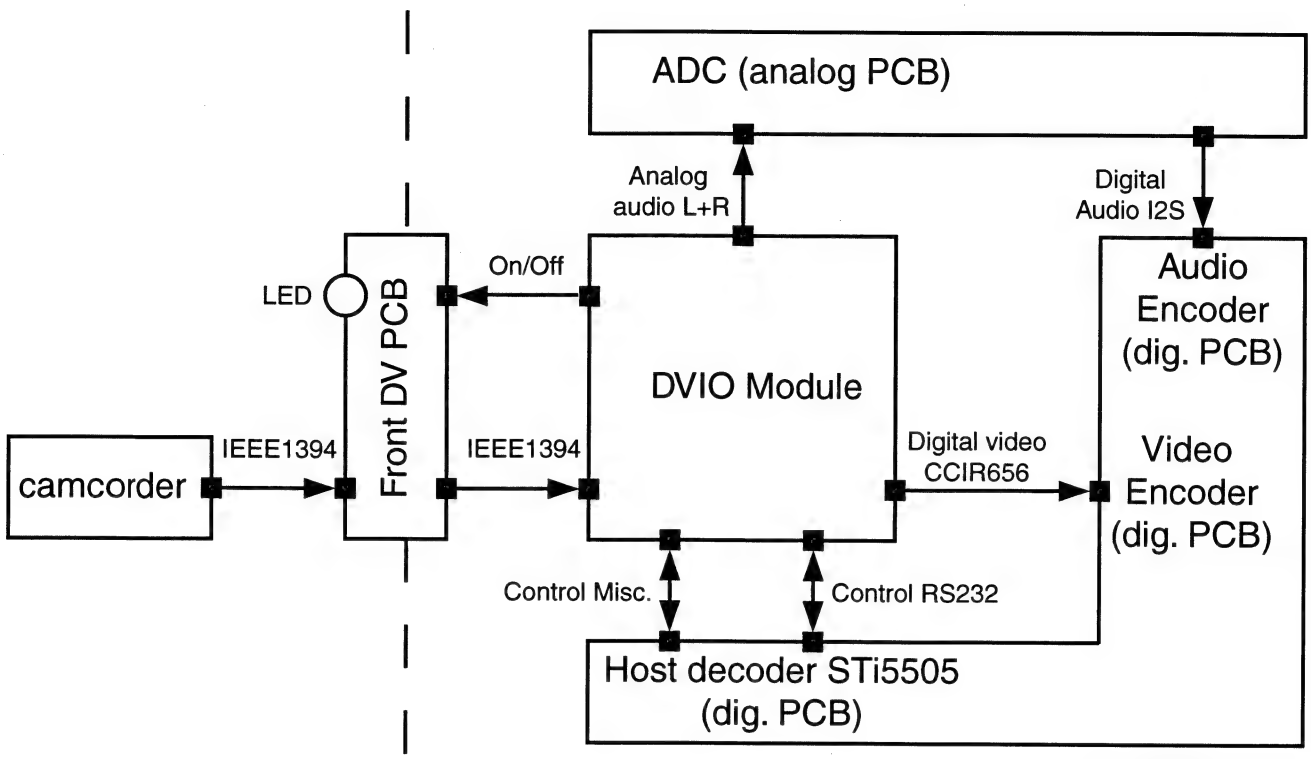

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Figure 9-9

9.6.2 Block Diagram

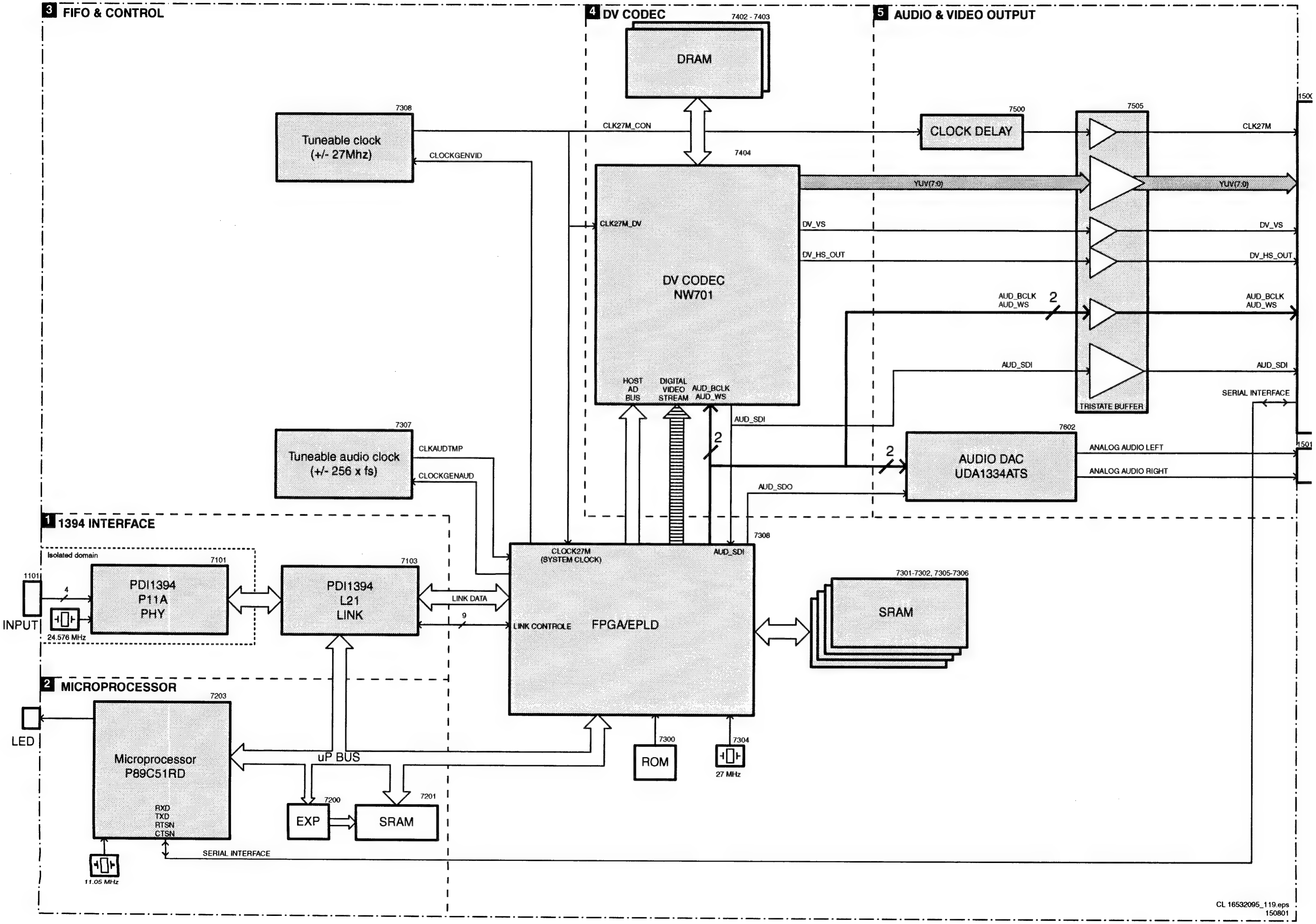


Figure 9-10

9.6.3 Functional Description

The DVIO module consists of the following blocks (see blockdiagram):

1. IEEE1394 Interface
   - PDI1394P11A (7101)
   - PDI1394L21(7103)
2. Micro-controller
   - 89C51RD(7203)
   - 32kb RAM(7201)
3. FIFO and Control
   - FPGA/EPLD(7308)
   - SRAM(7301, 7302, 7305, 7306)
   - Clock generation(7307, 7308)
     - Independently tuneable audio and video clock, implemented with FPGA and PLL
4. DV-Codec
   - NW701(7404)
   - DRAM(7402, 7403)
5. Audio & Video output
   - Audio DAC UDA1334ATS(7602)
   - Clock delay(7500)
   - Tristate buffer(7505)

IEEE1394 Interface

The 1394 interface consists of a PDI1394P11A physical layer and a PDI1394L21 link layer. The physical layer has its own isolated power supply. It has the following features:

- S200 operation (200 megabit per second)
- One i.Link port (4 pin)
- 1nF isolation barrier between link and phy
- AV link port
- Isolated power supply for phy

Micro-Controller

The 89C51RD processor has a 8051 cpu with the following extra features:

- 64 kilobyte of flash memory as program memory
- 1 kilobyte of internal data memory
- watchdog timer
- PCA outputs
- Power control modes
- Speed allowed up to 33 MHz but used at 22.1184 MHz
- On board ISP(In Circuit Programming) functionality

ISP

By use of In Circuit Programming, it is possible to update the software of the DVIO board that is in the 89C51RD+. ISP can be made active by resetting the processor and keeping the ISPN pin low during reset. During ISP, the ISPN signal on the board has to be kept low. This because the ISPN signal not only drives the PSEN pin low, but will also put 12V instead of 5V on the VPP pin. When the ISP mode is active, the new program can be sent to the microprocessor through the serial port.

Fifo & Control

In decode mode, an isochronous AV-stream is flowing through the IEEE1394 Interface into the FPGA. The FPGA stores the data in a FIFO buffer (ping-pong buffer type, i.e. 2 buffers that can hold one whole frame each).

Reset

The FPGA controls the reset signals on the board. This has the advantage that it is possible to reset the board both from software and hardware.

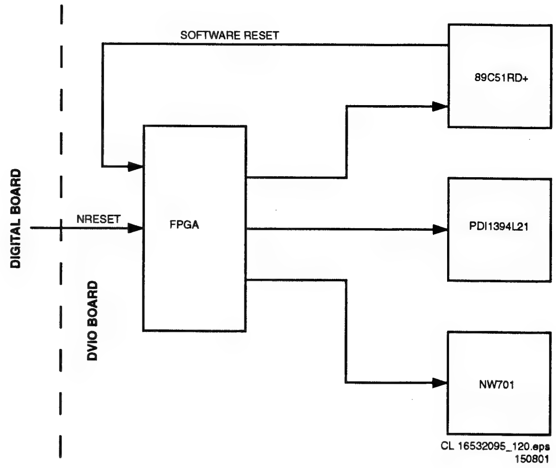


Figure 9-11

The board reset NRESET will reset the whole board, and the software reset can reset everything except the microprocessor itself. Power-on reset is implemented by adding pull-ups and pull-downs to the reset inputs of the devices. Since the FPGA will tri-state all the pins during configuration, reset is active during configuration time. After configuration of the FPGA, the reset signals are driven inactive. The NRESET signal is used to reset the DVIO board. After reset, the tri-state buffers to connector 1500 are disabled.

Clock Circuit

There are 2 clocks to consider in the system, this is the video clock and the audio clock. These two clocks do not have a relation, so these clocks must be considered independently. The video clock is approximately 27 MHz. When data is flowing from an external source that is supposed to have the same frequency, it does not have exactly the same clock. Because of this, buffers may under-run of over-run. Since the clock can not be directly recovered from the 1394 interface, there has to be another solution. This solution is a tuneable clock that is adjusted to the required frequency to process at the rate of the incoming data.

The hardware implementation of such a tuneable clock is as follows:

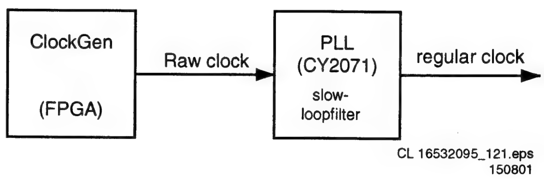


Figure 9-12

The same can be applied for the audio clock. For this clock, a frequency of 8.192 MHz, 11.2896 MHz or 12.228 MHz is required. This depends on the sample-rate of the audio signal.

DV Codec

The AV-data will go from the FIFO to the NW701. The NW701 decodes the stream into video data in 656 format and audio data in I2S format.

The microprocessor has the ability to read the status registers of the NW701 through the FPGA. By reading these registers, extra data from the DV stream, that is not decoded into audio or video, can be sent to the digital board using pin TXD of the serial interface. This data includes time stamp and some more.

Audio & Video Output
The audio I2S data are sent to audio DAC UDA1334. Analog audio left and right signals are connected to the analog board.
The tristate buffer enables the digital video stream to the Video Input Processor on the digital board when the DV source is selected.
The clock delay synchronizes the AV clock with the AV data at the output.

9.7 Progressive Scan

9.7.1 Block Diagram

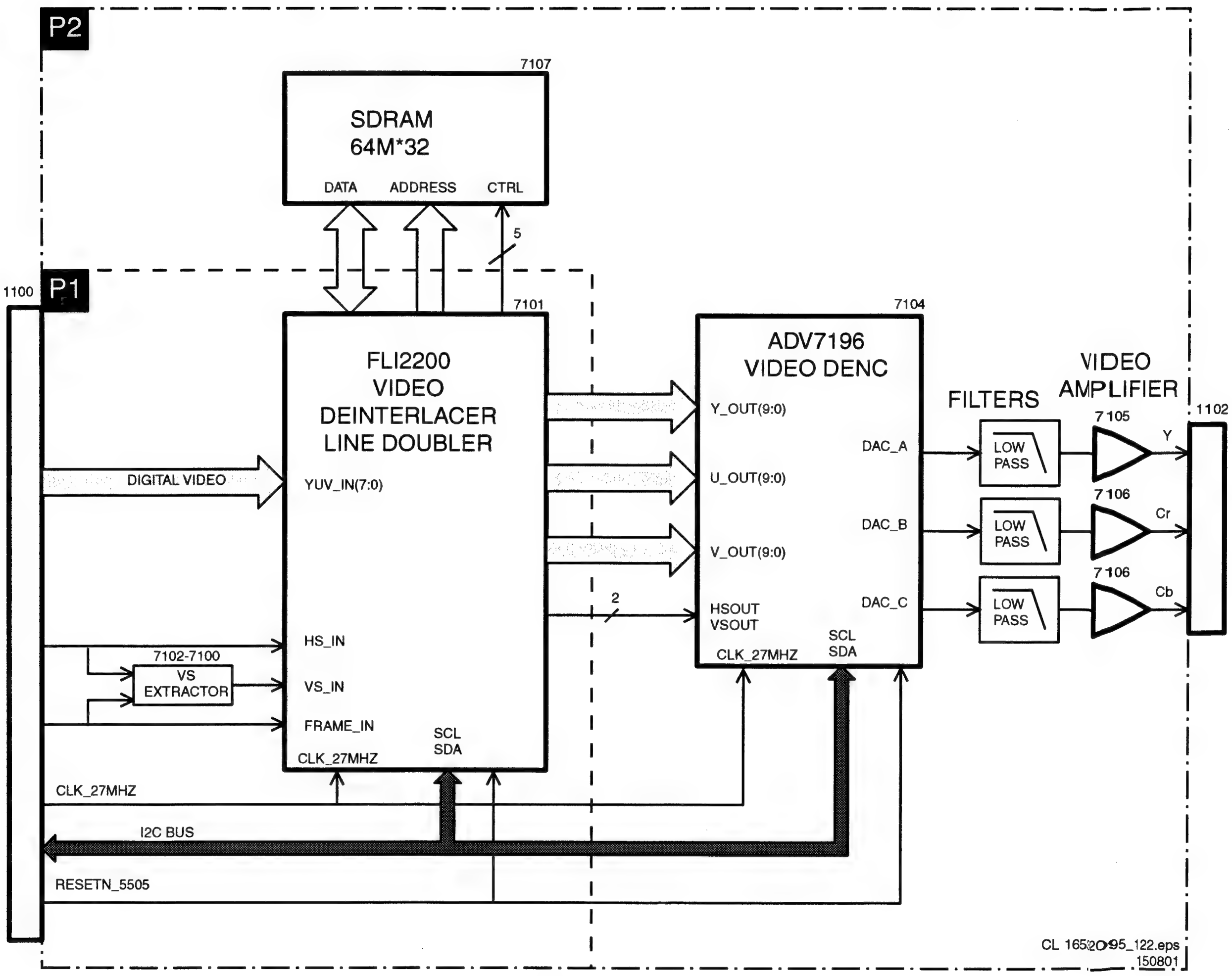


Figure 9-13

9.7.2 Description

The progressive scan module, used in the first generation DVD+RW player, is built around the SAGE Fli2200 de-interlacer / line doubler (7101). This I2C controlled de-interlacer uses a 64Mbit SDRAM (32bit x 2M) to perform high quality deinterlacing (meshing). The de-interlacer gets his digital YUV input data from the STi5505 (7202), located on the digital board. Via a 24-poled flex, digital video, power supply, reset and I2C is connected to the board. The format of the digital YUV input to the SAGE is CCIR656 with separated Hsync, Vsync and odd/even signal running on 27Mhz.
Because the STi5505 doesn't have a Vsync output the odd/even output of this IC has to be translated to a Vsync signal. Some glue logic has been added to extract the vertical sync. The glue logic circuit consists of Flip-Flop IC 74HC74D (7102) and EXOR 74LVC86 (7100). The next diagram shows how the vertical sync is extracted.

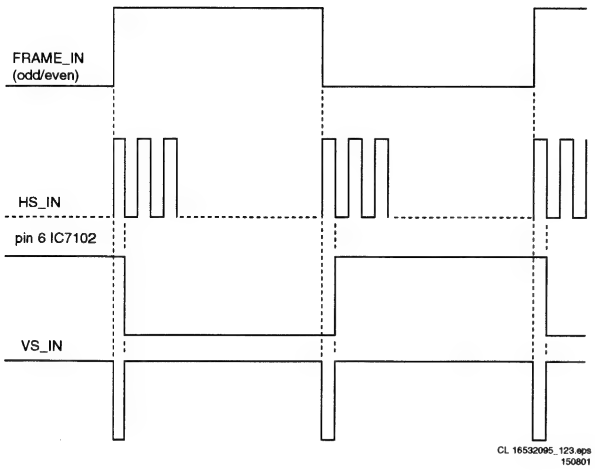


Figure 9-14

The output of the de-interlacer (4:4:4 progressive video) is fed to the Analog Devices AD7196 MacroVision compliant DENC (7104).
The YUV current output of the DENC is fed via a low pass filter to the single supply output opamps AD8061/8062 (7105-7106). The analog video is fed via a 7 poled flex to the analog board where the YUV 2FH cinch connectors are located.
The board uses as power supply 3.3V and 5V. The 2,5V power required for the SAGE is derived locally from the 3.3V with voltage regulator LF25C (7103).

9.8 IC's Analogue Board

9.8.1 IC7001: UDA1328T

Multi-channel filter DAC

UDA1328T

BITSTREAM CONVERSION

1 FEATURES

1.1 General

- 2.7 to 3.6 V power supply
- 5 V tolerant TTL compatible inputs
- Selectable control via L3 microcontroller interface or via static pin control
- Multi-channel integrated digital filter plus non-inverting Digital-to-Analog Converter (DAC)
- Supports sample frequencies between 5 and 100 kHz
- Digital silence detection (output)
- Slave mode only applications
- No analog post filtering required for DAC
- Easy application.

1.2 Multiple format input interface

- I^2S-bus, MSB-justified and LSB-justified format compatible (in L3 mode)
- I^2S-bus and LSB-justified format compatible
- $1f_s$ input format data rate.

1.3 Multi-channel DAC

- 6-channel DAC with power on/off control
- Digital logarithmic volume control via L3; volume can be set for each of the channels individually
- Digital de-emphasis for 32, 44.1, 48 and 96 kHz f_s via L3 and, for 32, 44.1 and 48 kHz in static mode
- Soft or quick mute via L3
- Output signal polarity control via L3 microcontroller interface.

1.4 Advanced audio conÞguration

- 6-channel line output (under L3 volume control)
- A stereo differential output (channel 1 and channel 2) for improved performance
- High linearity, wide dynamic range, low distortion.

2 APPLICATIONS

This multi-channel DAC is eminently suitable for DVD-like applications in which 5.1 channel encoded signals are used.

3 GENERAL DESCRIPTION

The UDA1328 is a single-chip 6-channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.

The UDA1328 supports the I^2S-bus data format with word lengths of up to 24 bits, the MSB-justified data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 18, 20 and 24 bits.

All digital sound processing features can be controlled with the L3 interface e.g. volume control, selecting digital silence type, output polarity control and mute. Also system features such as power control, digital silence detection mode and output polarity control.

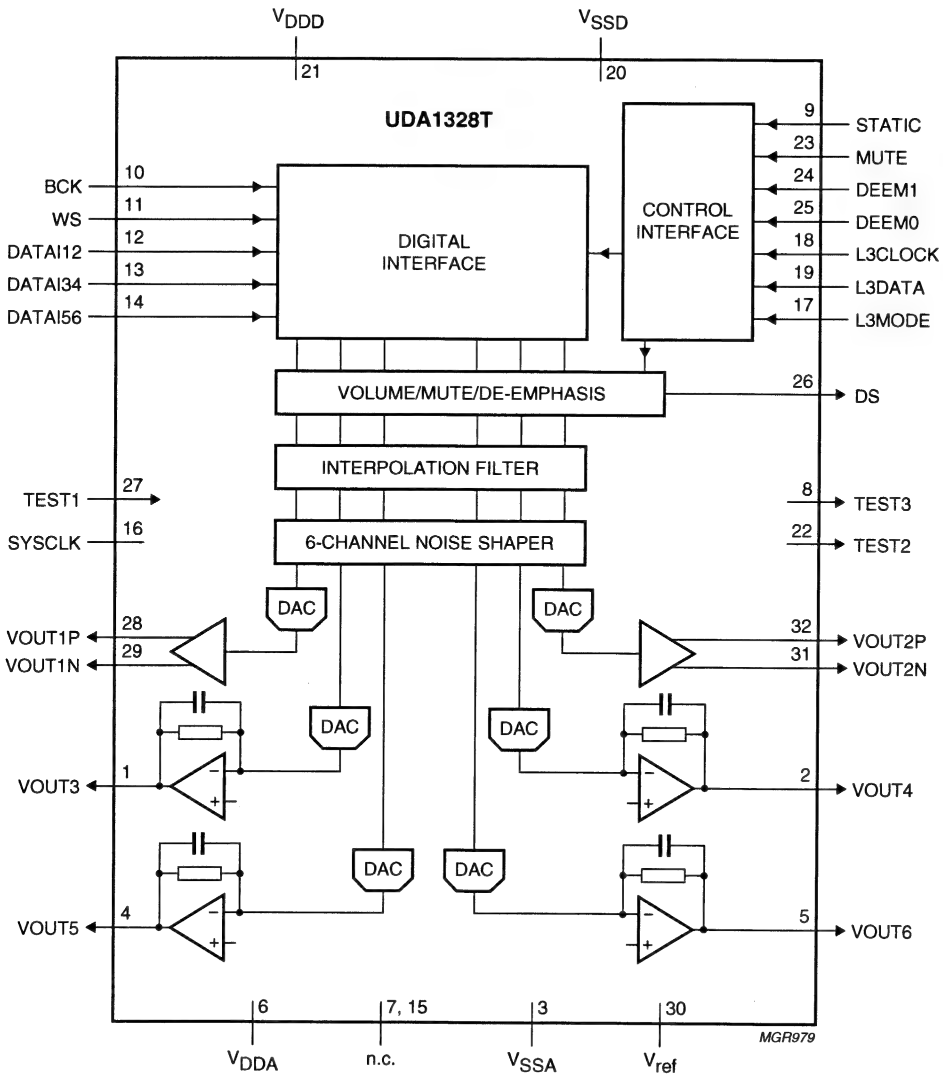
Under static pin control, via static pins, the system clock can be set to either $256f_s$ or $384f_s$ support, digital de-emphasis can be set, there is digital mute and the digital input formats can also be set.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1328T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

Multi-channel filter DAC UDA1328T

6 BLOCK DIAGRAM



Multi-channel filter DAC UDA1328T

7 PINNING

SYMBOL	PIN	DESCRIPTION
VOUT3	1	channel 3 analog output
VOUT4	2	channel 4 analog output
V_{SSA}	3	analog ground
VOUT5	4	channel 5 analog output
VOUT6	5	channel 6 analog output
V_{DDA}	6	analog supply voltage
n.c.	7	not connected (reserved)
TEST3	8	test output 3
STATIC	9	static mode/L3 mode switch input
BCK	10	bit clock input
WS	11	word select input
DATAI12	12	data input channel 1 and 2
DATAI34	13	data input channel 3 and 4
DATAI56	14	data input channel 5 and 6
n.c.	15	not connected (reserved)
SYSCLK	16	system clock: $256f_s$, $384f_s$, $512f_s$ and $768f_s$
L3MODE	17	L3 mode selection input
L3CLOCK	18	L3 clock input
L3DATA	19	L3 data input
V_{SSD}	20	digital ground
V_{DDD}	21	digital supply voltage
TEST2	22	test output 2
MUTE	23	static mute control input
DEEM1	24	DEEM control 1 input (static mode)
DEEM0	25	L3 address select (L3 mode)/DEEM control 0 input (static mode)
DS	26	digital silence detect output
TEST1	27	test input 1
VOUT1P	28	channel 1 analog output P
VOUT1N	29	channel 1 analog output N
V_{ref}	30	DAC reference voltage
VOUT2N	31	channel 2 analog output N
VOUT2P	32	channel 2 analog output P

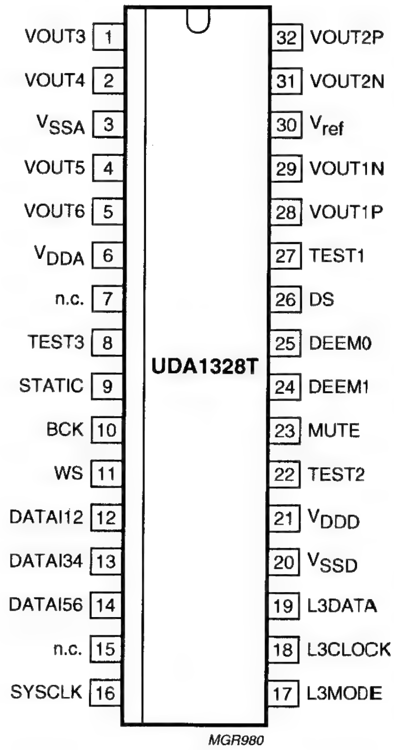


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1328 operates in slave mode only, this means that in all applications the system must provide the system clock. The system frequency is selectable. The options are $256f_s$, $384f_s$, $512f_s$ and $768f_s$ for the L3 mode and $256f_s$ or $384f_s$ for the static mode. The system clock must be frequency-locked to the digital interface signals.

It should be noted that the UDA1328 can operate from 5 to 100 kHz sampling frequency (f_s). However in $768f_s$ mode the sampling frequency must be limited to 55 kHz.

8.2 Application modes

Operating mode can be set with the STATIC pin, either to L3 mode (STATIC = LOW) or to the static mode (STATIC = HIGH). See Table 1 for pin functions in the static mode.

Table 1 Mode selection in the static mode

PIN	L3 MODE	STATIC MODE
L3CLOCK	L3CLOCK	clock select
L3MODE	L3MODE	SF1(1)
L3DATA	L3DATA	SF0(1)
MUTE	X(2)	MUTE
DEEM1	X(2)	DEEM1
DEEM0	L3ADR	DEEM0

Notes

1. SF1 and SF0 are the Serial Format inputs (2-bit).
2. X means that the pin has no function in this mode and can best be connected to ground.

8.3 Interpolation Þlter (DAC)

The digital filter interpolates from 1 to $128f_s$ by cascading a half-band filter and a FIR filter, see Table 2. The overall filter characteristic of the digital filters is illustrated in Fig.3, and the pass-band ripple is illustrated in Fig.4. Both figures are with a 44.1 kHz sampling frequency.

Table 2 Interpolation Þlter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	±0.02
Stop band	$>0.55f_s$	−55
Dynamic range	0 to $0.45f_s$	>114
DC gain	−	−3.5

8.4 Digital silence detection

The UDA1328 can detect digital silence conditions in channels 1 to 6, and report this via the output pin DS. This function is implemented to allow for external manipulation of the audio signal in the absence of program material, such as muting or recorder control.

An active LOW output is produced at the DS pin if the channels selected via L3 or for all channels in static mode, carries all zeroes for at least 9600 consecutive audio samples (equals 200 ms for f_s = 48 kHz). The DS pin is also active LOW when the output is digitally muted either via the L3 interface or via the STATIC pin.

In static mode all channels participate in the digital silence detection. In L3 mode control each channel can be set, either to participate in the digital silence detection or not.

8.5 Noise shaper

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream DAC (FSDAC).

8.6 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post-filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

8.7 Static mode

The UDA1328 is set to static mode by setting the STATIC pin HIGH. The function of 6 pins of the device now get another function as can be seen in Table 1.

8.7.1 SYSTEM CLOCK SETTING

In static mode pin 18 (L3CLOCK) is used to select the system clock setting. When pin 18 is LOW, the device is in $256f_s$ mode, when pin 18 is HIGH the device is in $384f_s$ mode.

8.7.2 De-emphasis control

In static pin mode the pins DEEM0 and DEEM1 control the de-emphasis mode; see Table 3.

Table 3 De-emphasis control

DEEM MODE	DEEM1	DEEM0
No de-emphasis	0	0
32 kHz de-emphasis	0	1
44.1 kHz de-emphasis	1	0
48 kHz de-emphasis	1	1

8.7.3 Digital interface formats

In static pin mode the digital audio interface formats can be selected via pin 17 (SF1) and 19 (SF0). The following interface formats can be selected (see also Table 4):

- I^2S-bus with data word length of up to 24 bits
- LSB-justified format with data word length of 16, 20 or 24 bits.

Table 4 Input format selection in the static mode

INPUT FORMAT	SF1	SF0
I^2S-bus	0	0
LSB-justiÞed 16bits	0	1
LSB-justiÞed 20bits	1	0
LSB-justiÞed 24bits	1	1

It should be noted that the digital audio interface holds that the BCK frequency can be 64 times the WS maximum frequency, or $f_{BCK} \leq 64 \times f_{WS}$

8.8 L3 mode

The device is set to L3 mode by setting the STATIC pin to LOW. The device can then be controlled via the L3 microcontroller interface (see Chapter 9).

8.8.1 Digital interface formats

The following interface formats can be selected in the L3 mode:

- I^2S-bus with data word length of up to 24 bits
- MSB-justified with data word length of up to 24 bits
- LSB-justified format with data word length of 16, 18, 20 or 24 bits.

8.8.2 L3 address

The UDA1328 can be addressed via the L3 microcontroller interface using one of two addresses. This is done in order to individually control the UDA1328 and other Philips DACs or CODECs via the same L3 bus.

The address can be selected using pin 25 (DEEM0) in L3 mode. When pin 25 is set LOW, the address is 000100. When pin 25 is set HIGH the address is 000101.

9.8.2 IC7004: UDA1360TS

Low-voltage low-power stereo audio ADC UDA1360TS

BITSTREAM CONVERSION

FEATURES

General

- Low power consumption
- 2.4 to 3.6 V power supply
- Supports 256 and $384f_s$ system clock
- Supports sampling frequency range of 5 to 55 kHz
- Small package size (SSOP16)
- Integrated high-pass filter to cancel DC offset
- Power-down mode
- Supports 2 V (RMS) input signals
- Easy application
- Non-inverting ADC plus decimation filter.

Multiple format output interface

- I^2S-bus and MSB-justified format compatible
- Up to 20 significant bits serial output.

Advanced audio configuration

- Stereo single-ended input configuration
- High linearity, dynamic range and low distortion.

GENERAL DESCRIPTION

The UDA1360TS is a single chip stereo Analog-to-Digital Converter (ADC) employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording functions.

The UDA1360TS supports the I^2S-bus data format and the MSB-justified data format with word lengths of up to 20 bits.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
I_{DDA}	analog supply current		–	9	–	mA
I_{DDD}	digital supply current		–	3.5	–	mA
T_{amb}	operating ambient temperature		–40	–	+85	°C
ADC						
$V_{i(rms)}$	input voltage (RMS value)	see Table 1	–	1.0	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–37	–33	dB
S/N	signal-to-noise ratio	V_I = 0 V; A-weighted	–	97	–	dB
α_{cs}	channel separation		–	100	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1360TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

Low-voltage low-power stereo audio ADC UDA1360TS

BLOCK DIAGRAM

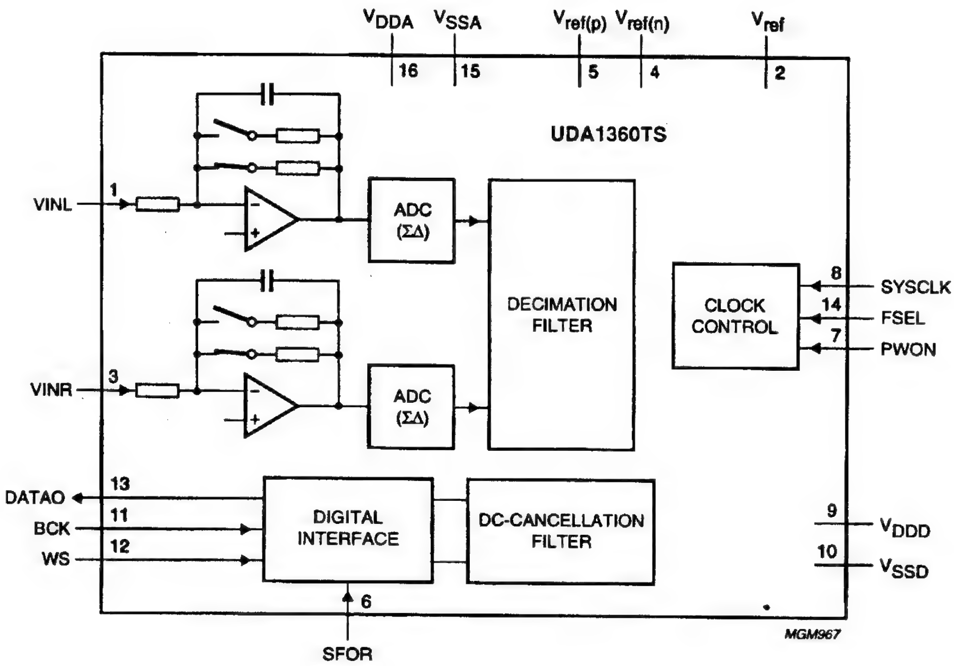


Fig.1 Block diagram.

Low-voltage low-power stereo audio ADC UDA1360TS

PINNING

SYMBOL	PIN	DESCRIPTION
VINL	1	left channel input
V_{ref}	2	reference voltage
VINR	3	right channel input
$V_{ref(n)}$	4	ADC negative reference voltage
$V_{ref(p)}$	5	ADC positive reference voltage
SFOR	6	data format selection input
PWON	7	power control input
SYSCLK	8	system clock input 256 or $384f_s$
V_{DDD}	9	digital supply voltage
V_{SSD}	10	digital ground
BCK	11	bit clock input
WS	12	word selection input
DATAO	13	data output
FSEL	14	system clock frequency select
V_{SSA}	15	analog ground
V_{DDA}	16	analog supply voltage

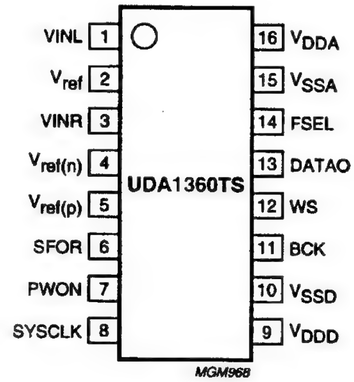


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

System clock

The UDA1360TS accommodates slave mode only, this means that in all applications the system devices must provide the system clock. The system frequency is selectable via the static FSEL pin, and the system clock must be locked in frequency to the digital interface input signals.

The options are $256f_s$ (FSEL = LOW) and $384f_s$ (FSEL = HIGH). The sampling frequency range is 5 to 55 kHz.

The BCK clock can be up to $128f_s$, or in other words the BCK frequency is 128 times the Word Select (WS) frequency or less: $f_{BCK} \leq 128 \times f_{WS}$.

Notes:

1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface.
2. For MSB justified formats it is important to have a WS signal with 50% duty factor.

Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1360TS consists of two 3rd-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The over-sampling ratio is 128.

Input level

The overall system gain is proportional to V_{DDA}. The 0 dB input level is defined as that which gives a −1 dB FS digital output (relative to the full-scale swing). In addition, an input gain switch is incorporated with the above definitions.

The UDA1360TS front-end is equipped with a selectable 0 or 6 dB gain, in order to supports 2 V (RMS) input using a series resistor of 12 kΩ.

For the definition of the pin settings for 1 or 2 V (RMS) mode given in Table 1, it is assumed that this resistor is present as a default component.

If the 2 V (RMS) signal input is not needed, the external resistor should not be used.

Table 1 Application modes using input gain stage

RESISTOR (12 kΩ)	INPUT GAIN SWITCH	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS)
Present	6 dB	1 V (RMS)
Absent	0 dB	1 V (RMS)
Absent	6 dB	0.5 V (RMS)

Multiple format output interface

The UDA1360TS supports the following data output formats:

- I^2S-bus with data word length of up to 20 bits
- MSB-justified serial format with data word length of up to 20 bits.

The output format can be set by the static SFOR pin. When SFOR is LOW, the I^2S-bus is selected, when SFOR is set HIGH the MSB-justified format is selected.

The data formats are illustrated in Fig.4. Left and right data channel words are time multiplexed.

Decimation filter

The decimation from $128f_s$ is performed in two stages. The first stage realizes 3rd-order sin x/x characteristic. This filter decreases the sample rate by 16. The second stage (an FIR filter) consists of 3 half-band filters, each decimating by a factor of 2.

Table 2 DC cancellation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple		none
Pass-band gain		0
Stop band	$>0.55f_s$	−60
Droop	at $0.00045f_s$	0.031
Attenuation at DC	at $0.00000036f_s$	>40
Dynamic range	0 to $0.45f_s$	>110

Mute

On recovery from power-down, the serial data output DATAO is held LOW until valid data is available from the decimation filter. This time tracks with the sampling frequency:

$$t = \frac{12288}{f_s} = 279\text{ ms}\ ;\ \text{where } f_s = 44.1\text{ kHz.}$$

Power-down mode

The PWON pin can control the power saving together with the optional gain switch for 2 V (RMS) or 1 V (RMS) input. When the PWON pin is set LOW, the ADC is set to power-down. When PWON is set to HIGH or to half the power supply, then either 6 dB gain or 0 dB gain in the analog front-end is selected.

Application modes

The UDA1360TS can be set to different modes using two 3-level pins and one 2-level pin. The selection of modes is given in Table 3.

Table 3 Mode selection summary

PIN	V_{SS}	$\frac{1}{2}V_{DD}$	V_{DD}
SFOR	I^2S-bus	test mode	MSB
PWON	power-down	0 dB gain	6 dB gain
FSEL	$256f_s$	–	$384f_s$

9.8.3 IC7430: BA7660FS

3-channel 75Ω driver
BA7660FS

The BA7660FS is a 75Ω driver with a 6dB amplifier and three internal circuits, and provides 75Ω drive of composite Y signals and C signals, as well as RGB signals. Each load is capable of driving two circuits, and a sag correction function reduces the capacitance of the output coupling capacitor.
The input voltage is within a range of 0V to 1.5V, enabling direct connection of ordinary D / A converter output. An internal power-saving circuit is also included which provides simultaneous muting on all three channels, and output pin shorting protection.

●Applications
DVDs, set top boxes and other digital video devices

●Features
1) Can be coupled directly to D / A converter output.
2) Operates at a low power consumption (115mW typ.).
3) Internal output muting circuit.
4) Internal power-saving circuit.
5) Internal output protection circuit.
6) An internal sag correction function makes it possible to reduce the capacitance of the output coupling capacitor.
7) Each load is capable of driving two circuits.
8) The compact 16-pin SSOP-A package is used.

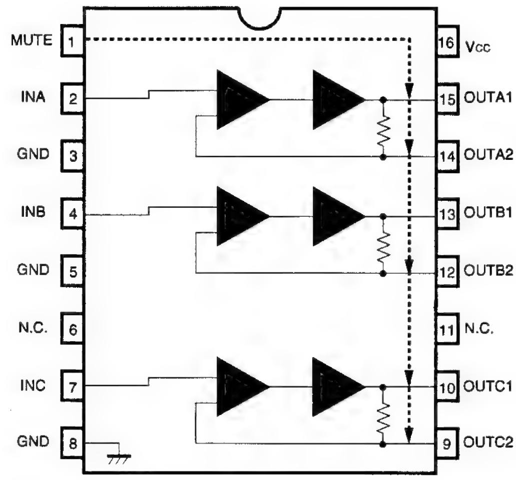
●Absolute maximum ratings (Ta = 25C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	8	V
Power dissipation	Pd	650	mW
Operating temperature	Topr	– 25 ~ + 75	°C
Storage temperature	Tstg	– 55 ~ + 125	°C

●Recommended operating conditions (Ta = 25C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating power supply voltage	Vcc	4.5	5.0	5.5	V

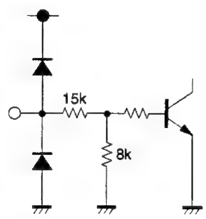
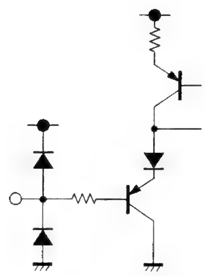
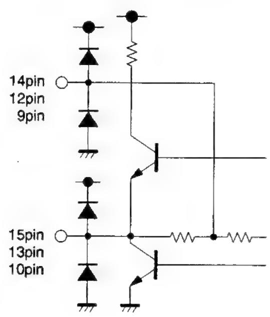
●Block diagram



MUTE (1pin)

H	3ch MUTE
L	NORMAL

●Pin descriptions and input / output circuits

Pin. No	Pin name	IN	OUT	Reference voltage	Equivalent circuit	Function
1	MUTE	K	—	—		Muting control If MUTE (pin 1) is set to HIGH, muting is carried out simultaneously on all three channels.
2 4 7	INA INB INC	K	—	—		Signal input Input signals consist of composite video signals, Y signals, C signals, RGB, and others. The input level is within a range of 0 to 1.3 (min.) to 1.5 (typ.).
3 5 8	GND	—	—	0V		Ground
14 12 9 15 13 10	OUTA2 OUTB2 OUTC2 OUTA1 OUTB1 OUTC1	—	K	0.9V 0.95V		Signal output The signal output level is (0.9 + 2 × input voltage [V]). Pins 9, 12, and 14 are the pins for sag correction. If pins 10, 13, and 15 are set to 0.2V or less, the protective circuit is triggered and the power-saving mode is accessed.
16	Vcc	—	—	5.0V		Power supply

9.8.4 IC7507: STV6410

STV6410

AUDIO/VIDEO SWITCH MATRIX

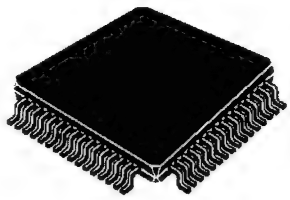
- I²C BUS CONTROL
- STANDBY MODE

VIDEO SECTION

- 5 CVBS INPUTS, 4 CVBS OUTPUTS (ONE WITH SELECTABLE CHROMA TRAP FILTER)
- 5 Y/C INPUTS, 3 Y/C OUTPUTS
- 6dB GAIN ON ALL CVBS/Y AND C OUTPUTS
- 1 Y/C ADDER
- 2 RGB/FB INPUTS, 1 RGB/FB OUTPUT WITH 6dB ADJUSTABLE GAIN
- VIDEO MUTING ON ALL THE OUTPUTS
- 3 SLOW BLANKING INPUTS/OUTPUTS
- SYNC BOTTOM CLAMP ON ALL CVBS/Y AND RGB INPUTS, AVERAGE ON C INPUTS
- BANDWIDTH : 15MHz
- CROSSTALK : 60dB Typ.

AUDIO SECTION

- 5 STEREO INPUTS, 4 STEREO OUTPUTS (TWO WITH LEVEL ADJUSTMENT)
- MONO SOUND OUTPUT
- MONO SOUND CAPABILITY ON TV OUTPUTS
- AUDIO MUTING ON ALL THE OUTPUTS



TQFP64
(Plastic Quad Flat Pack)

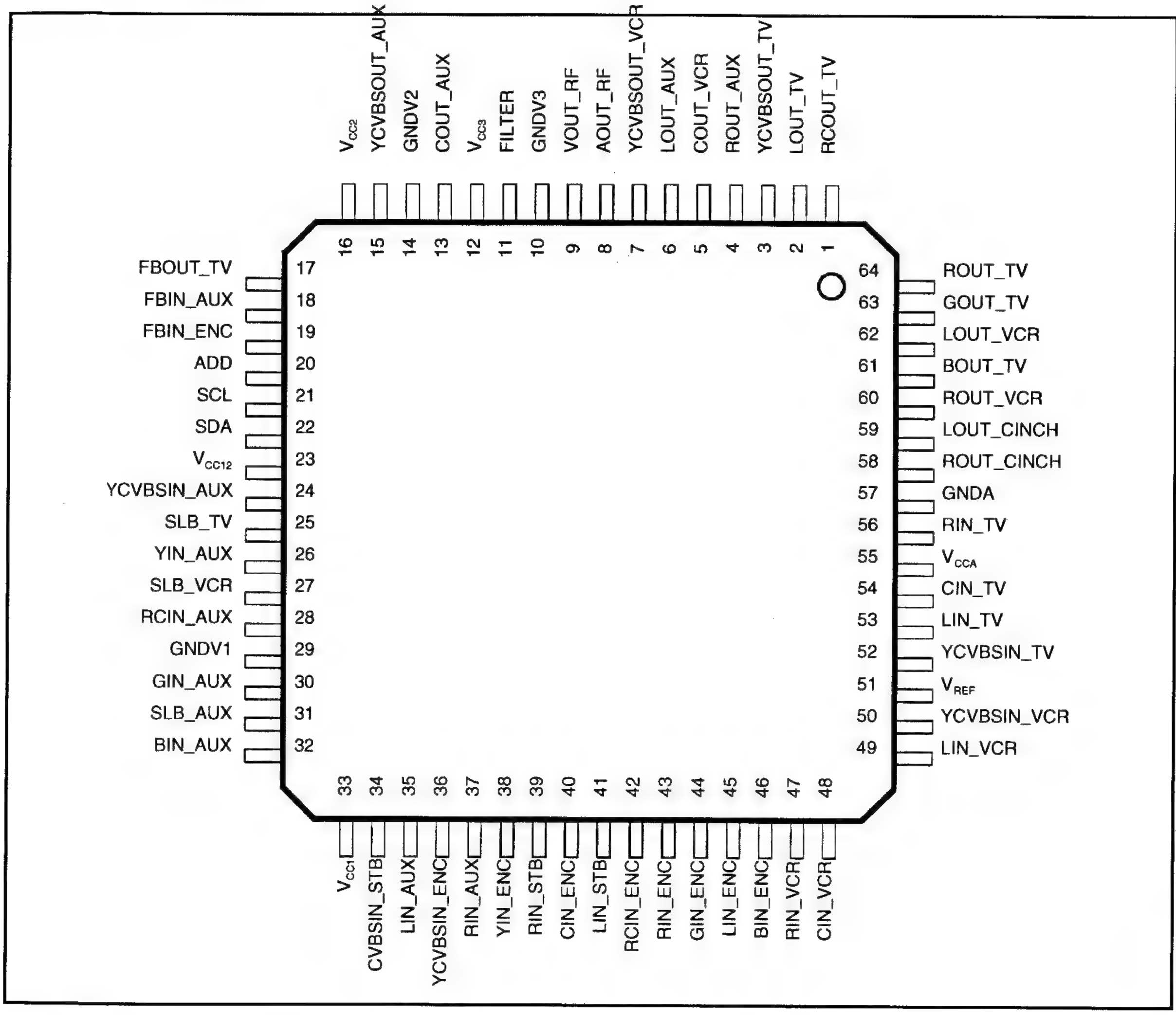
ORDER CODE : STV6410D

DESCRIPTION

The STV6410 is a highly integrated I²C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. It provides all the audio and video routings required in a full three scart set-top box design. It is also fully pin compatible with STV6411, the two scart version.

STV6410

PIN CONNECTIONS



6410-01.EPS

PIN LIST

Pin Number	Symbol	Description
1	RCOUT_TV	Red/chroma Output, to TV Scart
2	LOUT_TV	Audio Left Output, to TV Scart
3	YCVBSOUT_TV	Y/CVBS Output, to TV scart
4	ROUT_AUX	Audio Right Output, to AUX Scart
5	COUT_VCR	Chroma Output, to VCR Scart
6	LOUT_AUX	Audio Left Output, to AUX Scart
7	YCVBSOUT_VCR	Y/CVBS Output, to VCR Scart
8	AOUT_RF	Audio (L+R) Output to RF Modulator
9	VOUT_RF	Video (CVBS) Output to RF Modulator
10	GNDV3	Video Switches Ground 3
11	FILTER	Chroma Trap Filter
12	V_{CCV3}	Video Switches Supply 3 (8V)
13	COUT_AUX	Chroma Output, to AUX Scart
14	GNDV2	Video Switches Ground 2
15	YCVBSOUT_AUX	Y/CVBS Output, to AUX Scart

6410-01.TBL

STV6410

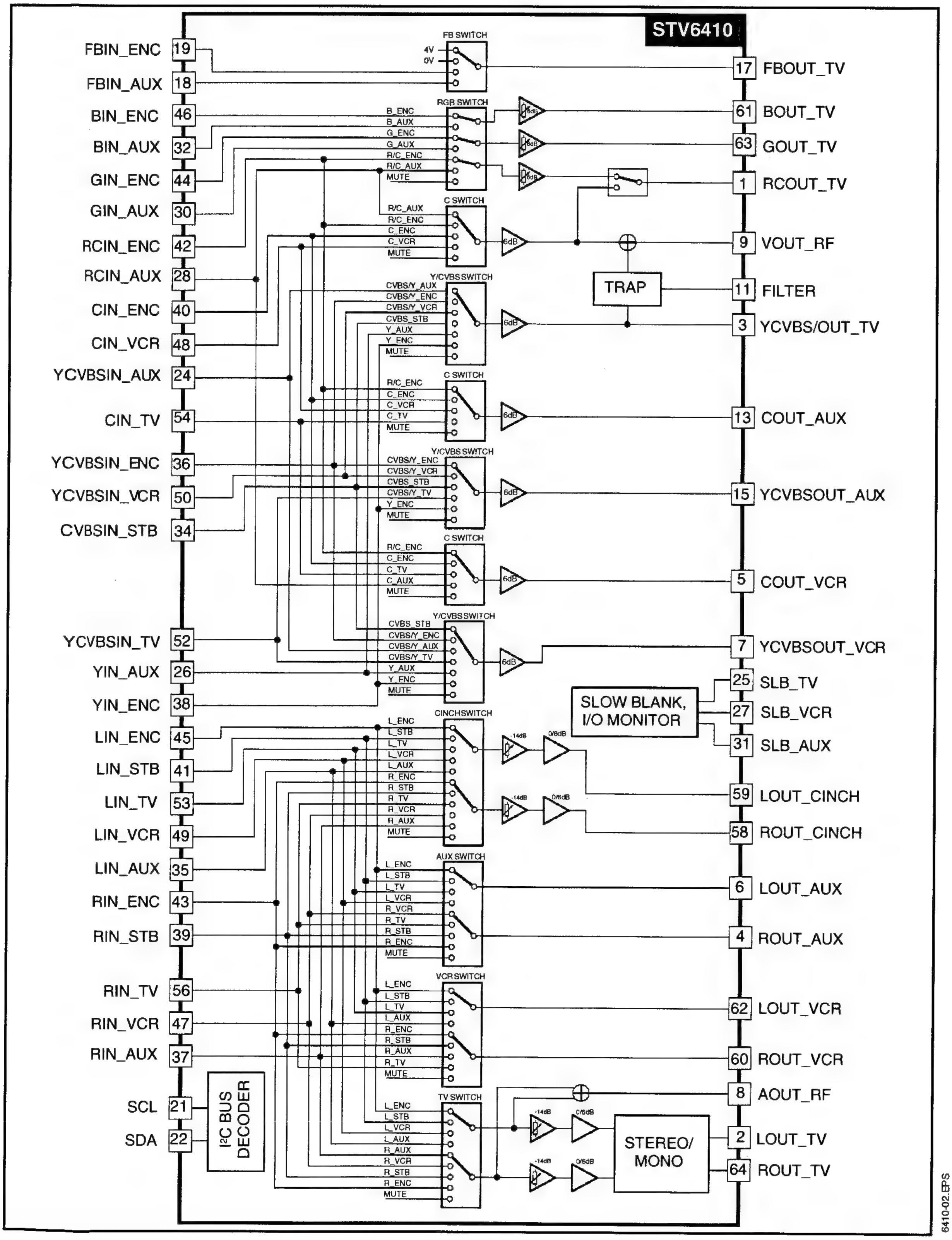
PIN LIST (continued)

Pin Number	Symbol	Description
16	V_{CCV2}	Video Switches Supply 2 (8V)
17	FBOUT_TV	Fast Blanking Output, to TV Scart
18	FBIN_AUX	Fast Blanking Input, from AUX Scart
19	FBIN_ENC	Fast Blanking Input, from Encoder
20	ADD	I2C Bus IC Address Programmation
21	SCL	I2C Bus Clock
22	SDA	I2C Bus Data
23	V_{CC12}	Slow Blanking Power Supply (12V)
24	YCVBSIN_AUX	Y/CVBS Input from AUX Scart
25	SLB_TV	Slow Blanking Input/Ouput from TV
26	YIN_AUX	Y Input, from AUX Scart
27	SLB_VCR	Slow Blanking Input/Ouput from VCR
28	RCIN_AUX	Red/Chroma Input, from AUX Scart
29	GNDV1	Video Switches Ground 1
30	GIN_AUX	Green Input, from AUX Scart
31	SLB_AUX	Slow Blanking Input/Ouput from AUX
32	BIN_AUX	Blue Input, from AUX Scart
33	V_{CCV1}	Video Switches Supply 1 (8V)
34	CVBSIN_STB	CVBS Input from STB
35	LIN_AUX	Audio Left Input, from AUX Scart
36	YCVBSIN_ENC	Y/CVBS Input from Encoder
37	RIN_AUX	Audio Right Input, from AUX Scart
38	YIN_ENC	Y Input, from Encoder
39	RIN_STB	Audio Right Input, from STB
40	CIN_ENC	Chroma Input, from Encoder
41	LIN_STB	Audio Left Input, from STB
42	RCIN_ENC	Red/Chroma Input, from Encoder
43	RIN_ENC	Audio Right Input, from Encoder
44	GIN_ENC	Green Input, from Encoder
45	LIN_ENC	Audio Left Input, from Encoder
46	BIN_ENC	Blue Input, from Encoder
47	RIN_VCR	Audio Right Input, from VCR Scart
48	CIN_VCR	Chroma Input, from VCR Scart
49	LIN_VCR	Audio Left Input, from VCR
50	YCVBSIN_VCR	Y/CVBS Input from VCR Scart
51	V_{REF}	Voltage Reference Decoupling
52	YCVBSIN_TV	Y/CVBS Input, from TV Scart
53	LIN_TV	Audio Left Input, from TV Scart
54	CIN_TV	Chroma Input, from TV Scart
55	V_{CCA}	Audio Switches Supply (8V)
56	RIN_TV	Audio right input, from TV Scart
57	GNDA	Audio Switches Ground
58	ROUT_CINCH	Audio Right Output, to CINCH
59	LOUT_CINCH	Audio Left Output, to CINCH
60	ROUT_VCR	Audio Right Output, to VCR sCart
61	BOUT_TV	Blue Output, to TV Scart
62	LOUT_VCR	Audio Left Output, to VCR Scart
63	GOUT_TV	Green Output, to TV Scart
64	ROUT_TV	Audio Right Output, to TV Scart

6410-01.TBL

STV6410

BLOCK DIAGRAM



9.8.5 IC7600: MSP3415D

Multistandard Sound Processor Family

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 34x5G version B8 and following versions.

1. Introduction

The MSP 34x5G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed in a single chip. Figure 1–1 shows a simplified functional block diagram of the MSP 34x5G.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM-Stereo-Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x5G has optimum stereo performance without any adjustments.

All MSP 34xxG versions are pin compatible to the MSP 34xxD. Only minor modifications are necessary to adapt a MSP 34xxD controlling software to the MSP 34xxG. The MSP 34x5G further simplifies controlling software. Standard selection requires a single I^2C transmission only.

Note: The MSP 34x5G version has reduced control registers and less functional pins. The remaining registers are software-compatible to the MSP 34x0G. The pinning is compatible to the MSP 34x0G.

The MSP 34x5G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I^2C interaction is necessary (Automatic Sound Selection).

The MSP 34x5G can handle very high FM deviations even in conjunction with NICAM processing. This is especially important for the introduction of NICAM in China.

The ICs are produced in submicron CMOS technology. The MSP 34x5G is available in the following packages: PSDIP64, PSDIP52, PMQFP44, PLQFP64, and PQFP80.

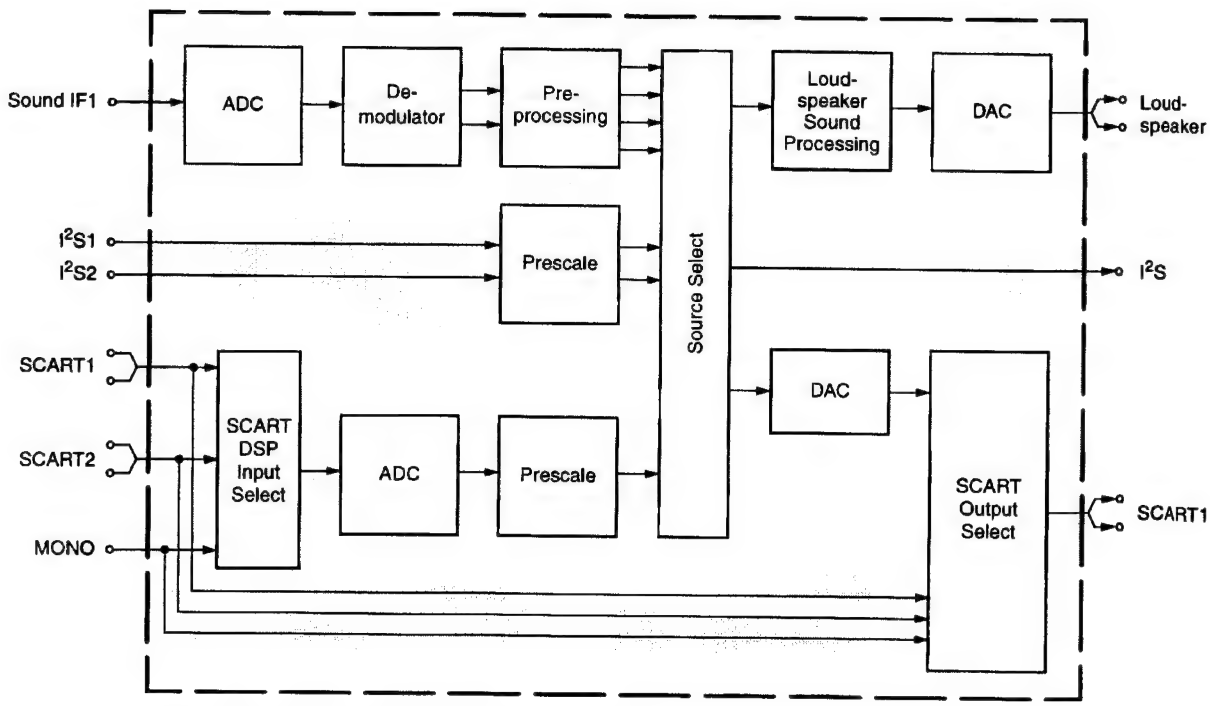


Fig. 1–1: Simplified functional block diagram of MSP 34x5G

2. Functional Description

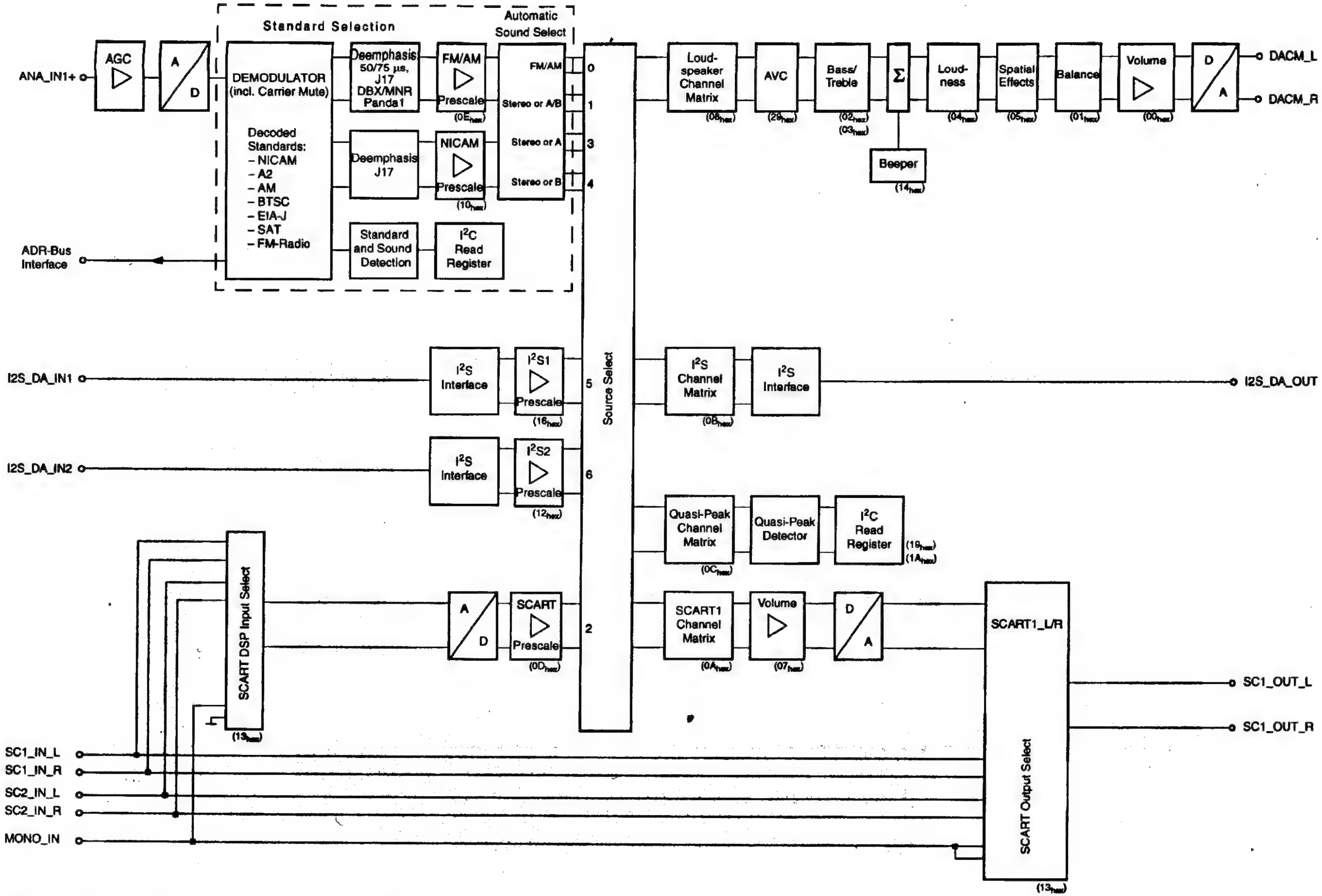


Fig. 2–1: Signal flow block diagram of the MSP 34x5G (input and output names correspond to pin names).

2.1. Architecture of the MSP 34x5G Family

Fig. 2–1 on page 8 shows a simplified block diagram of the IC. The block diagram contains all features of the MSP 3455G. Other members of the MSP 34x5G family do not have the complete set of features: The demodulator handles only a subset of the standards presented in the demodulator block; NICAM processing is only possible in the MSP 3415G and MSP 3455G (see dashed block in Fig. 2–1).

2.2. Sound IF Processing

2.2.1. Analog Sound IF Input

The input pins ANA_IN1+ and ANA_IN– offer the possibility to connect sound IF (SIF) sources to the MSP 34x5G. The analog-to-digital conversion of the preselected sound IF signal is done by an A/D-converter. An analog automatic gain circuit (AGC) allows a wide range of input levels. The high-pass filter formed by the coupling capacitor at pin ANA_IN1+ (see Section 7. "Appendix D: Application Information" on page 92) is sufficient in most cases to suppress video components. Some combinations of SAW filters and sound IF mixer ICs, however, show large picture components on their outputs. In this case, further filtering is recommended.

2.2.2. Demodulator: Standards and Features

The MSP 34x5G is able to demodulate all TV sound standards worldwide including the digital NICAM system. Depending on the MSP 34x5G version, the following demodulation modes can be performed:

A2-Systems: Detection and demodulation of two separate FM carriers (FM1 and FM2), demodulation and evaluation of the identification signal of carrier FM2.

NICAM-Systems: Demodulation and decoding of the NICAM carrier, detection and demodulation of the analog (FM or AM) carrier. For D/K-NICAM, the FM carrier may have a maximum deviation of 384 kHz.

Very high deviation FM-Mono: Detection and robust demodulation of one FM carrier with a maximum deviation of 540 kHz.

BTSC-Stereo: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, AM demodulation of the (L-R)-carrier and detection of the SAP subcarrier. Processing of the DBX noise reduction or Micronas Noise Reduction (MNR).

BTSC-Mono + SAP: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, detection and FM demodulation of the SAP-subcarrier. Processing of the DBX noise reduction or Micronas Noise Reduction (MNR).

Japan Stereo: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Demodulation and evaluation of the identification signal and FM demodulation of the (L-R)-carrier.

FM-Satellite Sound: Demodulation of one or two FM carriers. Processing of high-deviation mono or narrow bandwidth mono, stereo, or bilingual satellite sound according to the ASTRA specification.

FM-Stereo-Radio: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Detection and evaluation of the pilot carrier and AM demodulation of the (L-R)-carrier.

The demodulator blocks of all MSP 34x5G versions have identical user interfaces. Even completely different systems like the BTSC and NICAM systems are controlled the same way. Standards are selected by means of MSP Standard Codes. Automatic processes handle standard detection and identification without controller interaction. The key features of the MSP 34x5G demodulator blocks are

Standard Selection: The controlling of the demodulator is minimized: All parameters, such as tuning frequencies or filter bandwidth, are adjusted automatically by transmitting one single value to the STANDARD SELECT register. For all standards, specific MSP standard codes are defined.

Automatic Standard Detection: If the TV sound standard is unknown, the MSP 34x5G can automatically detect the actual standard, switch to that standard, and respond the actual MSP standard code.

Automatic Carrier Mute: To prevent noise effects or FM identification problems in the absence of an FM carrier, the MSP 34x5G offers a configurable carrier mute feature, which is activated automatically if the TV sound standard is selected by means of the STANDARD SELECT register. If no FM carrier is detected at one of the two MSP demodulator channels, the corresponding demodulator output is muted. This is indicated in the STATUS register.

2.2.3. Preprocessing of Demodulator Signals

The NICAM signals must be processed by a deemphasis filter and adjusted in level. The analog demodulated signals must be processed by a deemphasis filter, adjusted in level, and dematrixed. The correct deemphasis filters are already selected by setting the standard in the STANDARD SELECT register. The level adjustment has to be done by means of the FM/AM and NICAM prescale registers. The necessary dematrix function depends on the selected sound standard and the actual broadcasted sound mode (mono, stereo, or bilingual). It can be manually set by the FM Matrix Mode register or automatically by the Automatic Sound Selection.

2.2.4. Automatic Sound Select

In the Automatic Sound Select mode, the dematrix function is automatically selected based on the identification information in the STATUS register. No I^2C interaction is necessary when the broadcasted sound mode changes (e.g. from mono to stereo).

The demodulator supports the identification check by switching between mono-compatible standards (standards that have the same FM-Mono carrier) automatically and non-audible. If B/G-FM or B/G-NICAM is selected, the MSP will switch between these standards. The same action is performed for the standards: D/K1-FM, D/K2-FM, and D/K-NICAM. Switching is only done in the absence of any stereo or bilingual identification. If identification is found, the MSP keeps the detected standard.

In case of high bit-error rates, the MSP 34x5G automatically falls back from digital NICAM sound to analog FM or AM mono.

Table 2-1 summarizes all actions that take place when Automatic Sound Select is switched on.

To provide more flexibility, the Automatic Sound Select block prepares four different source channels of demodulated sound (Fig. 2-2). By choosing one of the four demodulator channels, the preferred sound mode can be selected for each of the output channels (loudspeaker, headphone, etc.). This is done by means of the Source Select registers.

The following source channels of demodulated sound are defined:

- **"FM/AM" channel:** Analog mono sound, stereo if available. In case of NICAM, analog mono only (FM or AM mono).
- **"Stereo or A/B" channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains both languages A (left) and B (right).
- **"Stereo or A" channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language A (on left and right).
- **"Stereo or B" channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language B (on left and right).

Fig. 2-2 and Table 2-2 show the source channel assignment of the demodulated signals in case of Automatic Sound Select mode for all sound standards.

Note: The analog primary input channel contains the signal of the mono FM/AM carrier or the L+R signal of the MPX carrier. The secondary input channel contains the signal of the 2nd FM carrier, the L-R signal of the MPX carrier, or the SAP signal.

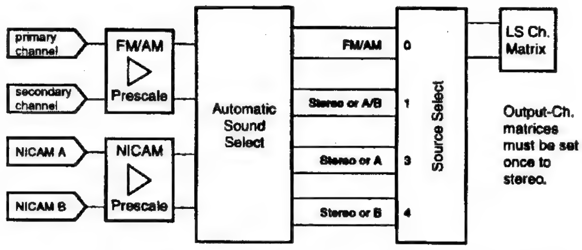


Fig. 2-2: Source channel assignment of demodulated signals in Automatic Sound Select Mode

2.2.5. Manual Mode

Fig. 2-3 shows the source channel assignment of demodulated signals in case of manual mode. If manual mode is required, more information can be found in Section 6.7. "Demodulator Source Channels in Manual Mode" on page 90.

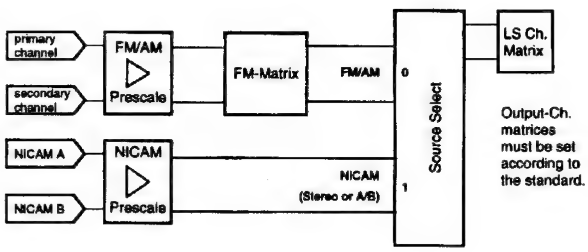


Fig. 2-3: Source channel assignment of demodulated signals in Manual Mode

2.3. Preprocessing for SCART and I^2S Input Signals

The SCART and I^2S inputs need only be adjusted in level by means of the SCART and I^2S prescale registers.

2.4. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (one of the demodulator source channels or SCART) to the desired output channels (loudspeaker, etc.). All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the sound mode can be set to sound A, sound B, stereo, or mono by means of the output channel matrix.

If Automatic Sound Select is on, the output channel matrix can stay fixed to stereo (transparent) for demodulated signals.

2.5. Audio Baseband Processing

2.5.1. Automatic Volume Correction (AVC)

Different sound sources (e.g. terrestrial channels, SAT channels, or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The AVC solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see page 30).

For input signals ranging from –24 dBr to 0 dBr, the AVC maintains a fixed output level of –18 dBr. Fig. 2–4 shows the AVC output level versus its input level. For prescale and volume registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output. This is

– SCART input/output 0 dBr = 2.0 V_{rms}

– Loudspeaker output 0 dBr = 1.4 V_{rms}

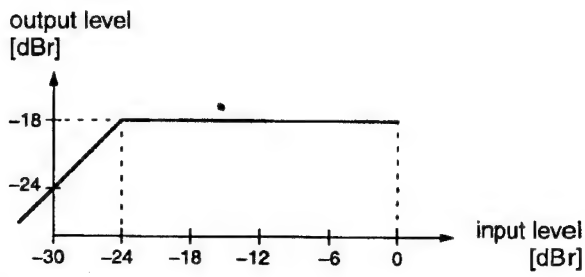


Fig. 2–4: Simplified AVC characteristics

2.5.2. Loudspeaker Outputs

The following baseband features are implemented in the loudspeaker output channels: bass/treble, loudness, balance, and volume. A square wave beeper can be added to the loudspeaker channel.

2.5.3. Quasi-Peak Detector

The quasi-peak readout register can be used to read out the quasi-peak level of any input source. The feature is based on following filter time constants:

attack time: 1.3 ms
decay time: 37 ms

2.6. SCART Signal Routing

2.6.1. SCART DSP In and SCART Out Select

The SCART DSP Input Select and SCART Output Select blocks include full matrix switching facilities. To design a TV set with two pairs of SCART-inputs and one pair of SCART-outputs, no external switching hardware is required. The switches are controlled by the ACB user register (see page 34).

2.6.2. Stand-by Mode

If the MSP 34x5G is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off DVSUP and AVSUP, but keeping AHVSUP (**'Stand-by'-mode**), the SCART switches maintain their position and function. This allows the copying from selected SCART-inputs to SCART-outputs in the TV set's stand-by mode.

In case of power on or starting from stand-by (switching on the DVSUP and AVSUP, RESETQ going high 2 ms later), all internal registers except the ACB register (page 34) are reset to the default configuration (see Table 3–5 on page 18). The reset position of the ACB register becomes active after the first I^2C transmission into the Baseband Processing part. By transmitting the ACB register first, the reset state can be redefined.

2.7. I^2S Bus Interface

The MSP 34x5G has a synchronous master/slave input/output interface running on 32 kHz.

The interface accepts two formats:

1. I^2S_WS changes at the word boundary
2. I^2S_WS changes one I^2S-clock period before the word boundaries.

All I^2S options are set by means of the MODUS and the I2S_CONFIG registers.

The I^2S bus interface consists of five pins:

- I2S_DA_IN1, I2S_DA_IN2:
  I^2S serial data input: 16, 18....32 bits per sample
- I2S_DA_OUT:
  I^2S serial data output: 16, 18...32 bits per sample
- I2S_CL:
  I^2S serial clock
- I2S_WS:
  I^2S word strobe signal defines the left and right sample

If the MSP 34x5G serves as the master on the I^2S interface, the clock and word strobe lines are driven by the IC. In this mode, only 16 or 32 bits per sample can be selected. In slave mode, these lines are input to the IC and the MSP clock is synchronized to 576 times the I2S_WS rate (32 kHz). NICAM operation is not possible in slave mode.

An I^2S timing diagram is shown in Fig. 4–28 on page 62.

2.8. ADR Bus Interface

For the ASTRA Digital Radio System (ADR), the MSP 3405G, MSP 3415G, and MSP 3455G performs preprocessing such as carrier selection and filtering. Via the 3-line ADR-bus, the resulting signals are transferred to the DRP 3510A coprocessor, where the source decoding is performed. To be prepared for an upgrade to ADR with an additional DRP board, the following lines of MSP 34x5G should be provided on a feature connector:

- I2S_DA_IN1 or I2S_DA_IN2
- I2S_DA_OUT
- I2S_WS
- I2S_CL
- ADR_CL, ADR_WS, ADR_DA

For more details, please refer to the DRP 3510A data sheet.

2.9. Digital Control I/O Pins and Status Change Indication

The static level of the digital input/output pins D_CTR_I/O_0/1 is switchable between HIGH and LOW via the I^2C-bus by means of the ACB register (see page 34). This enables the controlling of external hardware switches or other devices via I^2C-bus.

The digital input/output pins can be set to high impedance by means of the MODUS register (see page 23). In this mode, the pins can be used as input. The current state can be read out of the STATUS register (see page 25).

Optionally, the pin D_CTR_I/O_1 can be used as an interrupt request signal to the controller, indicating any changes in the read register STATUS. This makes polling unnecessary; I^2C-bus interactions are reduced to a minimum (see STATUS register on page 25 and MODUS register on page 23).

2.10. Clock PLL Oscillator and Crystal Specifications

The MSP 34x5G derives all internal system clocks from the 18.432 MHz oscillator. In NICAM or in I^2S-Slave mode, the clock is phase-locked to the corresponding source. Therefore, it is not possible to use NICAM and I^2S-Slave mode at the same time.

For proper performance, the MSP clock oscillator requires a 18.432-MHz crystal. Note, that for the phase-locked mode (NICAM, I^2S slave), crystals with tighter tolerance are required.

4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
DVSS: if not used, connect to DVSS
X = obligatory; connect as described in circuit diagram
AHVSS: connect to AHVSS

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PQFP 80-pin	PLQFP 64-pin	PMQFP 44-pin	PSDIP 64-pin	PSDIP 52-pin				
1	64	–	8	–	NC		LV	Not connected
2	1	12	9	7	I2C_CL	IN/OUT	X	I^2C clock
3	2	13	10	8	I2C_DA	IN/OUT	X	I^2C data
4	3	14	11	9	I2S_CL		LV	I^2S clock
5	4	15	12	10	I2S_WS		LV	I^2S word strobe
6	5	16	13	11	I2S_DA_OUT		LV	I^2S data output
7	6	17	14	12	I2S_DA_IN1		LV	I^2S1 data input
8	7	–	15	13	ADR_DA		LV	ADR data output
9	8	–	16	14	ADR_WS		LV	ADR word strobe
10	9	18	17	15	ADR_CL		LV	ADR clock
11	–	–	–	–	DVSUP		X	Digital power supply +5 V
12	–	–	–	–	DVSUP		X	Digital power supply +5 V
13	10	19	18	16	DVSUP		X	Digital power supply +5 V
14	–	20	–	–	DVSS		X	Digital ground
15	–	–	–	–	DVSS		X	Digital ground
16	11	–	19	17	DVSS		X	Digital ground
17	12	21	20	18	I2S_DA_IN2		LV	I^2S2-data input
18	13	–	21	19	NC		LV	Not connected
19	14	–	22	–	NC		LV	Not connected
20	15	–	23	–	NC		LV	Not connected
21	16	22	24	20	RESETQ	IN	X	Power-on-reset
22	–	–	–	–	NC		LV	Not connected
23	–	–	–	–	NC		LV	Not connected
24	17	23	25	21	NC		LV	Not connected
25	18	24	26	22	NC		LV	Not connected

Pin No. PQFP 80-pin	PLQFP 64-pin	PMQFP 44-pin	PSDIP 64-pin	PSDIP 52-pin	Pin Name	Type	Connection (if not used)	Short Description
26	19	25	27	23	VREF2		X	Reference ground 2 high-voltage part
27	20	26	28	24	DACM_R	OUT	LV	Loudspeaker out, right
28	21	27	29	25	DACM_L	OUT	LV	Loudspeaker out, left
29	22	–	30	–	NC		LV	Not connected
30	23	–	31	26	NC		LV	Not connected
31	24	–	32	–	NC		LV	Not connected
32	–	–	–	–	NC		LV	Not connected
33	25	–	33	27	NC		LV	Not connected
34	26	28	34	28	NC		LV	Not connected
35	27	29	35	29	VREF1		X	Reference ground 1 high-voltage part
36	28	30	36	30	SC1_OUT_R	OUT	LV	SCART 1 output, right
37	29	31	37	31	SC1_OUT_L	OUT	LV	SCART 1 output, left
38	30	32	38	32	NC		LV	Not connected
39	31	33	39	33	AHVSUP		X	Analog power supply 8.0 V
40	32	34	40	34	CAPL_M		X	Volume capacitor MAIN
41	–	–	–	–	NC		LV	Not connected
42	–	–	–	–	NC		LV	Not connected
43	–	–	–	–	AHVSS		X	Analog ground
44	33	35	41	35	AHVSS		X	Analog ground
45	34	36	42	36	AGNDC		X	Analog reference voltage high-voltage part
46	–	–	–	–	NC		LV	Not connected
47	35	–	43	–	NC		LV	Not connected
48	36	–	44	–	NC		LV	Not connected
49	37	–	45	–	NC		LV	Not connected
50	38	–	46	37	NC		LV	Not connected
51	39	–	47	38	NC		LV	Not connected
52	40	–	48	–	NC		AHVSS	Analog Shield Ground
53	41	37	49	39	SC2_IN_L	IN	LV	SCART 2 input, left
54	42	38	50	40	SC2_IN_R	IN	LV	SCART 2 input, right

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PQFP 80-pin	PLQFP 64-pin	PMQFP 44-pin	PSDIP 64-pin	PSDIP 52-pin				
55	43	39	51	–	ASG		AHVSS	Analog Shield Ground
56	44	40	52	41	SC1_IN_L	IN	LV	SCART 1 input, left
57	45	41	53	42	SC1_IN_R	IN	LV	SCART 1 input, right
58	46	42	54	43	VREFTOP		X	Reference voltage IF A/D converter
59	–	–	–	–	NC		LV	Not connected
60	47	43	55	44	MONO_IN	IN	LV	Mono input
61	–	–	–	–	AVSS		X	Analog ground
62	48	44	56	45	AVSS		X	Analog ground
63	–	–	–	–	NC		LV	Not connected
64	–	–	–	–	NC		LV	Not connected
65	–	–	–	–	AVSUP		X	Analog power supply +5 V
66	49	1	57	46	AVSUP		X	Analog power supply +5 V
67	50	2	58	47	ANA_IN1+	IN	LV	IF input 1
68	51	3	59	48	ANA_IN–	IN	LV	IF common
69	52	–	60	49	NC		LV	Not connected
70	53	4	61	50	TESTEN	IN	X	Test pin
71	54	5	62	51	XTAL_IN	IN	X	Crystal oscillator
72	55	6	63	52	XTAL_OUT	OUT	X	Crystal oscillator
73	56	7	64	1	TP		LV	Test pin
74	57	–	1	2	NC		LV	Not connected
75	58	–	2	–	NC		LV	Not connected
76	59	–	3	–	NC		LV	Not connected
77	60	8	4	3	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
78	61	9	5	4	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
79	62	10	6	5	ADR_SEL	IN	X	I^2C Bus address select
80	63	11	7	6	STANDBYQ	IN	X	Standby (low-active)

9.8.6 IC7703: TDA9818

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

FEATURES

- 5 V supply voltage
- Applicable for IFs (Intermediate Frequencies) of 38.9 MHz, 45.75 MHz and 58.75 MHz
- Gain controlled wide band Video IF (VIF)-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Robustness for over-modulation better than 105% due to gated phase detector at L/L accent standard and PLL-bandwidth control at negative modulated standards
- VCO (Voltage Controlled Oscillator) frequency switchable between L and L accent (alignment external) picture carrier frequency
- VIF AGC (Automatic Gain Control) detector for gain control, operating as peak sync detector for B/G, peak white detector for L; signal controlled reaction time for L
- Tuner AGC with adjustable TakeOver Point (TOP)
- AFC (Automatic Frequency Control) detector without extra reference circuit
- AC-coupled limiter amplifier for sound intercarrier signal
- Alignment-free FM PLL (Phase Locked Loop) demodulator with high linearity
- SIF (Sound IF) input for single reference QSS (Quasi Split Sound) mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode
- AM demodulator without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- ESD (Electrostatic Discharge) protection for all pins.

GENERAL DESCRIPTION

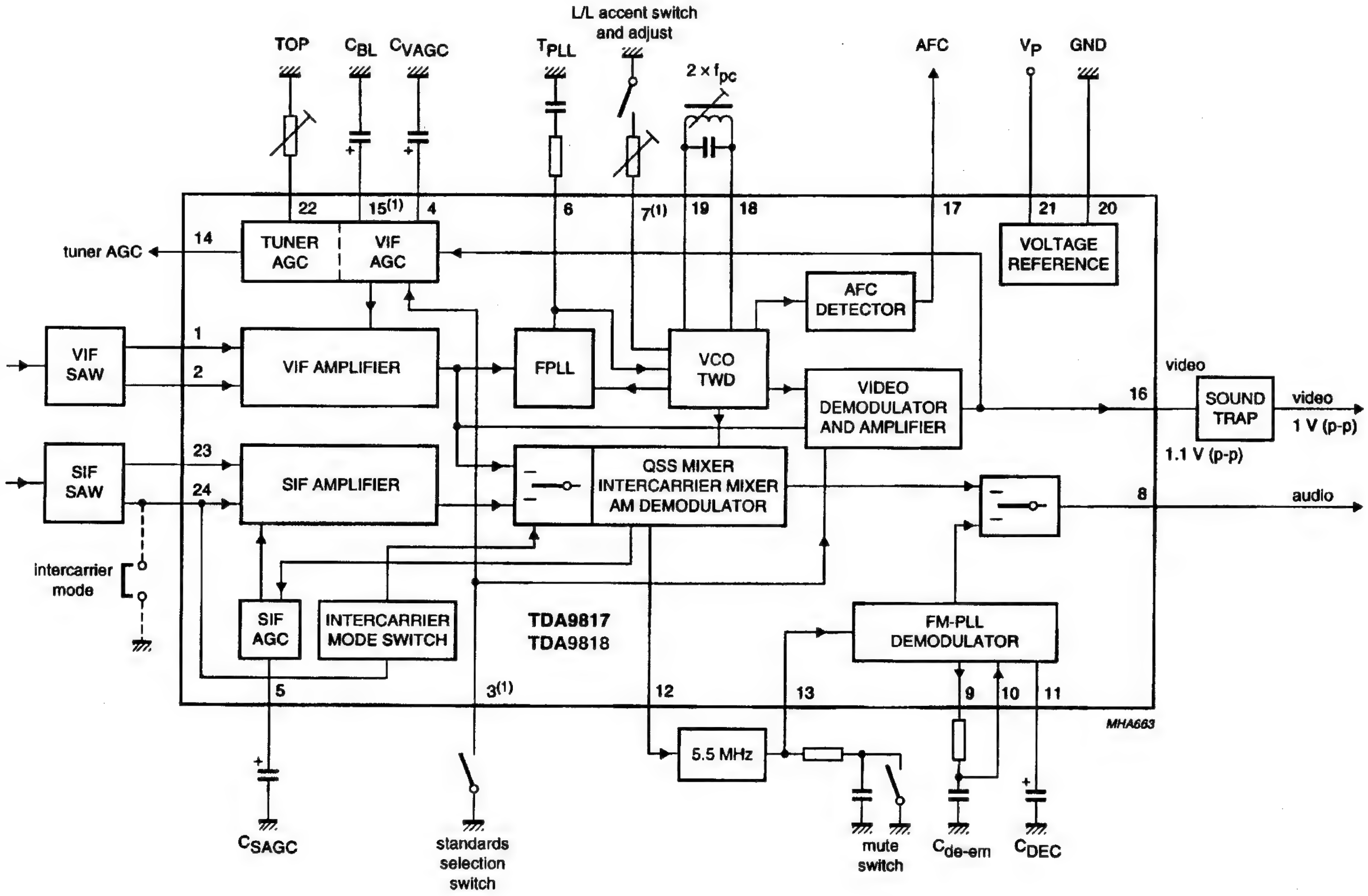
The TDA9817 is an integrated circuit for single standard vision IF signal processing and FM demodulation.

The TDA9818 is an integrated circuit for multistandard vision IF signal processing, sound AM and FM demodulation.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9817	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
TDA9818	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1

BLOCK DIAGRAM



(1) Not connected for TDA9817.

Fig.1 Block diagram.

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

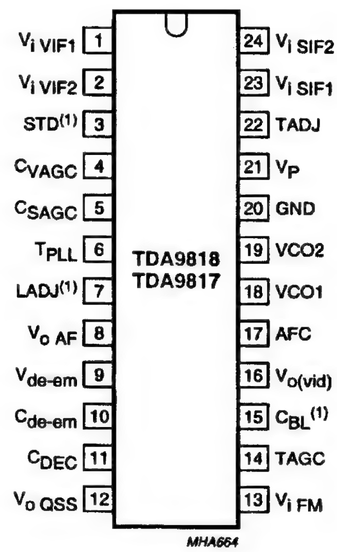
TDA9817; TDA9818

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF1}$	1	VIF differential input signal voltage 1
$V_{i\ VIF2}$	2	VIF differential input signal voltage 2
STD(1)	3	standard switch
C_{VAGC}	4	VIF AGC capacitor
C_{SAGC}	5	SIF AGC capacitor
T_{PLL}	6	PLL loop filter
LADJ(1)	7	L/L accent switch and adjust
$V_{o\ AF}$	8	audio output
$V_{de\text{-}em}$	9	de-emphasis input
$C_{de\text{-}em}$	10	de-emphasis output
C_{DEC}	11	decoupling capacitor
$V_{o\ QSS}$	12	single reference QSS/intercarrier output voltage
$V_{i\ FM}$	13	sound intercarrier input voltage
TAGC	14	tuner AGC output
C_{BL}(1)	15	black level detector
$V_{o(vid)}$	16	composite video output voltage
AFC	17	AFC output
VCO1	18	VCO1 resonance circuit
VCO2	19	VCO2 resonance circuit
GND	20	ground
V_P	21	supply voltage
TADJ	22	tuner AGC takeover point adjust
$V_{i\ SIF1}$	23	SIF differential input signal voltage 1
$V_{i\ SIF2}$	24	SIF differential input signal voltage 2

Note

1. Not connected for TDA9817.



(1) Not connected for TDA9817.

Fig.2 Pin configuration.

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

FUNCTIONAL DESCRIPTION

The integrated circuit comprises the functional blocks as shown in Fig.1:

- Vision IF amplifier and VIF AGC detector
- Tuner AGC
- Frequency Phase Locked Loop detector (FPLL)
- VCO, Travelling Wave Divider (TWD) and AFC
- Video demodulator and amplifier
- SIF amplifier and SIF AGC
- Single reference QSS mixer
- AM demodulator
- FM-PLL demodulator
- AF (Audio Frequency) signal processing
- Internal voltage stabilizer.

Vision IF amplifier and VIF AGC detector

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration.

The AGC detector generates the required VIF gain control voltage for constant video output by charging/discharging the AGC capacitor. Therefore for negative video modulation the sync level and for positive video modulation the peak white level of the video signal is detected. In order to reduce the reaction time for positive modulation, where a very large time constant is needed, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step. The additional level information is given by the black-level detector voltage.

Tuner AGC

The AGC capacitor voltage is converted to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current at pin TAGC (open-collector output). The tuner AGC takeover point can be adjusted at pin TADJ. This allows to match the tuner to the SAW filter in order to achieve the optimum IF input level.

Frequency Phase Locked Loop detector (FPLL)

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. The DC current of either frequency detector or phase detector is converted into a DC voltage via the loop filter, which controls the VCO frequency. In the event of positive modulated signals the phase detector is gated by composite sync in order to avoid signal distortion for overmodulated VIF signals.

VCO, Travelling Wave Divider (TWD) and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated variable capacitors.
The control voltage required to tune the VCO from its free-running frequency to actually double the PC frequency is generated by the frequency-phase detector (FPLL) and fed via the loop filter to the first variable capacitor. This control voltage is amplified and additionally converted into a current which represents the AFC output signal. At centre frequency the AFC output current is equal to zero.

For TDA9818: the VCO centre frequency can be decreased (required for L accent standard) by activating an additional internal capacitor. This is achieved by using the L accent switch. In this event the second variable capacitor can be controlled by a variable resistor at the L accent switch for setting the VCO centre frequency to the required L accent value.

The oscillator signal is divided by 2 with a TWD which generates two differential output signals with a 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the 'in phase' signal of the travelling wave divider output. In the demodulator stage the video signal polarity can be switched in accordance with the TV standard.

The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics for B/G and L standard. The standard dependent level shift in this stage delivers the same sync level for positive and negative modulation. The video output signal at $V_{o(vid)}$ is 1.1 V (p-p) for nominal vision IF modulation, in order to achieve 1 V (p-p) at sound trap output.

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

SIF amplifier and SIF AGC

The sound IF amplifier consists of two AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.

The SIF AGC detector is related to the SIF input signal (average level of AM or FM carrier) and controls the SIF amplifier to provide a constant SIF signal to the AM demodulator and single reference QSS mixer. At L standard (AM sound) the SIF AGC reaction time is set to 'slow' for nominal video conditions. But with a decreasing VIF amplitude step the SIF AGC is set to 'fast' mode controlled by the VIF AGC detector. In FM mode this reaction time is always 'fast'.

Single reference QSS mixer

The single reference QSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass for attenuation of the video signal components to the output pin 12. With this system a high performance hi-fi stereo sound processing can be achieved.

For a simplified application without a sound IF SAW filter the single reference QSS mixer can be switched to the intercarrier mode by connecting pin 24 to ground. In this mode the sound IF passes the vision IF SAW filter and the composite IF signal is fed to the single reference QSS mixer. This IF signal is multiplied with the 90 degree TWD output signal for converting the sound IF to intercarrier frequency. This composite intercarrier signal is fed to the output pin 12, too. By using this quadrature detection, the low frequency video signals are removed.

AM demodulator

The AM demodulator is realized by a multiplier. The modulated SIF amplifier output signal is multiplied in phase with the limited (AM is removed) SIF amplifier output signal. The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the AF amplifier.

FM-PLL demodulator

The FM-PLL demodulator consists of a limiter and an FM-PLL. The limiter provides the amplification and limitation of the FM sound intercarrier signal. The result is high sensitivity and AM suppression. The amplifier consists of 7 stages which are internally AC-coupled in order to minimize the DC offset.

Furthermore the AF output signal can be muted by connecting a resistor between the limiter input pin 13 and ground.

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. The FM-PLL operates as an FM demodulator.

AF signal processing

The AF amplifier consists of two parts:

1. The AF pre-amplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal pin 9 at which the de-emphasis network for FM sound is applied. An additional DC control circuit is implemented to keep the DC level constant, independent of process spread.
2. The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to AM, FM de-emphasis or mute state, controlled by the standard switching voltage and the mute switching voltage.

Internal voltage stabilizer

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

9.8.7 IC7803: TMP93C071

CMOS 16-Bit Microcontroller
TMP93C071F

1. Outline and Feature

TMP93C071F is a high-speed advanced 16-bit microcontroller developed for application with VCR system control, software servo motor control and timer control.

In addition to basics such as I/O ports, the TMP93C071F has high-speed/high-precision signal measuring circuit, PWM (Pulse-Width-Modulator) and high-precision real timing pulse generator.

The device characteristics are as follows:

(1) Original 16-bit CPU (900L_CPU)
- TLCS-90 instruction mnemonic upward compatible
- 16 Mbyte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication/division and bit transfer/arithmetic instructions
- High-speed micro DMA: 4 channels (1.6 µs / 2 byte at 20 MHz)

(2) Minimum instruction execution time: 200 ns at 20 MHz
(3) Internal ROM: ROMless
(4) Internal RAM: 8 Kbyte
(5) External memory expansion
- Can be expanded up to 16 Mbyte (for both programs and data)
- AM8/16 pin (select the external data bus width)
- Can be mixed 8 and 16bit external data buses.
  ...Dynamic data bus sizing.

(6) 20-bit time-base-counter (TBC)
- free running counter
- accuracy: 100 ns (at 20 MHz)
- overflow: 105 ms (at 20 MHz)

(7) 8-bit timer (TC0): 1 channel
- for CTL linear time counter

(8) 16-bit timer (TC1-5): 5 channels
- C-sync count, capstan FG count, general: (3 channels)

(9) Timing pulse generator (TPG): 2 channels
- (16-bit timing data + 6-bit-output data) with 8-stages FIFO: 1 channel
- (16-bit timing data + 4-bit-output data): 1 channel
- accuracy: 400 ns (at 20 MHz)

(10) Pulse width modulation outputs (PWM)
- 14-bit PWM: 3 channels (for controlling capstan, drum and tuner)
- 8-bit PWM: 9 channels (for controlling volume)
- carrier frequency: 39.1 kHz (at 20 MHz)

980910EBP1

(11) 24-bit time base counter capture circuit (Capture 0)
- (18-bit timing data + 6-bit trigger data) with 8-stages FIFO: 1 channel
- capture input sources: Remote-control-input (RMTIN), V-sync, CTL, Drum-PG, general (1 channel)
- accuracy: 400 ns (at 20 MHz)

(12) 17-bit time base counter capture circuit (Capture 1/2)
- (16-bit timing data + 1-bit trigger data): 2 channel
- capture input sources: Drum-FG, Capstan-FG
- accuracy: 100 ns (at 20 MHz)

(13) VISS/VASS detection circuit (VISS/VASS)
- CTL duty detection
- VASS data 16-bit latch

(14) Composite-sync-signal (C-sync) input (C-sync In)
- Vertical-sync-signal (V-sync) separation (V-sepa)

(15) Head Amp switch/Color Rotary control (HA/CR)

(16) Pseudo-V/H generator (PV/PH)

(17) 8-bit A/D converter (ADC): 16 channels
- Conversion speed: 95states (9.5 µs at 20 MHz)

(18) Serial bus I/F
- 8-bit synchronous (SIO0, 1): 2 channels
- UART: 1 channel
- I^2CBUS: 1 channel/2 ports
  •••• Multi - Master function/Master transfer with micro DMA.

(19) Watch dog timer (WDT)

(20) Interrupt controller (INTC)
- CPU: 2 sources ••• SWI instruction, and illegal instruction
- Internal: 20 sources 7-level priority can be set.
- External: 5 sources

(21) I/O ports
- 57 I/O ports (multiplexed functional pins)
- 8 Input ports (P40/AIN3-P47/AIN10: These pins are used as analog input for A/D converter.)
- 4 Output ports (P24/A20-P27/A23: These pins are also used as address bus outputs.)

(22) Standby function: 4 halt modes (RUN, IDLE2, IDLE1, STOP)

(23) System clock function
- Dual clock operation 20 MHz (High-speed: normal)/32 kHz(Low-speed: slow)
  •••• 17-bit Real Time Counter built in

(24) Operating Voltage
- Vcc = 2.7 to 5.5 V (at 32 kHz)
- Vcc = 4.5 to 5.5 V (at 20 MHz)

(25) Package
- 120 pin QFP 28 mm × 28 mm (Pin pitch: 0.8 mm)
- Type name QFP120-P-2828-0.80A

Block Diagram of TMP93C071F

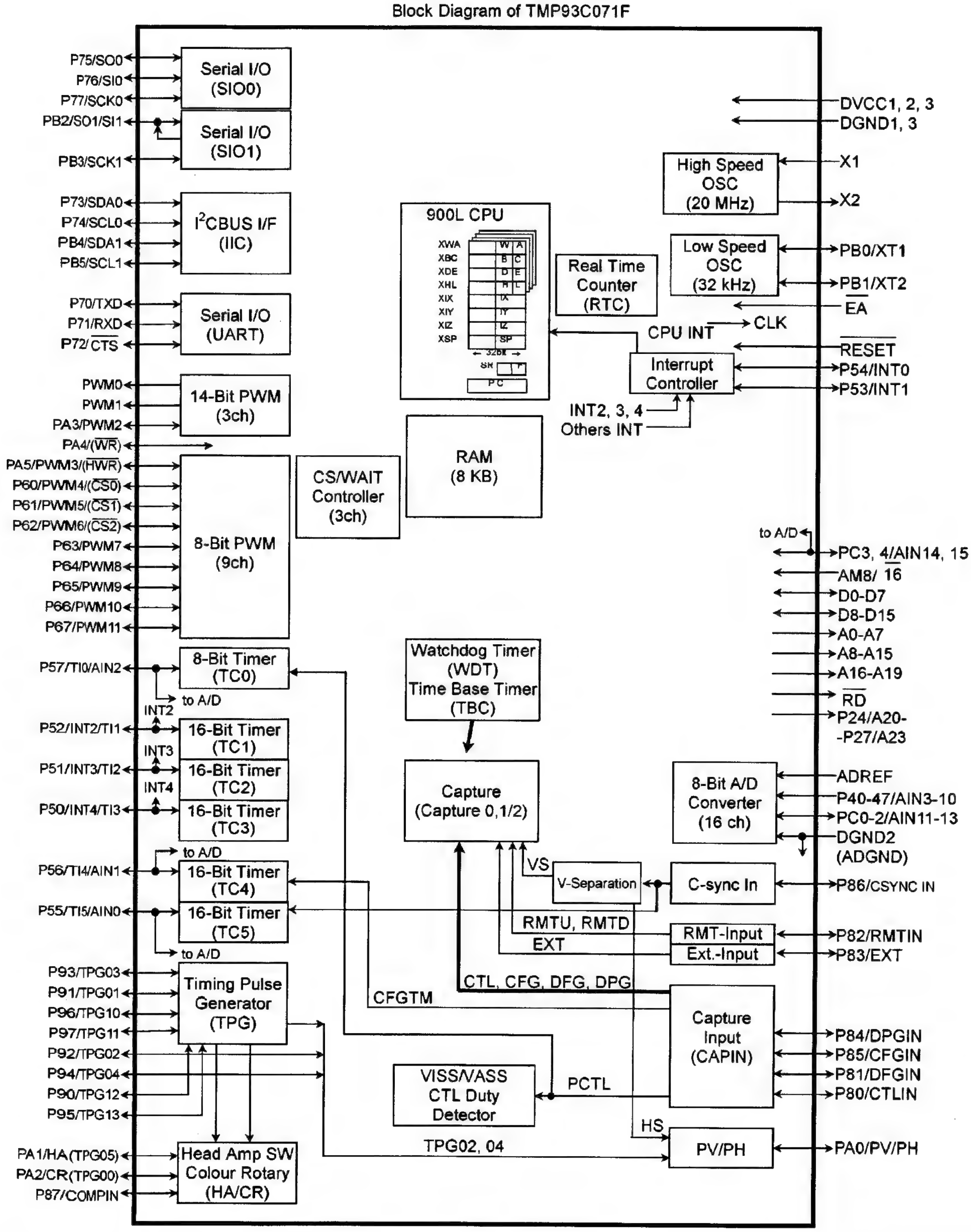


Figure 1 TMP93C071 Block Diagram

2. Pin Assignment And Functions

The assignment of input and output pins for the TMP93C071, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93C071.

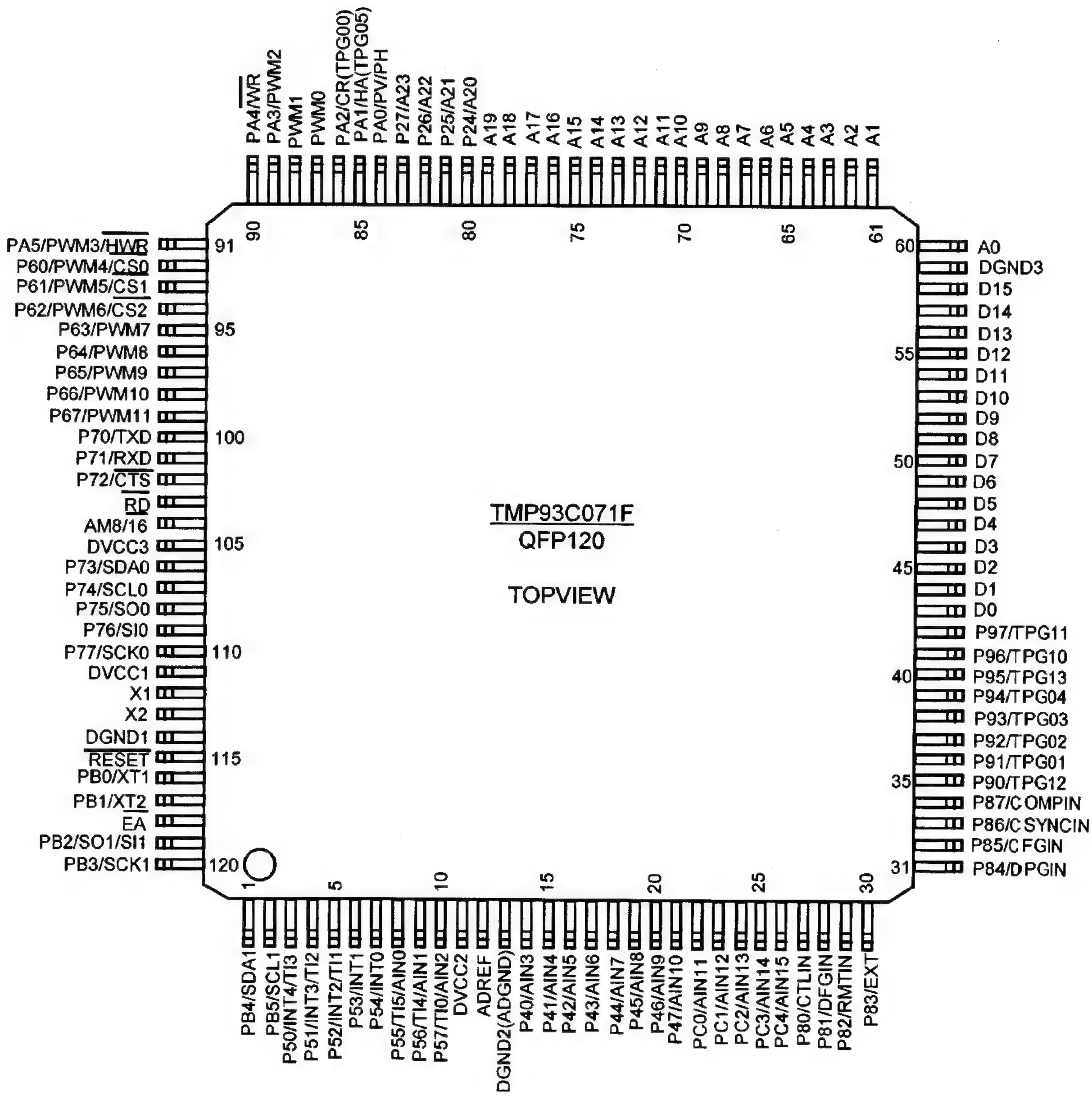


Figure 2.1.1 Pin Assignment (120-pin QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 Pin Names and Function (1/5)

Pin name	Number of pins	I/O	Functions
D0 to D15	16	I/O (3-state)	data: 0 to 15 for data bus
A0 to A19	20	Output	Address: 0 to 19 for address bus
A20 to A23/ P24 to P27	4	Output Output	Address: 20 to 23 for address bus Port 2: Output port
$\overline{\text{RD}}$	1	Output	Read: strobe signal for reading external memory
AM8/16	1	Input	data bus width select input (only 8 bit or 8 bit/16 bit)
PC3, 4/ $\overline{16}$ AIN14, 15	2	I/O Input	Port C3, 4: I/O port that allows selection of I/O on a bit basis. Analog Input: Analog input signal for A/D converter
$\overline{\text{EA}}$	1	Input	External access: Always set to _0
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI.(with pull-up R)
X1/X2	2	I/O	High Frequency Oscillator connecting pins (20 MHz)
PB0/ XT1	1	I/O Input	Port B0: I/O port (Open Drain Output) Low Frequency Oscillator connecting pin (32 kHz)
PB1/ XT2	1	I/O Output	Port B1: I/O port (Open drain Output) Low Frequency Oscillator connecting pin
ADREF	1	Input	A/D reference Voltage input
P40 to P47/ AIN3 to AIN10	8	Input Input	Port 4: Input ports Analog input: Analog input signal for A/D converter
PC0 to PC2/ AIN11 to AIN13	3	I/O Input	Port C: PC0 to PC2 I/O port that allows selection of I/O on a bit basis. Analog input: Analog input signal for A/D converter
P57/ TI0/ AIN2	1	I/O Input (schmitt) Input	Port 57: I/O port 8-bit timer0 (TC0) Input 0 Analog input: Analog input signal for A/D converter
P56/ TI4/ AIN1	1	I/O Input (schmitt) Input	Port 56: I/O port 16-bit timer4 (TC4) Input 4 Analog input: Analog input signal for A/D converter
P55/ TI5/ AIN0	1	I/O Input (schmitt) Input	Port 55: I/O port 16-bit timer5 (TC5) Input 5 Analog input: Analog input signal for A/D converter
P54/ INT0	1	I/O Input (schmitt)	Port 54: I/O port External Interrupt request input 0: Rising edge/ Level selectable
P53/ INT1	1	I/O Input (schmitt)	Port 53: I/O port External Interrupt request input 1: Rising edge/ Level selectable
P52/ INT2/ TI1	1	I/O Input Input (schmitt)	Port 52: I/O port External Interrupt request input 2 Rising edge/Falling edge selectable 16-bit timer1(TC1) Input 1

Table 2.2.1 Pin Names and Function (2/5)

Pin name	Number of pins	I/O	Functions
P51/ INT3/ TI2	1	I/O Input Input (schmitt)	Port 51: I/O port External Interrupt request input 3 Rising edge/Falling edge selectable 16-bit timer2 (TC2) Input 2
P50/ INT4/ TI3	1	I/O Input Input (schmitt)	Port 50: I/O port External Interrupt request input 4 Rising edge/Falling edge selectable 16-bit timer3 (TC3) Input 3
PWM0	1	Output 3-state Open Drain	PWM (14 bit) output 0: PWM0 output push/pull or open drain output selectable
PWM1	1	Output 3-state Open Drain	PWM (14 bit) output 1: PWM1 output push/pull or open drain output selectable
PA3/ PWM2	1	I/O 3-state Open Drain	Port A3: I/O port PWM (14 bit) output 2: PWM2 output push/pull or open drain output selectable
PA4/ $\overline{WR}$	1	I/O 3-state Open Drain Output	Port A4: I/O port push/pull or open drain output selectable Write: Strobe signal for writing data on pins D0 to D7
PA5/ PWM3/ $\overline{HWR}$	1	I/O Output 3-state Open Drain Output	Port A5: I/O port 8-bit PWM output 3: PWM3 output push/pull or open drain output selectable High write: Strobe signal for writing data on pins D8 to D15
P60/ PWM4/ $\overline{CS0}$	1	I/O Output 3-state Open Drain Output	Port 60: I/O port 8-bit PWM output 4: PWM4 output push/pull or open drain output selectable Chip select0: Output _0_ when address is within specified address area.
P61/ PWM5/ $\overline{CS1}$	1	I/O Output 3-state Open Drain Output	Port 61: I/O port 8-bit PWM output 5: PWM5 output push/pull or open drain output selectable Chip select1: Output _0_ when address is within specified address area.
P62/ PWM6/ $\overline{CS2}$	1	I/O Output 3-state Open Drain Output	Port 62: I/O port 8-bit PWM output 6: PWM6 output push/pull or open drain output selectable Chip select2: Output _0_ when address is within specified address area.

Table 2.2.1 Pin Names and Function (3/5)

Pin name	Number of pins	I/O	Functions
P63/ PWM7	1	I/O Output 3-state Open Drain	Port 63: I/O port 8-bit PWM output7: PWM7 output push/pull or open drain output selectable
P64/ PWM8	1	I/O Output 3-state Open Drain	Port 64: I/O port 8-bit PWM output8: PWM8 output push/pull or open drain output selectable
P65/ PWM9	1	I/O Output 3-state Open Drain	Port 65: I/O port 8-bit PWM output9: PWM9 output push/pull or open drain output selectable
P66/ PWM10	1	I/O Output 3-state Open Drain	Port 66: I/O port 8-bit PWM output 10: PWM10 output push/pull or open drain output selectable
P67/ PWM11	1	I/O Output 3-state Open Drain	Port 67: I/O port 8-bit PWM output 11: PWM11 output push/pull or open drain output selectable
P73/ SDA0	1	I/O I/O (schmitt) Open Drain	Port 73: I/O port I^2CBUS SDA line 0 push/pull or open drain output selectable
P74/ SCL0	1	I/O I/O (schmitt) Open Drain	Port 74: I/O port I^2CBUS SCL line 0 push/pull or open drain output selectable
P75/ SO0	1	I/O Output (schmitt) Open Drain	Port 75: I/O port SIO0 send data 0 push/pull or open drain output selectable
P76/ SI0	1	I/O Input (schmitt)	Port 76: I/O port SIO0 receive data 0
P77/ SCK0	1	I/O I/O (schmitt) Open Drain	Port 77: I/O port SIO0 transfer clock input/output 0 push/pull or open drain output selectable
P70/ TXD	1	I/O Output (schmitt) Open Drain	Port 70: I/O port UART send data push/pull or open drain output selectable
P71/ RXD	1	I/O Input (schmitt)	Port 71: I/O port UART receive data
P72/ $\overline{CTS}$	1	I/O Input (schmitt)	Port 72: I/O port UART clear to send
P80/ CTLIN	1	I/O Input (schmitt)	Port 80: I/O port Capture input for Control signal (CTL)

Table 2.2.1 Pin Names and Function (4/5)

Pin Name	Number of pins	I/O	Functions
P81/ DFGIN	1	I/O Input (schmitt)	Port 81: I/O port Capture input for Drum-FG signal (DFG)
P82/ RMTIN	1	I/O Input (schmitt)	Port 82: I/O port Capture input for Remote Control Input signal
P83/ EXT	1	I/O Input (schmitt)	Port 83: I/O port External Capture input (Rising edge only)
P84/ DPGIN	1	I/O Input (schmitt)	Port 84: I/O port Capture input for Drum-PG signal (DPG)
P85/ CFGIN	1	I/O Input (schmitt)	Port 85: I/O port Capture input for Capstan-FG signal (CFG)
P86/ CSYNC IN	1	I/O Input (schmitt)	Port 86: I/O port Capture input for C-sync
P87/ COMPIN	1	I/O Input (schmitt)	Port 87: I/O port Envelope Comparator Input (to HA/CR)
P90/ TPG12	1	I/O Output Open Drain	Port 90: I/O port TPG12: TPG output 12 push/pull or open drain output selectable
P91/ TPG01	1	I/O Output Open Drain	Port 91: I/O port TPG01: TPG output 01 push/pull or open drain output selectable
P92/ TPG02	1	I/O Output Open Drain	Port 92: I/O port TPG02: TPG output 02 (Internally connected to PV/PH Logic) push/pull or open drain output selectable
P93/ TPG03	1	I/O Output Open Drain	Port 93: I/O port TPG03: TPG output 03 push/pull or open drain output selectable
P94/ TPG04	1	I/O Output Open Drain	Port 93: I/O port TPG04: TPG output 04 (Internally connected to PV/PH Logic) push/pull or open drain output selectable
P95/ TPG13	1	I/O Output Open Drain	Port 95: I/O port TPG13: TPG output 13 push/pull or open drain output selectable
P96/ TPG10	1	I/O Output Open Drain	Port 96: I/O port TPG10: TPG output 10 push/pull or open drain output selectable
P97/ TPG11	1	I/O Output Open Drain	Port 97: I/O port TPG11: TPG output 11 push/pull or open drain output selectable
PA0/ PV-PH	1	I/O Output 3-state	Port PA0: I/O Port Pseudo-Vsync/Pseudo-Hsync (PV/PH) output (controlled by TPG02/04.)
PA1/ HA (TPG05)	1	I/O Output	Port PA1: I/O Port HA: Head amp switch output (are also used as TPG05 output.)
PA2/ CR (TPG00)	1	I/O Output	Port PA2: I/O Port CR: Colour Rotary output (are also used as TPG00 output.)

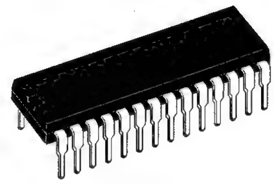
Table 2.2.1 Pin Names and Function (5/5)

Pin name	Number of pins	I/O	Functions
PB2/ SO1/SI1	1	I/O I/O (schmitt) Open Drain	Port PB2: I/O Port SIO1 send data 1 and receive data 1 (Internally connected) push/pull or open drain output selectable
PB3/ SCK1	1	I/O I/O (schmitt) Open Drain	Port PB3: I/O Port SIO1 transfer clock input/output 1 push/pull or open drain output selectable
PB4/ SDA1	1	I/O I/O (schmitt) Open Drain	Port PB4: I/O Port I^2CBUS SDA line 1 push/pull or open drain output selectable
PB5/ SCL1	1	I/O I/O (schmitt) Open Drain	Port PB5: I/O Port I^2CBUS SCL line 1 push/pull or open drain output selectable
DVCC1, 2, 3	3		Power supply pins All of these pins should be connected to power source.
DGND1, DGND2 (ADGND), DGND3	3		GND pins (0 V) All of these pins should be connected to GND (0 V) line. DGND2 are also used as ADGND for A/D converter.

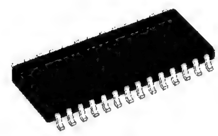
9.8.8 IC7990: STV5348

STV5348

- COMPLETE TELETEXT AND VPS DECODER INCLUDING AN 8 PAGE MEMORY ON A SINGLE CHIP
- UPWARD SOFTWARE COMPATIBLE WITH PREVIOUS SGS-THOMSON's MULTICHIP SOLUTIONS (SAA5231, SDA5243, STV5345)
- PERFORM PDC SYSTEM A (VPS) AND PDC SYSTEM B (8/30/2) DATA STORAGE SEPARATLY
- DEDICATED "ERROR FREE" OUTPUT FOR VALID PDC DATA
- INDICATION OF LINE 23 FOR EXTERNAL USE
- SINGLE +5V SUPPLY VOLTAGE
- SINGLE 13.875MHz CRYSTAL
- REDUCED SET OF EXTERNAL COMPONENTS, NO EXTERNAL ADJUSTMENT
- OPTIMIZED NUMBER OF DIGITAL SIGNALS REDUCING EMC RADIATION
- HIGH DENSITY CMOS TECHNOLOGY
- DIGITAL DATA SLICER AND DISPLAY CLOCK PHASE LOCK LOOP
- 28 PIN DIP & SO PACKAGE



DIP28
(Plastic Package)
ORDER CODE :
STV5348 West European
STV5348/H East European
STV5348/T Turkish & European



SO28
(Plastic Package)
ORDER CODE :
STV5348D West European
STV5348D/H East European
STV5348D/T Turkish & European

DESCRIPTION

The STV5348 decoder is a computer-controlled teletext device including an 8 page internal memory. Data slicing and capturing extracts the teletext information embedded in the composite video signal. Control is accomplished via a two wire serial I^2C bus ®. Chip address is 22h. Internal ROM provides a character set suitable to display text using up to seven national languages. Hardware and software features allow selectable master/slave synchronization configurations. The STV5348 also supports facilities for reception and display of current level protocol data.

PIN CONNECTIONS

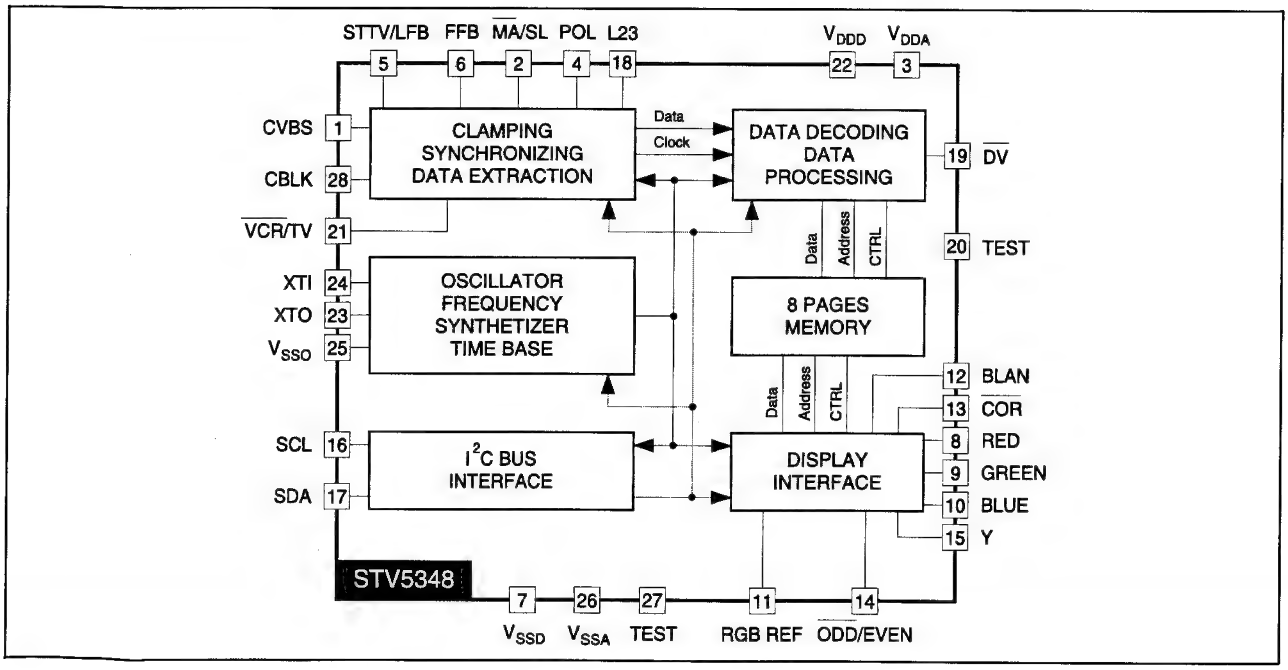
CVBS	1	28	CBLK
$\overline{MA}$/SL	2	27	TEST
V_{DDA}	3	26	V_{SSA}
POL	4	25	V_{SSD}
STTV/LFB	5	24	XTI
FFB	6	23	XTO
V_{SSD}	7	22	V_{DDD}
R	8	21	$\overline{VCR}$/TV
G	9	20	RESERVED
B	10	19	$\overline{DV}$
RGB REF	11	18	L23
BLAN	12	17	SDA
$\overline{COR}$	13	16	SCL
$\overline{ODD}$/EVEN	14	15	Y

PIN DESCRIPTION

Pin N°	Symbol	Function	Description	Figure
1	CVBS	Input	Composite Video Signal Input through Coupling Capacitor	9
2	MA/SL	Input	Master/Slave Selection Mode	11
3	V_{DDA}	Analog Supply	+5V	-
4	POL	Input	STTV / LFB / FFB Polarity Selection	12
5	STTV/LFB	Output / Input	Composite Sync Output, Line Flyback Input	15
6	FFB	Input	Field Flyback Input	12
7	V_{SSD}	Ground	Digital Ground	-
8	R	Output	Video Red Signal	13
9	G	Output	Video Green Signal	13
10	B	Output	Video Blue Signal	13
11	RGBREF	Supply	DC Voltage to define RGB High Level	13
12	BLAN	Output	Fast Blanking Output TTL Level	15
13	COR	Output	Open Drain Contrast Reduction Output	15
14	ODD/EVEN	Output	25Hz Output Field synchronized for non-interlaced display	15
15	Y	Output	Open Drain Foreground Information Output	15
16	SCL	Input	Serial Clock Input	16
17	SDA	Input/ Output	Serial Data Input/Output	17
18	L23	Output	Line 23 Identification	15
19	DV	Output	VPS Data Valid	15
20	RESERVED	Test	To be connected to V_{SSD} through a resistor	15
21	VCR/TV	Input	PLL Time Constant Selection	15
22	V_{DDD}	Digital Supply	+5V	-
23	XTO	Crystal Output	Oscillator Output 13.875MHz	14
24	XTI	Crystal Input	Oscillator Input 13.875MHz	14
25	V_{SSO}	Ground	Oscillator Ground	-
26	V_{SSA}	Ground	Analog Ground	-
27	TEST	Test	Grounded to V_{SSA}	11
28	CBLK	Input / Output	To connect Black Level Storage Capacitor	28

5348-01.TBL

BLOCK DIAGRAM



9.8.9 **Tuner1705: UV1316K**

VHF/UHF television tuner UV1336K MK3

FEATURES

- Member of UV1300 MK3 family of small-sized UHF/VHF tuners
- Integrated with passive splitter
- Covers systems M, N
- Digitally-controlled (PLL) tuning via I^{2}C-bus
- Fast 400kHz I^{2}C bus protocol compatible with 3.3V and 5V micro controllers
- 181 channels coverage (Off-air and full cable)
- World standardized mechanical dimensions and pinning. Horizontal mounting is optionally available.

DESCRIPTION

The UV1336K MK3 splitter - tuner belongs to the UV1300 family of WSP tuners, which are designed to meet a wide range of TV applications. It is a full band tuner suitable for NTSC M, N and PAL M, N. The low IF output impedance is designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

The UV1336K MK3 incorporates internal wideband-AGC with selectable TOP adjustment via I^{2}C.

This tuner complies with the requirements of radiation, conforming with:

- FCC Part 15, Subpart B
- BETS 7
- CISPR13

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner:

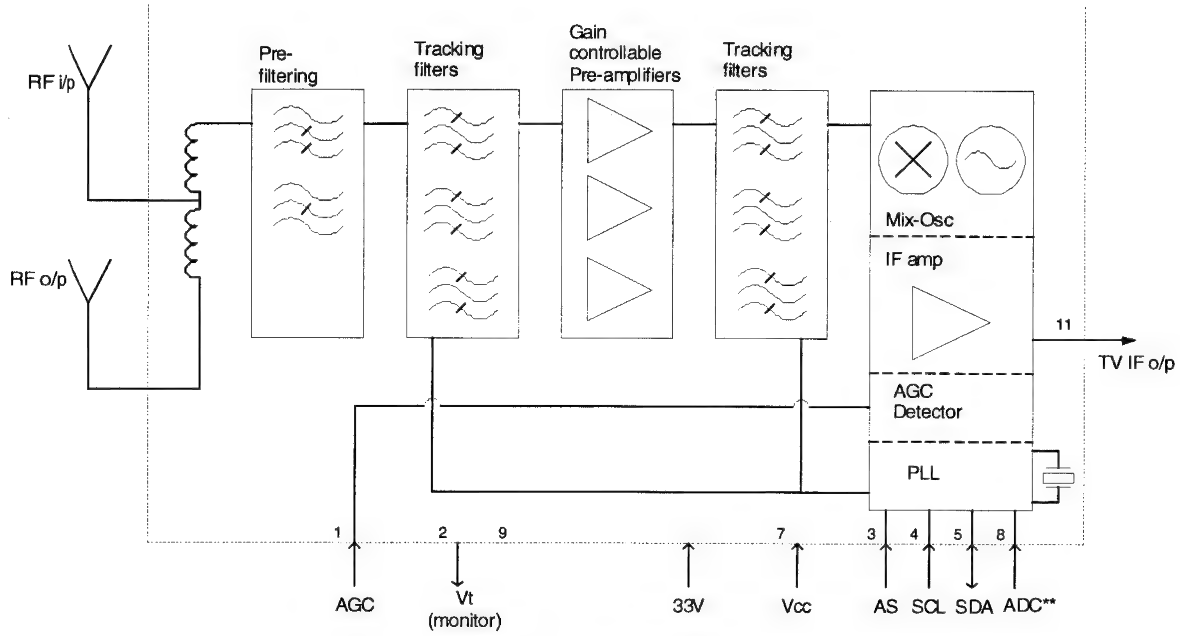
- Type number
- Code number
- Origin letter of factory
- Change code
- Year and week code

ORDERING INFORMATION

TYPE	DESCRIPTION	ORDER NUMBERS
UV1336K/A F G S-3	F connector, wideband AGC, switchable FM trap	3139 147 17011

VHF/UHF television tuner UV1336K MK3

BLOCK DIAGRAM



** ADC option not available in NTSC versions

PINNING

SYMBOL	PIN	DESCRIPTION
AGC	1	Gain Control Voltage
TU	2	Tuning voltage
AS	3	I^2C-Bus Address Select
SCL	4	I^2C-Bus Serial Clock
SDA	5	I^2C-Bus Serial Data
n.c.	6	Not Connected
V_s	7	PLL Supply Voltage +5V
n.c	8	Not Connected
V_{ST}	9	Fixed tuning Supply Voltage +33V
n.c	10	Not connected
IF1	11	Asymmetrical IF Output
GND	M1,M2,M3,M4	Mounting Tags (Ground)

9.9 IC's Digital Board

9.9.1 IC7100: VSM

VERSATILE STREAM MANAGER

GENERAL DESCRIPTION

The Versatile Stream Manager (VSM) is an ASIC used in the first generation DVD Video Recorder. Main function of the VSM is to interface directly to the different hardware modules such as Basic Engine, MPEG encoders, MPEG decoders and buffering the data streams that are coming from or going to these hardware modules.
The VSM contains a memory interface to support one 4M*16 SDRAM device. A host interface allows a CPU to directly access this memory and the VSM's internal registers.
Handling of data streams is done using scatter / gather DMA's under software control. Hardware support is provided in the VSM to support software MPEG AV multiplexing.

FEATURES

The VSM features include:

- SDRAM memory interface to support one 4 banks*1M*16 (64Mbit) SDRAM device.
- Glueless Host Interface for STM's STi5505.
- Glueless MPEG Decoder interface for STM's STi5505
- Glueless interface to Philips' SAA6750 MPEG Video Encoder or SAA6752 MPEG AV Encoder.
- Glueless interface to Motorola's DSP56362 used as MPEG Audio Encoder.
- Glueless interface to Philips' HDR65 as part of Basic Engine interface including the Sector Processor as also included in the STi5505.
- Audio Clock Control providing PLL loop and clock lock detection.
- Double Extraction of VBI decoded data from extended CCIR 656 stream.
- Double UART with hardware handshake and 8 byte Rx/Tx FIFO.
- Generation of additional Host Bus to support Audio Encoder DSP56362.
- Descriptor based DMA Controllers for data stream handling.
- Hardware support for software MPEG multiplex process.
- Internal Interrupt Controller to handle internal and 4 external interrupt sources.
- Operates from single 27 MHz clock input.
- JTAG for production tests.
- 3.3V logic core.
- 3.3V / 5V toleration IO pins.
- 208 PIN LQFP Package. (CR1087)

BLOCK DIAGRAM

Figure 2.1 shows the block diagram of the VSM. The hardware blocks can be divided in to three categories:

- General modules: Host Interface, Memory Interface, Interrupt Controller.
- DMA Controllers.
- Functional Interfaces; the link between the actual external hardware interface and the DMA Controller. Some Functional Interfaces have knowledge about the stream coming through in order to perform for example MPEG stream characteristics extraction and insertion.

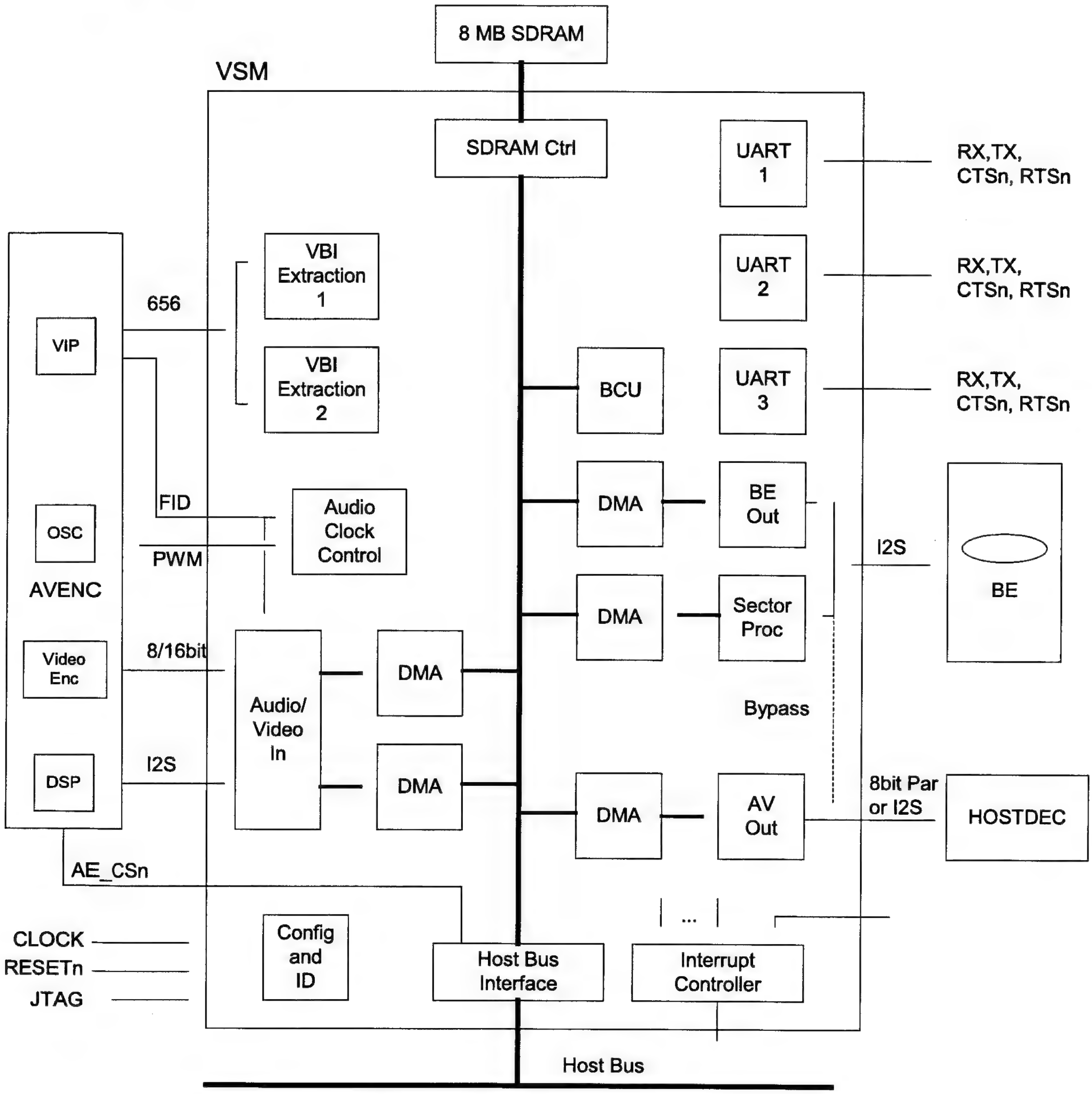


Figure 2.1: VSM Overview

PINNING

OVERVIEW

Name	Pins	Type	Function
System			
RESETn	1	In	
SYSCLK (27MHz)	1	In	
Host Interface			
HO_A(21:1)	21	In	
HO_D(15:0)	16	In/Out	
HO_BEn(1:0)	2	In	
HO_RWn	1	In	
HO_CSLn	1	In	
HO_CSHn	1	In	
HO_A22	1	In	
HO_WAIT	1	Out	
HO_PROCCLK	1	In	
Memory Interface			
M_A(13:0)	14	Out	
M_DQ(15:0)	16	In/Out	
M_RASn	1	Out	
M_CASn	1	Out	
M_WEn	1	Out	
M_LDQM	1	Out	
M_UDQM	1	Out	
M_CLKOUT	1	Out	
M_CLKEN	1	Out	
Basic Engine Interface			
BE_BCLK	1	In	
BE_DATI	1	In	
BE_WCLK	1	In	
BE_SYNC	1	In/Out	
BE_FLAG	1	In	
BE_V4	1	In	
BE_DATO	1	Out	
Video Encoder Interface			
VE_D(15:0)	16	In	
VE_DSn	1	Out	
VE_DTACKn	1	In	
VE_VIP_ERROR	1	In	Signal coming from SAA7114
Audio Encoder Interface			
AE_CSn	1	Out	
AE_BCLK	1	In/Out	(CR151,CR157)
AE_WCLK	1	In/Out	(CR151,CR157)
AE_DATA	1	In	(CR157)

Decoder Interface			
D_PAR_D(7:0)	8	Out	
D_PAR_DVALID	1	Out	
D_PAR_STR	1	Out	
D_PAR_REQ	1	In	
D_PAR_SYNC	1	Out	
D_WCLK	1	Out	
D_V4	1	Out	
Audio Clock Control			
ACC_FID	1	In	(CR200)
ACC_PWM	1	Out	
ACC_ACLK_OSC	1	In	
ACC_ACLK_DAI	1	In	
ACC_ACLK_PLL	1	In	
ACC_ACLK_DEC	1	Out	
VBI Extractor			
VBI_IPD(7:0)	8	In	
VBI_ICLK	1	In	
UART 1			
UART1_RX	1	In	
UART1_TX	1	Out (OC)	
UART1_CTSn	1	In	
UART1_RTSn	1	Out (OC)	
UART 2			
UART2_RX	1	In	
UART2_TX	1	Out (OC)	
UART2_CTSn	1	In	
UART2_RTSn	1	Out (OC)	
UART 3 **(VSM1B)**			
UART3_RX	1	In	
UART3_TX	1	Out	
UART3_CTSn	1	In	
UART3_RTSn	1	Out	
Interrupt Controller			
EXTINT(3:0)	4	In	From: VEnc, AEnc, BE, VSync (STi5505)
CPUINT(1:0)	2	Out (OC)	
JTAG			
TCK	1	In	Boundary Scan
TDI	1	In	
TDO	1	Out/Z	
TMS	1	In	
TRSTn	1	In	
Test			
TEST0	1	In	Amsal Test
TEST1	1	In	
Power Supply			
VDD	20	Power	10% of total pins package
VSS	20	Power	10% of total pins package

Total Pins	208		

9.9.2 IC7101; IC7306: SDRAM

SDRAM MT48LC1M16A1 SIT - 512K x 16 x 2 banks

FEATURES

- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
  1 Meg x 16 - 512K x 16 x 2 banks architecture with 11 row, 8 column addresses per bank
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge Mode, includes CONCURRENT AUTO PRECHARGE
- Self Refresh and Adaptable Auto Refresh Modes
  - 32ms, 2,048-cycle refresh or
  - 64ms, 2,048-cycle refresh or
  - 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Supports CAS latency of 1, 2 and 3
- Industrial temperature range: -40°C to +85°C

OPTIONS / MARKING

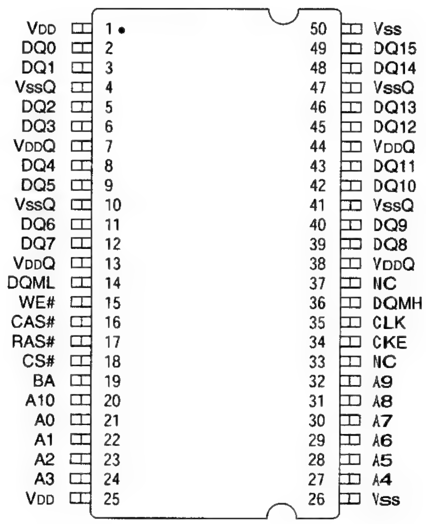
OPTIONS	MARKING
• Configuration	
1 Meg x 16 (512K x 16 x 2 banks)	1M16A1
• Plastic Package - OCPL*	
50-pin TSOP (400 mil)	TG
• Timing (Cycle Time)	
6ns (166 MHz)	-6
7ns (143 MHz)	-7
8ns (125 MHz)	-8A
• Refresh	
2K or 4K with Self Refresh Mode at 64ms	S
• Operating Temperature	
-40°C to +85°C	IT

- Part Number Example: MT48LC1M16A1TG-7SIT

KEY TIMING PARAMETERS

SPEED	CLOCK	ACCESS TIME CL = 3**	SETUP	HOLD
-6	166 MHz	5.5ns	2ns	1ns
-7	143 MHz	5.5ns	2ns	1ns
-8A	125 MHz	6ns	2ns	1ns

PIN ASSIGNMENT (Top View)
50-Pin TSOP



Note: The # symbol indicates signal is active LOW.

	1 Meg x 16
Configuration	512K x 16 x 2 banks
Refresh Count	2K or 4K
Row Addressing	2K (A0-A10)
Bank Addressing	2 (BA)
Column Addressing	256 (A0-A7)

16Mb (x16) SDRAM PART NUMBER

PART NUMBER	ARCHITECTURE
MT48LC1M16A1TG SIT	1 Meg x 16

GENERAL DESCRIPTION

The 16Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual 512K x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16-bit banks is organized as 2,048 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed

GENERAL DESCRIPTION (continued)

sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

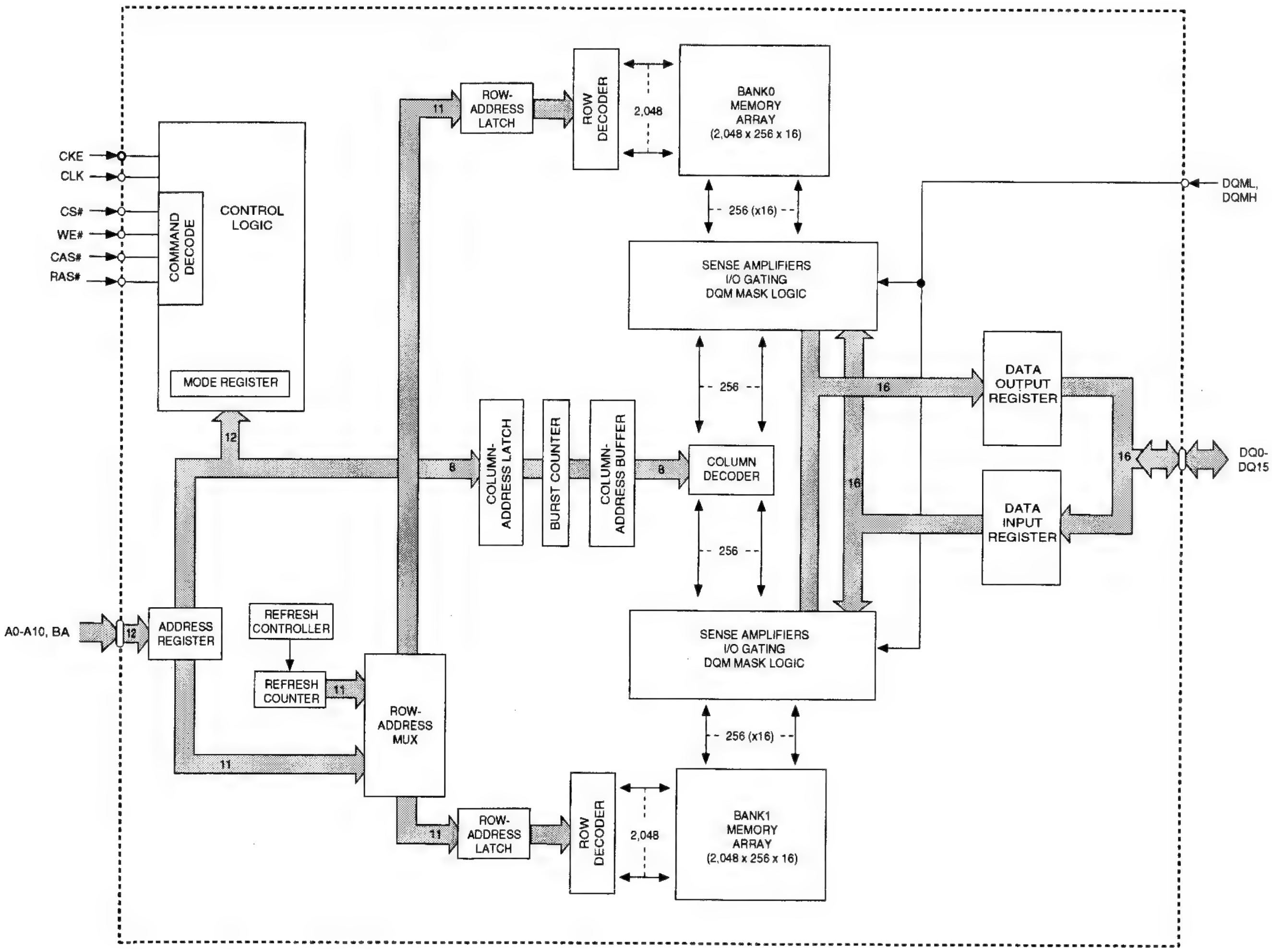
The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 1 Meg x 16 SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 1 Meg x 16 SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

FUNCTIONAL BLOCK DIAGRAM
1 Meg x 16 SDRAM



PIN DESCRIPTIONS

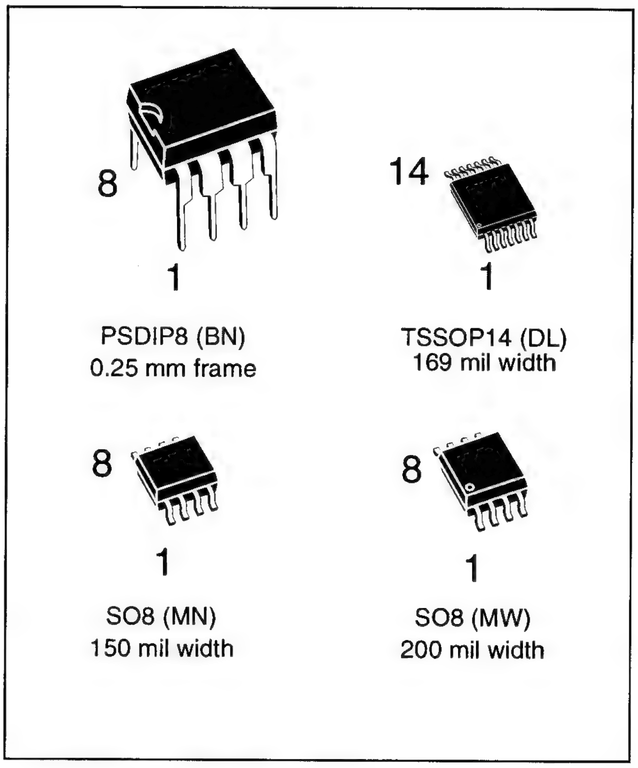
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
35	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
34	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), ACTIVE POWER-DOWN (row ACTIVE in either bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
18	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
15, 16, 17	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
14, 36	DQML, DQMH	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQML corresponds to DQ0-DQ7; DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
19	BA	Input	Bank Address Inputs: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the twelfth bit of the Mode Register.
21-24, 27-32, 20	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7, with A10 defining AUTO PRECHARGE) to select one location out of the 512K available in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0-DQ15	Input/ Output	Data I/Os: Data bus.
33, 37	NC	–	No Connect: These pins should be left unconnected.
7, 13, 38, 44	$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
4, 10, 41, 47	$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 25	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
26, 50	V_{SS}	Supply	Ground.

9.9.3 IC7200: NVRAM

M24C64
M24C32

64/32 Kbit Serial I²C Bus EEPROM

- Compatible with I²C Extended Addressing
- Two Wire I²C Serial Interface Supports 400 kHz Protocol
- Single Supply Voltage:
  - 4.5V to 5.5V for M24Cxx
  - 2.5V to 5.5V for M24Cxx-W
  - 1.8V to 3.6V for M24Cxx-R
- Hardware Write Control
- BYTE and PAGE WRITE (up to 32 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- 1 Million Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)



DESCRIPTION

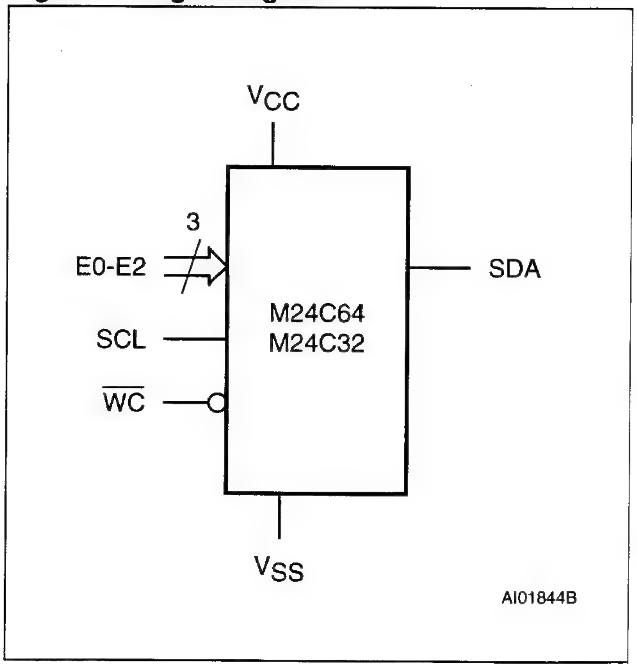
These I²C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192x8 bits (M24C64) and 4096x8 bits (M24C32), and operate down to 2.5 V (for the -W version of each device), and down to 1.8 V (for the -R version of each device).

The M24C64 and M24C32 are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages.

Table 1. Signal Names

E0, E1, E2	Chip Enable Inputs
SDA	Serial Data/Address Input/ Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



M24C64, M24C32

Figure 2A. DIP Connections

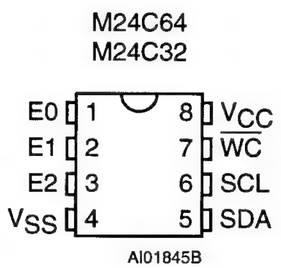
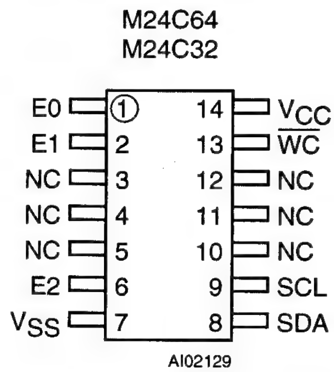
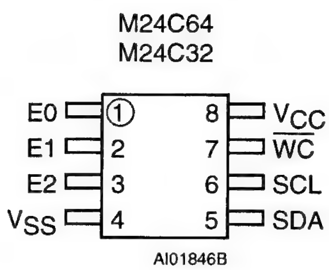


Figure 2C. TSSOP Connections



Note: 1. NC = Not Connected

Figure 2B. SO Connections



These memory devices are compatible with the I^2C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4-bit unique Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The memory behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and $R\overline{W}$ bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission.

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		-40 to 125	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PSDIP8: 10 sec SO8: 40 sec TSSOP14: t.b.c.	260 215 t.b.c.	°C
V_{IO}	Input or Output range		-0.6 to 6.5	V
V_{CC}	Supply Voltage		-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

9.9.4 IC7202: Sti5505

STi5505 (Rev. Ax)

DVD BACKEND DECODER WITH INTEGRATED HOST PROCESSOR

PRODUCT PREVIEW

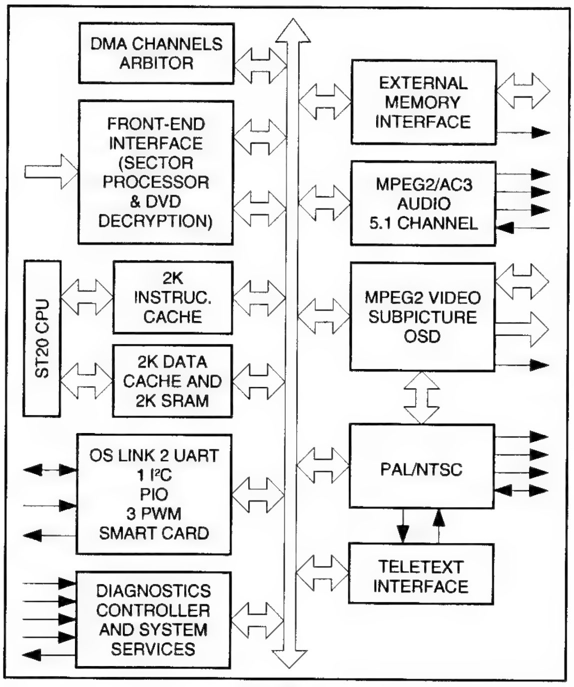
- INTEGRATED 32-BIT RISC HOST CPU
  - 2KBYTES INSTRUCTION CACHE, 2KBYTES DATA CACHE/SRAM
  - 50K DHRYSTONES/SEC (2.1) - 50MHz
- VIDEO DECODER
  - FULLY SUPPORTS MPEG-2 MP@ML
  - MEMORY REDUCTION - PAL IN 12MBITS
- SUBPICTURE DECODER
- HIGH PERFORMANCE ON-SCREEN DISPLAY
- AUDIO DECODER
  - 5.1 CHANNEL DOLBY AC-3® / MULTI CHANNEL MPEG-2 DECODING
  - DOWNMIX TO STEREO OR TO DOLBY PRO-LOGIC COMPATIBLE OUTPUTS FOR MPEG-2 AND AC-3
  - IEC6958 - IEC61937 COMPATIBLE OUTPUT
  - LPCM (DVD) MODE SUPPORTED
  - 6 CHANNELS OUTPUT
- PAL/NTSC ENCODER
  - MACROVISION™ 7.01/6.1 COMPATIBLE
  - TELETEXT, AND CLOSED CAPTION
- HIGH PERFORMANCE SDRAM INTERFACE
- PROGRAMMABLE MEMORY INTERFACE FOR DRAM, ROM, PERIPHERALS ETC.
- FRONT-END CHANNEL IC INTERFACE
  - DVD, VCD AND CD-DA COMPATIBLE
  - DSS - DVB BISTREAMS
  - SERIAL AND PARALLEL INTERFACES
  - HARDWARE SECTOR FILTERING
  - INTEGRATED CSS DECRYPTION AND TRACK BUFFER
- INTEGRATED PERIPHERALS
  - 2 UARTS, 1 I²C CONTROLLER, 3 PWM OUTPUTS, 3 TIMERS, 3 CAPTURE TIMERS, SMART CARD
  - 34 BITS OF PROGRAMMABLE I/O
  - OS LINK
- PROFESSIONAL TOOLSET SUPPORT
  - ANSI C COMPILER AND LIBRARIES
  - OPERATING SYSTEMS SUPPORT
  - ADVANCED DEBUGGING TOOLS
- 208 PIN PQFP PACKAGE

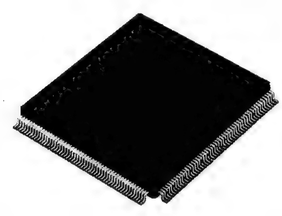
DESCRIPTION

The STi5505 provides a very highly integrated back-end solution for DVD and combo DVD-DVB (Set Top Box) applications. The STi5505 incorporates a host CPU which handles both general application (DVD navigation, CD-DA, VCD, DVB) and drivers of the different embedded periphals (audio/video, subpicture decoders, OSD, PAL/NTSC encoder...).

The STi5505 offers one of the best cost-effective (memory savings, internal peripherals availability) solution to DVD-DVB applications with rapid time to market (Reference design, DVD-DVB Software Toolkit).

Figure 1 : General Block Diagram





PQFP208 (Plastic Quad Flat Pack)
ORDER CODE : STi5505ACV

STi5505 (Rev. Ax)

I - GENERAL DESCRIPTION

The performance offered by the ST20 CPU and its associated hardware (decoders, encoder, peripherals...) allows an integrated and unified DVD or DVD-DVB software solution.

All the following operations are performed inside the STi5505 :

- application management (DVD Navigation, VCD, CD-DA, DVB-Program Guide ...),
- device data retrieval drivers (demultiplex, stream buffer management ...),
- device presentation drivers (video decoder, subpicture decoder, on-screen display, audio decoder, PAL/NTSC encoder ...),
- embedded peripherals drivers (UART, I^2C, Programmable I/O, Smart Card ...).

I.1 - ST20 32-bit CPU

The ST20 micro-core family has been developped by SGS-THOMSON Microelectronics to provide the tools and building blocks to enable the development of highly integrated application-specific 32-bits device at the lowest cost and fastest time to market.

The STi5505 integrates a ST20 C2 core with the following characteristics :

- 50K Dhrystones/s at 50MHz,
- 8/16 bits instructions (32 most common instructions in 8 bits),
- instruction cache 2Kbytes - write back replacement policy,
- internal SRAM 2Kbytes to ensure fast access to critical code, data, interrupt handler ...
- data cache 2 Kbytes - write back replacement policy,

The STi5505's ST20 is provided with advanced debugging tools :

- on-chip real-time emulation,
- debugging with minimal impact on software and performance,
- non intrusive attachment to the host via JTAG (IEEE1149.1),
- no intrusion into the performance of the CPU core,
- no intrusion into user code space by a debug kernel,
- only 40bytes used for breakpoint handler.

I.2 - Video Decoder

The video decoder implemented in the STi5505 uses a patented memory reduction/bandwith reduction scheme to offer the user the best bandwidth/memory size compromise.

The algorithm is lossless and uses "on-the-fly" decoding to reduce the memory requirements to two frame buffers in memory reduction mode.

In this mode, PAL decoding is contained in 12Mbits. When used in bandwith reduction mode, the memory usage is the normal three buffers but the bandwith required by the decoder is significantly reduced compared to a classical implementation.

In summary, the features of the decoder are :

- MPEG-2 Main Profile/Main Level (MP@ML) support,
- MPEG-2 program streams, Packet Elementary streams and MPEG-1 system streams support,
- memory reduction architecture allowing sharing of single 16 Mbits SDRAM between MPEG decoding, micro and transport functions - memory expandable to 32 Mbits of SDRAM,
- letter box (16:9) filter,
- pan-scan, horizontal and vertical image resizing,
- automatic error concealment.

I.3 - Subpicture Decoder

The STi5505 has a hardware DVD compliant subpicture decoder. Subpicture units are copied by DMA into subpicture bit buffer.

The subpicture decoder can decode complete subpicture units without any interaction from the ST20.

The main subpicture decoder features are :

- up to 720x480 or 720x576 subpicture area,
- internal LUTs for Sub Picture, Highlight and PCI (4 bits color and contrast outputs),
- internal color LUT (4 bits from SP, HL, PCI to 24 Y,Cr,Cb bits) for SP color inputs to MPEG, OSD, SP mixer.

I.4 - Audio Decoder

The audio decoder cell is a fully compatible Dolby AC-3™ / MPEG-1/MPEG-2 decoder capable of decoding both 5.1 and 2 channel streams compatible with the DVD standard.

Downmix from 5.1 channels is supported for both Dolby and MPEG-2 streams. The output can be sent directly to external DACs or formatted for transmission in accordance with the IE6958 standard.

The decoder can also handle linear PCM in accordance with the DVD standard. An integrated downsampler is provided for conversion from 96 kHz to 48kHz.

STi5505 (Rev. Ax)

I - GENERAL DESCRIPTION (continued)

The main features of the decoder core are :

- Decodes 5.1 Dolby AC-3 Digital surround,
- Output to 6 channels. Downmix modes : 1, 2, 3 or 4 channels for MPEG and AC-3 streams,
- Karaoke mode for DVD. MPEG-2 capable, AC-3 capable,
- MPEG-1, 2-channel audio decoder layers 1 and 2,
- MPEG-2, 6-channel audio decoder layer 2,
- PCM : transparent. downsampling 96 to 48 kHz,
- Accepts MPEG-2 PES stream format for : MPEG-2, MPEG-1, Dolby AC-3 and Linear PCM,
- IEC6958 Output Interface,
- CD-DA PCM format (subcode output in IEC6958 user data),
- Downmix for Dolby Pro Logic compatible outputs for AC-3 and MPEG-2 (Pro Logic encoder),
- Pro Logic decoder,
- PLL for Internal 44.1 and 48kHz PCM clock generation,
- On chip pink noise generator.

I.5 - High Performance On-Screen Display

The graphics performance of the STi5505 supports the new requirements for intelligent program guides and interactive applications.

The display interface supports up to 256 colors for each OSD region and a transparency feature allows mixing of video with the OSD. Fast access graphics and many other additional features are available and are supported by a graphics library.

Very high system performance is obtained by closely coupling the ST20 RISC processor and cache with the MPEG audio/video core and display memory.

Low latency RISC access and DMA engines allow rapid construction of bit maps.

I.6 - PAL/NTSC Encoder

The STi5505 integrates a PAL/NTSC encoder. It converts the digital MPEG/Sub Picture/OSD stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. Six analog output pins are available on which it is possible to output CVBS, S-VHS (Y/C) and RGB formats.

The encoder handles interlaced and non-interlaced mode.

It can perform Closed Captions, CGMS orTeletext encoding and allows Macrovision 7.01/6.1 copy protection.

The encoder supports both master and slave modes for synchronization.

I.7 - Memory Interfaces

The STi5505 has been designed to minimize system costs by enabling various memory savings. Two kinds of memory interfaces are used on the STi5505 : a programmable External Memory Interface (EMI) and a high performance SDRAM interface.

The External Memory Interface supports several address ranges (memory banks). In each bank, a set of signals are entirely programmable and can be used to map 8/16 bits peripherals such as Front End channel ICs in DVD applications.

The EMI contains a zero glue logic DRAM and a low-cost EPROM interface.

This interface can be programmed to interface very easily peripherals.

The SDRAM memory interface supports gluelessly 125 MHz SDRAMs providing the adequate bandwiths to achieve MPEG decoding and display, OSD drawing and display, and general system use.

Memory savings can be realized on ROM requirements too : the ST20 VL-RISC micro-core has the highest code density of any 32 bit CPU, leading to the lowest cost program ROM.

I.8 - Front-End Interface

The STi5505 's front end interface accepts :

- DVD, VCD and CD-DA sectors,
- DVB-DSS transport stream.

In DVD mode, DVD, VCD and CD-DA information can be input into STi5505 through a serial interface or a generic parallel interface.

In serial mode, data are captured and filtered from I2S and V4 interfaces by an internal sector processor. V4 interface is used to capture VCD and CD-DA subcode information. In parallel mode, sector processor is bypassed.

I - GENERAL DESCRIPTION (continued)

The main features of the DVD interface are :

- DVD, VCD and CD-DA compatible,
- hardware sector filtering,
- subcode error correction for CD-DA,
- integrated CSS decryption,
- integrated track buffer support,
- DMA engine to ST20 memory.

In DVB-DSS mode, DVB-DSS transport stream is input through a serial interface. The STi5505 extracts and descrambles Packet Elementary Streams belonging to one user selected program to be decoded and presented.

The main features of the DVB-DSS interface are :

- descrambling (transport packet and packet elementary streams in DVB mode, transport packet in DSS mode ; up to 32 streams descrambling),
- PID and section filtering,
- clock recovery,
- DMA engine.

In DVB-DSS mode, a high speed digital interface allows to transfer packets between the Set Top Box and external units, either for recording or playback purposes. This interface provides also full support for an external IEEE1394 connection.

I.9 - Integrated Peripherals

Several peripherals generally used in DVD players or DVD-DVB combos have been integrated into the STi5505.

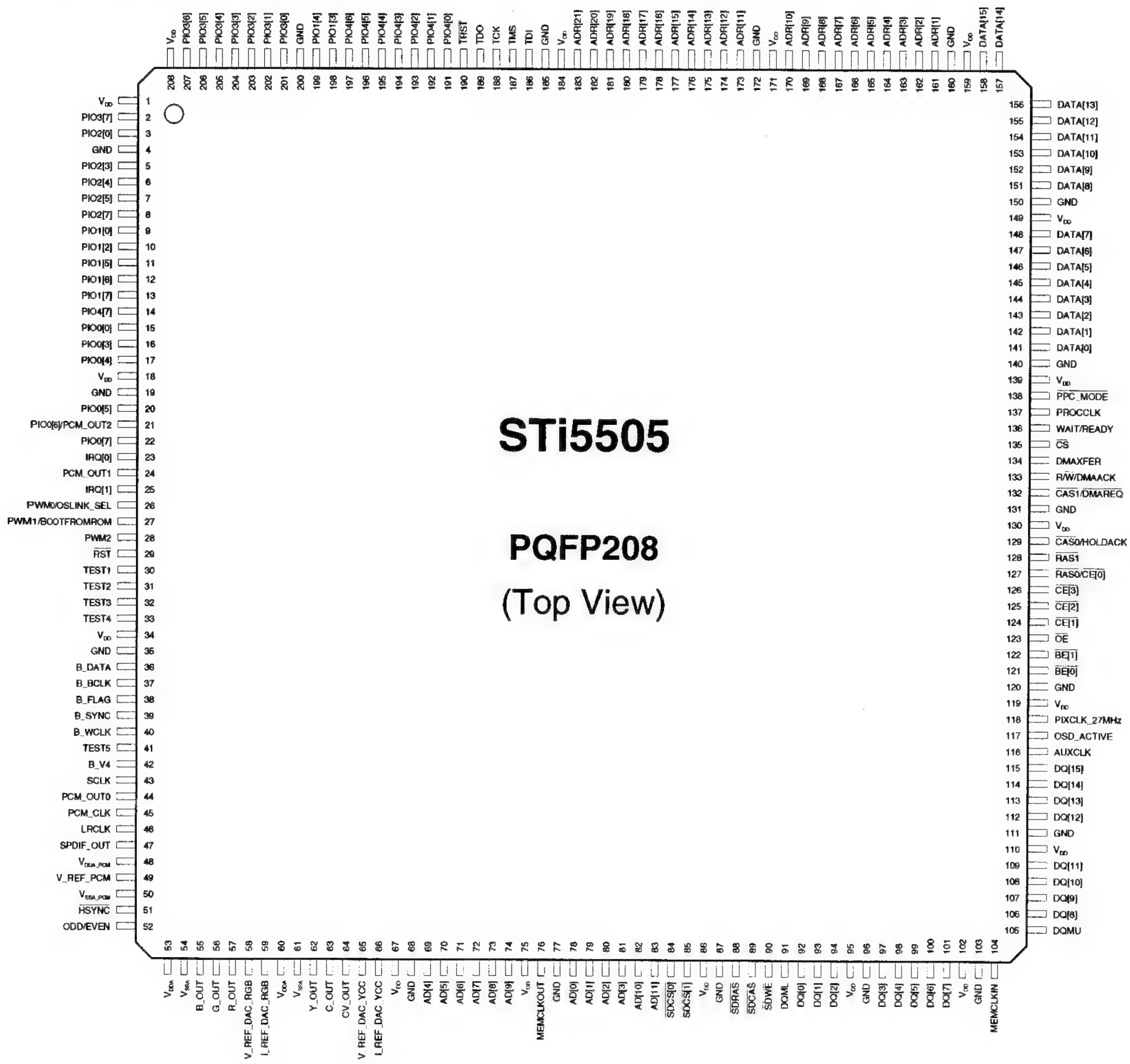
They are :

- two UARTs to interface remote control receivers, DVD front end, modem ...,
- one I^2C controller to interface serial memories, remote control receivers, microcontrollers...,
- 2 SmartCard interfaces (ISO7816-3) for DVB-DSS conditionnal access, pay per view ...,
- PWM/timer module for control of system clock,
- 34 programmable I/O pins,
- OS Link interface,
- JTAG with boundary scan for debug.

STi5505 (Rev. Ax)

II - PIN DESCRIPTION

II.1 - Pin Connections



STi5505 (Rev. Ax)

II - PIN DESCRIPTION (continued)

II.2 - Pin List

Pin	Name	Type	Function
SUPPLIES			
1, 18, 34, 67, 75, 86, 95, 102, 110, 119, 130, 139, 149, 159, 171, 184, 208	V_{DD}		Power Supply
4, 19, 35, 68, 77, 87, 96, 103, 111, 120, 131, 140, 150, 160, 172, 185, 200	GND		Ground
53, 60	V_{DDA}		Analog Power Supply for DENC D/A Converters
54, 61	V_{SSA}		Analog Ground for DENC D/A Converters
48	V_{DDA_PCM}		Analog Power Supply for PLL PCM
49	V_REF_PCM		Analog Reference for PLL PCM
50	V_{SSA_PCM}		Analog Ground for PLL PCM
FRONT-END INTERFACE			
36	B_DATA	I	I^2S Data (DVD) or PARA_DATA[2] (DVD//) or Link Data (DVB/DSS)
40	B_WCLK	I/O	I^2S Word Clock or PARA_DATA[6] (DVD//) or NRSS_CLK (DVB/DSS)
37	B_BCLK	I	I^2S Bit Clock (DVD) or PARA_DATA[3] (DVD//) or Link Bit Clock (DVB/DSS)
38	B_FLAG	I	Error Flag (DVD) or PARA_DATA [4] (DVD//) or Link Sync (DVB/DSS)
39	B_SYNC	I	Sector / Abs Time Sync (DVD) or PARA_DATA[5] (DVD//) or Link Not Valid (DVB/DSS)
42	B_V4	I	Versatile Input Pin (Subcode Input) or PARA_DATA[7] (DVD//) or NRSS_IN (DVB/DSS)
VIDEO OUTPUT INTERFACE			
57	R_OUT	O	Red Output
56	G_OUT	O	Green Output
55	B_OUT	O	Blue Output
63	C_OUT	O	Chroma Output
64	CV_OUT	O	Composite Video Output
62	Y_OUT	O	Luma Output
59	I_REF_DAC_RGB	I	DAC Current Reference
66	I_REF_DAC_YCC	I	DAC Current Reference
58	V_REF_DAC_RGB	I	DAC Voltage Reference
65	V_REF_DAC_YCC	I	DAC Voltage Reference
117	OSD_ACTIVE	I/O	OSD Active
118	PIXCLK_27MHz	I	System Clock Input
51	$\overline{\text{HSYNC}}$	I/O	Horizontal Sync
52	ODD/EVEN	I/O	Vertical Sync
AC-3/MPEG1-2 AUDIO OUTPUT INTERFACE			
43	SCLK	O	Serial Bit Clock
44	PCM_OUT0	O	Audio Serial Output Data 0
24	PCM_OUT1	O	Audio Serial Output Data 1
21	PCM_OUT2	O	Audio Serial Output Data 2
45	PCM_CLK	I/O	PCM Clock In or Out
46	LRCLK	O	Left/Right Clock
47	SPDIF_OUT	O	SPDIF Output

STi5505 (Rev. Ax)

II - PIN DESCRIPTION (continued)

II.2 - Pin List (continued)

Pin	Name	Type	Function
EXTERNAL INTERRUPTS			
23, 25	IRQ[0:1]	I	External Interrupts
PROGRAMMABLE I/O AND ALTERNATE FUNCTION (see Device Configuration Chapter)			
15	PIO0 [0]	I/O	General Purpose I/O or PARA_SYNC (DVD//Front End) or Sc1Data (Smart Card 1 Data I/O)
16	PIO0 [3]	I/O	General Purpose I/O or PARA_REQ (DVD//Front End) or Sc1Clk (Smart Card 1 Clock)
17	PIO0 [4]	I/O	General Purpose I/O or PARA_STR (DVD//Front End) or Sc1RST (Smart Card 1 Reset)
20	PIO0 [5]	I/O	General Purpose I/O or PARA_DATA[0] (DVD//Front End) or Sc1Cmd V_{CC} (Smart Card 1 Voltage Enable)
21	PIO0 [6]	I/O	General Purpose IO or Sc1DataDir (Smart Card 1 Dir)
22	PIO0 [7]	I/O	General Purpose I/O or PARA_DATA[1] (DVD//Front End) or Sc1Detect(Smart Card 1 Detect)
9	PIO1 [0]	I/O	General Purpose I/O or I^2C Data
10	PIO1 [2]	I/O	General Purpose I/O or I^2C Clock
198, 199	PIO1 [3:4]	I/O	General Purpose IO
11	PIO1 [5]	I/O	General Purpose IO or ASC1 TXD
12	PIO1 [6]	I/O	General Purpose IO or ASC1 RXD
13	PIO1 [7]	I/O	General Purpose IO or ASC3 TXD
3	PIO2 [0]	I/O	General Purpose I/O or Sc0Data (Smart Card 0 Data I/O)
5	PIO2 [3]	I/O	General Purpose I/O or Sc0Clk (Smart Card 0 Clock)
6	PIO2 [4]	I/O	General Purpose I/O or Sc0RST (Smart Card 0 Reset)
7	PIO2 [5]	I/O	General Purpose I/O or Sc0CmdV$_{CC}$ (Smart Card 0 Voltage Enable)
8	PIO2 [7]	I/O	General Purpose I/O or Sc0Detect (Smart Card 0 Detect)
201	PIO3 [0]	I/O	General Purpose IO or OSLink In
202	PIO3 [1]	I/O	General Purpose IO or OSLink Out
203	PIO3 [2]	I/O	General Purpose IO or CPUReset
204	PIO3 [3]	I/O	General Purpose IO or CPU Analyse
205	PIO3 [4]	I/O	General Purpose IO or ErrorOut
206, 207, 2	PIO3 [5:7]	I/O	General Purpose IO
191-197	PIO4 [0:6]	I/O	General Purpose IO
14	PIO4 [7]	I/O	General Purpose IO or ASC3 RXD
JTAG INTERFACE			
188	TCK	I	Test Clock
186	TDI	I	Test Data Input
189	TDO	O	Test Data Input
187	TMS	I	Test Mode Select
190	$\overline{\text{TRST}}$	I	Test Reset
SYSTEM USE			
28	PWM2	O	PWM2 Output
27	PWM1/BOOTFROMROM	O/I	PWM1 Output or Configuration Oslink Pins
26	PWM0/OSLINK_SEL	O/I	PWM0 Output or Boot from ROM during Reset
29	$\overline{\text{RST}}$	I	Reset
116	AUXCLK	O	Auxilary Clock for Any Purpose

II - PIN DESCRIPTION (continued)

II.2 - Pin List (continued)

Pin	Name	Type	Function
SDRAM INTERFACE			
78-81, 69, 70-74, 82, 83	AD[0:11]	O	SDRAM Address Bus
92-94, 97-101, 106-109, 112-115	DQ[0:15]	I/O	SDRAM Data (Lower Byte)
84, 85	SDCS[0:1]	O	SDRAM Chip Selects
89	SDCAS	O	SDRAM CAS
88	SDRAS	O	SDRAM RAS
90	SDWE	O	SDRAM Write Enable
104	MEMCLKIN	I	SDRAM Memory Clock Input
76	MEMCLKOUT	O	SDRAM Memory Clock Output
91	DQML	O	DQ Mask Enable (Lower)
105	DQMU	O	DQ Mask Enable (Upper)
EXTERNAL MEMORY INTERFACE			
161-170, 173-183	ADR[1:21]	I/O	External Memory Address Bus
141-148, 151-158	DATA[0:15]	I/O	External Memory Data Bus
128	RAS1/HOLDREQ	O	DRAM RAS or reserved
136	WAIT/READY	I/O	External Wait States or Reserved
133	R/W/DMAACK	I/O	DRAM R/W Strobe or Reserved
121, 122	BE[0:1]	O	Byte enable
129	CAS0/HOLDACK	O/I	DRAM CAS or Reserved
132	CAS1/DMAREQ	O	DRAM CAS or Reserved
124-126	CE[1:3]	O	Chip Select for Banks 1 - 3
135	CS	I	Reserved
137	PROCCLK	I/O	ST20 Clock or Reserved
127	RAS0/CE0	O	DRAM RAS or Chip Select for Bank 0
134	DMAXFER	I	Reserved
138	PPC_MODE	I	Reserved
123	OE	I/O	Output Enable or Reserved
SDAV/P1394 INTERFACE			
30	TEST1	I/O	DATA_RX/STROBE_TX (SDAV Mode) or SDAV_CLK (P1394 Mode)
31	TEST2	I/O	STROBE_RX/DATA_TX (SDAV Mode) or DATA_IN/DATA_OUT (P1394 Mode)
32	TEST3	I/O	Direction (SDAV Mode) or DATA_VALID In/Out(P1394 Mode)
MISCELLANEOUS			
41	TEST5	O	NRSS_OUT (DVB/DSS)

STi5505 (Rev. Ax)

III - FUNCTIONAL DESCRIPTION

III.1 - Functional Modules

Figure 1 shows the subsystem modules that make up the STi5505. These modules are outlined below.

III.1 - CPU

The Central Processing Unit (CPU) on the STi5505 is the ST20-C2 32-bit processor core. It contains instruction processing logic, instruction and data pointers and an operand register. It directly accesses the high speed on-chip SRAM memory, which can store data or programs, and uses the Caches to reduce access time to off chip program and data memory.

The processor can access memory via the general purpose External Memory Interface (EMI) or via the SDRAM EMI which is shared with the MPEG decoder.

III.2 - Memory Subsystem

The STi5505 on-chip SRAM memory system provides 160 Mbytes/s internal data bandwidth, supporting pipelined 2 cycles internal memory access at 25ns cycle times. The STi5505 memory system consists of 2 Kbytes of SRAM, 2Kbytes of instruction cache, a 2Kbytes data cache that can be programmed to be SRAM, and an external memory interface (EMI).

The STi5505 product has 2 Kbytes of on-chip SRAM. The advantage of this is the ability b store time critical code on chip, for instance interrupt routines, software kernels or device drivers, and even frequently used data without these being flushed from the caches.

The instruction and data caches are direct mapped with a write-back system for the data cache and support burst accesses to the external memories for refill and write-back which are effective for increasing performance with page-mode and SDRAM memories.

The STi5505 EMI controls access to the external memory and peripherals while the SDRAM EMI provides access to the SDRAM buffer for the MPEG decoders, ST20 and DMA peripherals.

The STi5505 EMI can access a 16 Mbytes (or greater if DRAM is used) physical address space in each of the four general purpose memory banks, and provides sustained transfer rates of up to 80 Mbytes/s. Peripherals that support an asynchronous data acknowledge are supported as is an external Power PC which can share the bus with the STi5505 and access the SDRAM buffer through the device.

High memory bandwidths up to 200 Mbytes/s can be supported by the SDRAM EMI.

The STi5505 internal memory interconnect provides buffering and arbitration of memory access requests to sustain very high throughput of memory accesses.

III.3 - Syste m Services Module

The STi5505 system services module includes :

- Phase locked loop (PLL) - accepts 27MHz input and generates all the internal high frequency clocks needed for the CPU and the OS-Link.
- test access port - JTAG compatible.
- Diagnostics controller accessed via the JTAG port providing :
- Bootstrapping during development
- Hardware breakpoint and watchpoint
- Real time trace
- External LSA triggering support.

III.4 - Serial Communications

To facilitate the connection of this system the front end device and other peripherals, two UARTs (ASCs) are included in the device. The UARTs provide an asynchronous serial interface.

The UART can be programmed to support a range of baud rates and data formats, for example, data size, stop bits and parity. Two synchronous serial communications (SSC) interfaces are provided on the device. These can be used for a remote control device for example via an I^2C or SPI bus.

III.5 - Interrupt Subsystem

The STi5505 interrupt subsystem supports eight prioritized interrupt levels. Two external interrupt pins are provided. Level assignment logic allows any of the internal or external interrupts to be assigned and, if necessary, share any interrupt level.

III.6 - Front End Interf ace & DVD Decryption

The front end interface accepts sectors in the case of DVD, MPEG-1 system stream in the case of VCD and PCM data for CD-DA applications on an I2S interface. In the case of VCD and CD-DA disks the subcode information is input via a simple asynchronous serial interface similar to a UART.

The bitstream and subcode stream then pass through a "sector processor" block which handles sector filtering in the case of DVD and sectorizing using the subcode stream for VCD and CD-DA systems.

III - FUNCTIONAL DESCRIPTION (continued)

The block also handles overspeed processing for all systems. The capturing of CD-DA sectors is based on a flywheel tiner to improve robusters by concealing erros in the subcode stream. For DVD the data, having had sector headers removed, then passes through a DVD conformant de-cryption stage and is written into any of the system memories using a programmable DMA engine. When a subcode stream is present it is locally buffered, by subcode block and can be read by the CPU for subsequent processing, if required.

III.7 - PWM and counter module

This unit includes three separate pulse width modulator (PWM) generators using a shared counter, and three timer compare and capture channels sharing a second counter.

The counters can be clocked from a pre-scaled internal clock or from a pre-scaled external clock via the capture clock input and the event on which the timer value is captured is also programmable.

The PWM counters are 8-bit with 8-bit registers to set the output high time. The capture/compare counter and the compare and capture registers are 32-bit.

III.8 - Parallel Programmable IO module

40 bits of parallel I/O are provided. 34 of then are connected to actual PIO pins. Each bit is programmable as an output or an input. The output can be configured as a totem pole or open drain driver. Input compare logic is provided which can generate an interrupt on any change on any input bit.

Many pins of the STi5505 device are multi-function and can either be configured as PIO or connected to an internal peripheral signal.

III.9 - MPEG Video decoder

The video decoder is a real-time video compression processor supporting the MPEG-1 and MPEG-2 standards at video rates up to 720 x 480 x 60 Hz and 720 x 576 x 50 Hz. Picture format conversion for display is performed by vertical and horizontal filters. User-defined bitmaps may be superimposed on the display picture through use of the on-screen display function.

III.10 - PAL/NTSC encoder

The digital encoder which is integrated in the STi5505 converts a multiplexed 4:2:2 YUV stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. The encoder can also perform closed-caption, CGMS or teletext encoding and allows Macrovision™ 7.01/6.1 copy protection.

III.11 - MPEG-2 Audio / Dolby AC-3 Decoder

The audio decoder is a Dolby AC-3 decoder capable of decoding both 5.1 and 2 channel DVD comformant bitstreams. The decoder also handles MPEG-1 (layers 1 & 2) and MPEG-2 layer 2 (6 channels). Downmix to 2 channels is possible for Dolby and MPEG standards with optional pro-logic encoding.

The decoder directly accepts MPEG-2 PES streams as input. The decoder is capable of supporting IEC6958-IEC61937 formatted outputs for AC-3 and MPEG audio, linear PCM (left & right,16, 18, 20 & 24 bits), zero output (Mute mode) and PCM audio.

9.9.5 IC7302: FLASH

FLASH AM39LV160DT

GENERAL DESCRIPTION

The Am29LV160D is a 16 Mbit, 3.0 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The device is offered in 48-ball FBGA, 44-pin SO, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. A 12.0 V V_{PP} or 5.0 V_{CC} are not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 70, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The Am29LV160D is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

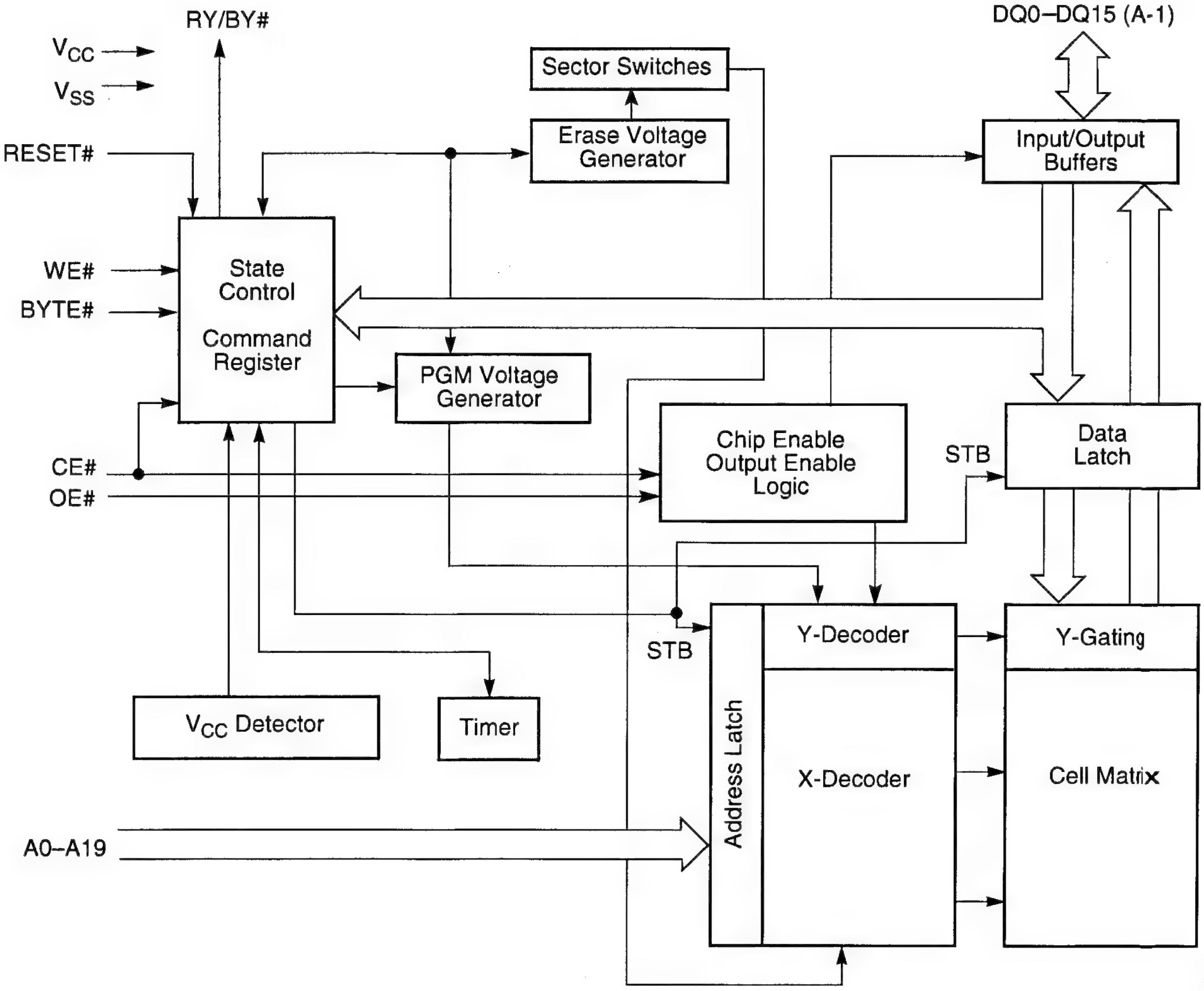
The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

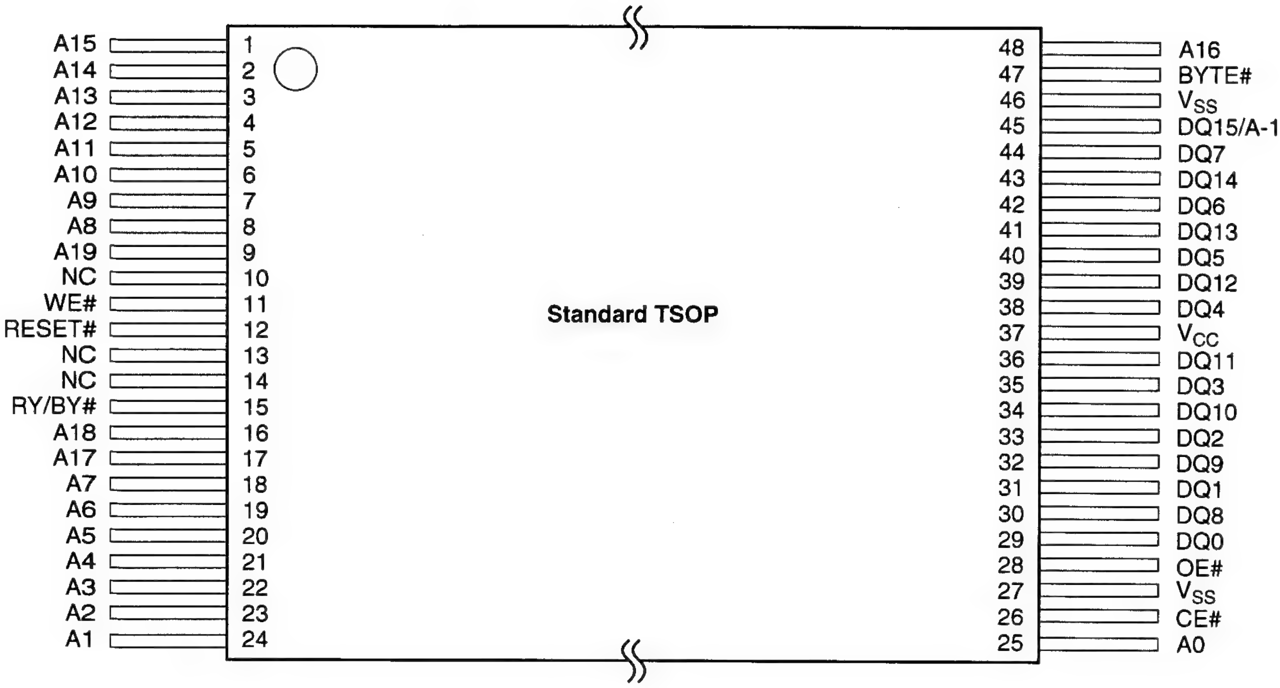
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

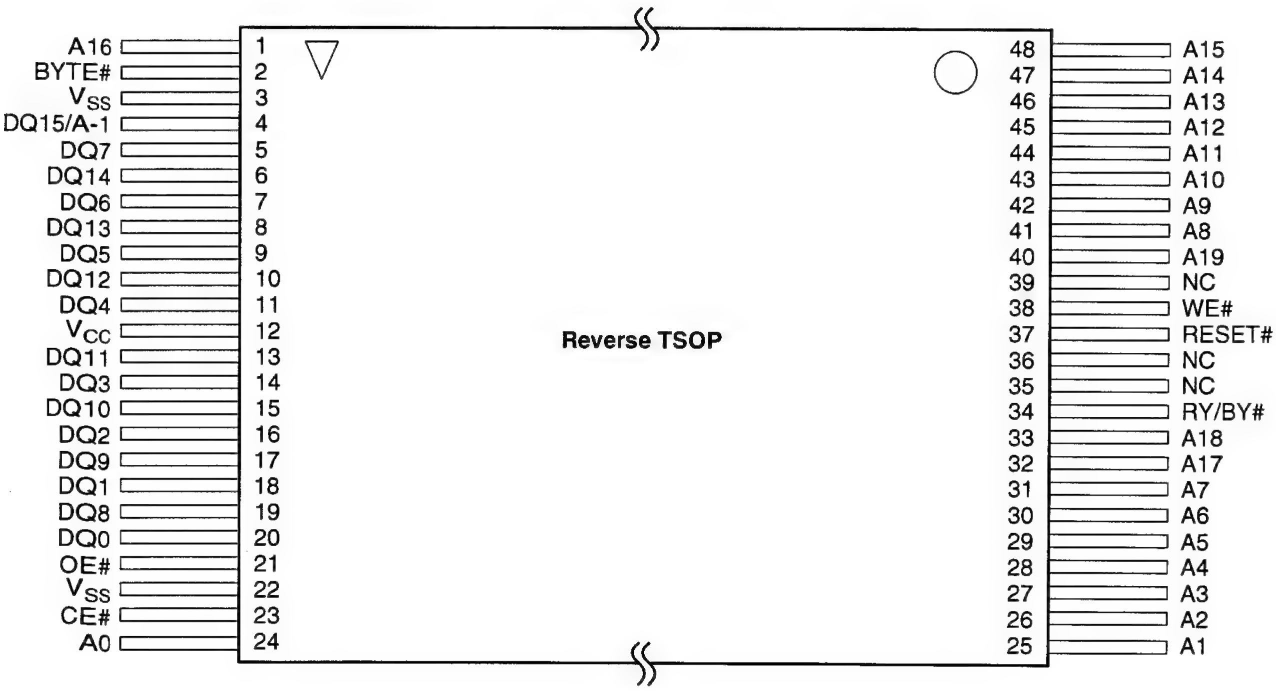
BLOCK DIAGRAM



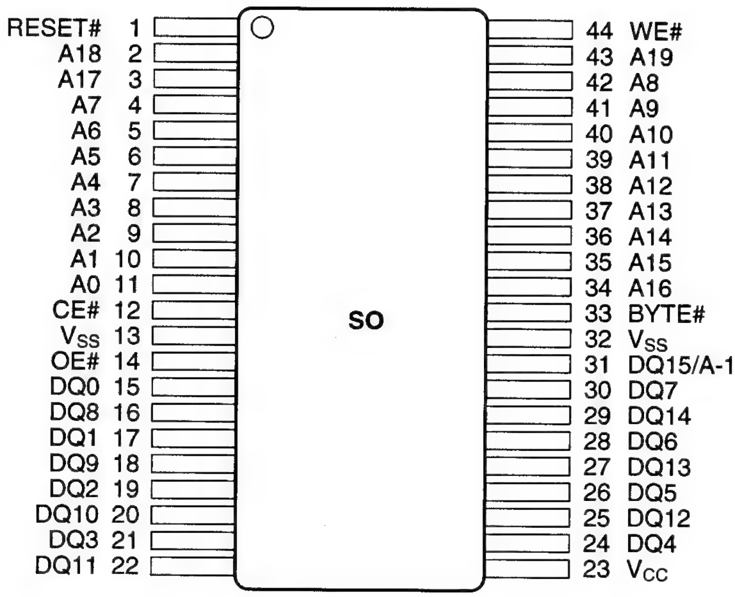
22358A-1

CONNECTION DIAGRAMS





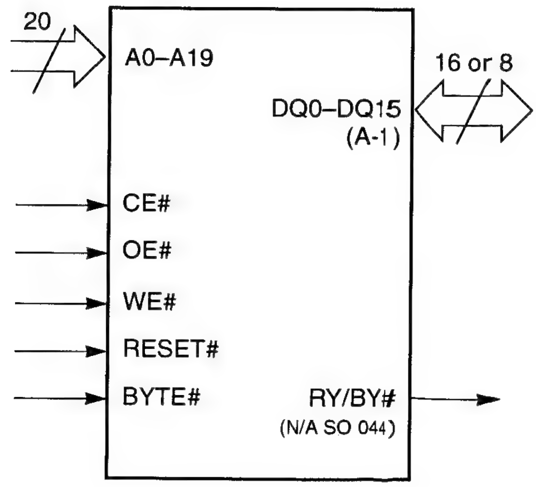
CONNECTION DIAGRAMS



PIN CONFIGURATION

A0–A19	=	20 addresses
DQ0–DQ14	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin
RY/BY#	=	Ready/Busy output (N/A SO 044)
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL



9.9.6 IC7300; IC7400; IC7403: DRAM

GM71VS18163CL

Description

The GM71V(S)18163C/CL is the new generation dynamic RAM organized 1,048,576 x 16 bit. GM71V(S)18163C/CL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71V(S)18163C/CL offers Extended Data out(EDO) Mode as a high speed access mode. Multiplexed address inputs permit the GM71V(S)18163C/CL to be packaged in standard 400 mil 42pin plastic SOJ, and standard 400mil 44(50)pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

Features

* 1,048,576Words x 16 Bit Organization
* Extended Data Out Mode Capability
* Single Power Supply (3.3V+/-0.3V)
* Fast Access Time & Cycle Time

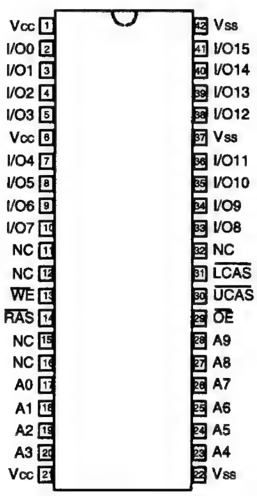
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
GM71V(S)18163C/CL-5	50	13	84	20
GM71V(S)18163C/CL-6	60	15	104	25
GM71V(S)18163C/CL-7	70	18	124	30

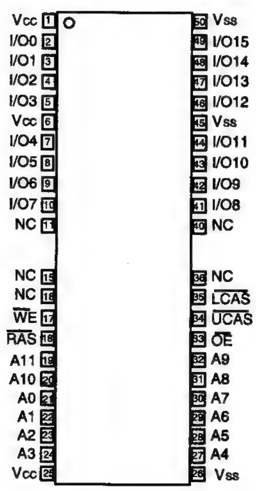
* Low Power
  Active : 684/612/540mW (MAX)
  Standby : 7.2mW (CMOS level : MAX)
  0.83mW (L-version : MAX)
* $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
* All inputs and outputs TTL Compatible
* 1024 Refresh Cycles/16ms
* 1024 Refresh Cycles/128ms (L-version)
* Self Refresh Operation (L-version)
* Battery Back Up Operation (L-version)
* 2 $\overline{CAS}$ byte Control

Pin Configuration

42SOJ



44(50)TSOP II



(Top View)

Pin Description

Pin	Function	Pin	Function
A0-A9	Address Inputs	$\overline{WE}$	Read/Write Enable
A0-A9	Refresh Address Inputs	$\overline{OE}$	Output Enable
I/O0-I/O15	Data-In/Out	V_{CC}	Power (+3.3V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{UCAS}$, $\overline{LCAS}$	Column Address Strobe	NC	No Connection

9.9.7 IC7410: SAA6750 (EMPIRE)

EMPIRE (SAA6750H)

1 FEATURES

- Digital YUV input according to *"ITU-T 601"* and to *"ITU-T 656"*
- NTSC and PAL (720 pixel × 480 lines at 60 Hz and 720 pixel × 576 lines at 50 Hz)
- Integrated colour conversion 4 : 2 : 2 to 4 : 2 : 0
- Integrated format conversion to SIF format (optional)
- Real time MPEG2 Simple Profile at Main Level (SP@ML) encoding
- IP frame or I frame only encoding supported
- Programmable Group Of Pictures (GOP) size
- Integrated motion estimation, half pixel accuracy, search range 128 × 128 pixels
- Motion compensated noise reduction
- Elementary stream data output compliant to MPEG2 standard (*"ISO 13818-2"*)
- Constant Bit-Rate (CBR) and Variable Bit-Rate (VBR) supported
- Bitstream output compatible to 16-bit parallel interface with Motorola (68xxx like) or Intel (xxx86 like) protocol style
- Adaptable to dedicated applications by embedded software
- Standard software package available (refer to software specification)
- No external host processor required
- High speed real time port for processor co-processor applications
- Only 4 × 4 Mbit external DRAM required
- I²C-bus controlled
- Single external video clock 27 MHz
- Power supply 3.3 V
- Digital inputs 5 V tolerant
- Boundary Scan Test (BST) supported.

2 GENERAL DESCRIPTION

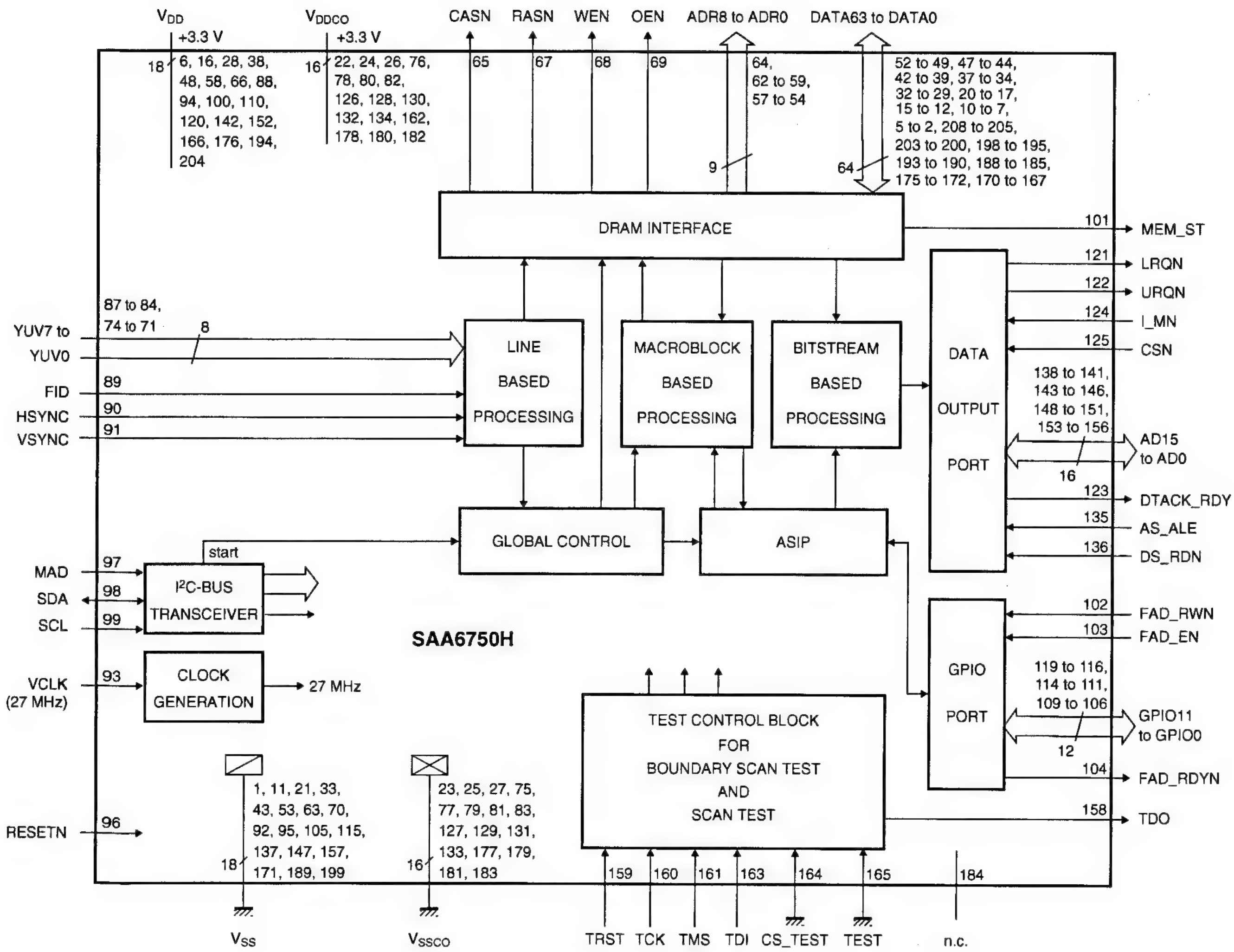
2.1 General

The SAA6750H is a new approach towards a stand-alone MPEG2 video encoder IC. It combines high quality SP at ML compliant real time encoding with cost-effectiveness, allowing for the first time the use of an MPEG2 encoder IC in applications and markets with a high cost pressure. This has been achieved by means of a number of innovations in architecture and algorithms developed by the Philips Research Laboratories. E.g.:

- The unique motion estimation algorithm supports highly efficient encoding by using only I frame and IP frame mode. B frames need not be used. This leads to a significantly smaller internal circuitry and also reduces DRAM memory requirements from at least 4 to 2 Mbyte. In addition, the absence of B frames simplifies editing of the compressed data stream.
- The patented, motion-compensated temporal noise filtering which was developed by Philips for professional equipment reduces noise in the input video before compression is performed. This technique gives visible improvements in picture quality, especially in the field of home recordings with noisy signal sources where this has proved to be of significant benefit.

Internally the SAA6750H uses a hardware solution for data compression and a specially developed high performance processor for control purposes. This programmable embedded Digital Signal Processor (DSP) approach allows Philips to tailor various customized sets of functions for this IC. Contact Philips for information on available software packages.

Blockdiagram



Block diagram.

Pin Description

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
V_{SS}	1	ground	–	ground for pad ring
DATA28	2	input/output	3	DRAM data interface bit 28
DATA29	3	input/output	3	DRAM data interface bit 29
DATA30	4	input/output	3	DRAM data interface bit 30
DATA31	5	input/output	3	DRAM data interface bit 31
V_{DD}	6	supply	–	supply voltage for pad ring
DATA32	7	input/output	3	DRAM data interface bit 32
DATA33	8	input/output	3	DRAM data interface bit 33
DATA34	9	input/output	3	DRAM data interface bit 34
DATA35	10	input/output	3	DRAM data interface bit 35
V_{SS}	11	ground	–	ground for pad ring
DATA36	12	input/output	3	DRAM data interface bit 36
DATA37	13	input/output	3	DRAM data interface bit 37
DATA38	14	input/output	3	DRAM data interface bit 38
DATA39	15	input/output	3	DRAM data interface bit 39
V_{DD}	16	supply	–	supply voltage for pad ring
DATA40	17	input/output	3	DRAM data interface bit 40
DATA41	18	input/output	3	DRAM data interface bit 41
DATA42	19	input/output	3	DRAM data interface bit 42
DATA43	20	input/output	3	DRAM data interface bit 43
V_{SS}	21	ground	–	ground for pad ring
V_{DDCO}	22	supply	–	supply voltage for core logic
V_{SSCO}	23	ground	–	ground for core logic
V_{DDCO}	24	supply	–	supply voltage for core logic
V_{SSCO}	25	ground	–	ground for core logic
V_{DDCO}	26	supply	–	supply voltage for core logic
V_{SSCO}	27	ground	–	ground for core logic
V_{DD}	28	supply	–	supply voltage for pad ring
DATA44	29	input/output	3	DRAM data interface bit 44
DATA45	30	input/output	3	DRAM data interface bit 45
DATA46	31	input/output	3	DRAM data interface bit 46
DATA47	32	input/output	3	DRAM data interface bit 47
V_{SS}	33	ground	–	ground for pad ring
DATA48	34	input/output	3	DRAM data interface bit 48
DATA49	35	input/output	3	DRAM data interface bit 49
DATA50	36	input/output	3	DRAM data interface bit 50
DATA51	37	input/output	3	DRAM data interface bit 51
V_{DD}	38	supply	–	supply voltage for pad ring
DATA52	39	input/output	3	DRAM data interface bit 52

SYMBOL	PIN	INPUT/OUTPUT[1]	I_{max} (mA)	DESCRIPTION
DATA53	40	input/output	3	DRAM data interface bit 53
DATA54	41	input/output	3	DRAM data interface bit 54
DATA55	42	input/output	3	DRAM data interface bit 55
V_{SS}	43	ground	–	ground for pad ring
DATA56	44	input/output	3	DRAM data interface bit 56
DATA57	45	input/output	3	DRAM data interface bit 57
DATA58	46	input/output	3	DRAM data interface bit 58
DATA59	47	input/output	3	DRAM data interface bit 59
V_{DD}	48	supply	–	supply voltage for pad ring
DATA60	49	input/output	3	DRAM data interface bit 60
DATA61	50	input/output	3	DRAM data interface bit 61
DATA62	51	input/output	3	DRAM data interface bit 62
DATA63	52	input/output	3	DRAM data interface bit 63 (MSB)
V_{SS}	53	ground	–	ground for pad ring
ADR0	54	output/3-state	3	DRAM address interface bit 0 (LSB)
ADR1	55	output/3-state	3	DRAM address interface bit 1
ADR2	56	output/3-state	3	DRAM address interface bit 2
ADR3	57	output/3-state	3	DRAM address interface bit 3
V_{DD}	58	supply	–	supply voltage for pad ring
ADR4	59	output/3-state	3	DRAM address interface bit 4
ADR5	60	output/3-state	3	DRAM address interface bit 5
ADR6	61	output/3-state	3	DRAM address interface bit 6
ADR7	62	output/3-state	3	DRAM address interface bit 7
V_{SS}	63	ground	–	ground for pad ring
ADR8	64	output/3-state	3	DRAM address interface bit 8 (MSB)
CASN	65	output/3-state	6	DRAM column address strobe (active LOW)
V_{DD}	66	supply	–	supply voltage for pad ring
RASN	67	output/3-state	3	DRAM row address strobe (active LOW)
WEN	68	output/3-state	3	DRAM write enable (active LOW)
OEN	69	output/3-state	3	DRAM chip select (active LOW)
V_{SS}	70	ground	–	ground for pad ring
YUV0	71	input	–	video input signal bit 0 (LSB)
YUV1	72	input	–	video input signal bit 1
YUV2	73	input	–	video input signal bit 2
YUV3	74	input	–	video input signal bit 3
V_{SSCO}	75	ground	–	ground for core logic
V_{DDCO}	76	supply	–	supply voltage for core logic
V_{SSCO}	77	ground	–	ground for core logic
V_{DDCO}	78	supply	–	supply voltage for core logic
V_{SSCO}	79	ground	–	ground for core logic

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
V_{DDCO}	80	supply	–	supply voltage for core logic
V_{SSCO}	81	ground	–	ground for core logic
V_{DDCO}	82	supply	–	supply voltage for core logic
V_{SSCO}	83	ground	–	ground for core logic
YUV4	84	input	–	video input signal bit 4
YUV5	85	input	–	video input signal bit 5
YUV6	86	input	–	video input signal bit 6
YUV7	87	input	–	video input signal bit 7 (MSB)
V_{DD}	88	supply	–	supply voltage for pad ring
FID	89	input	–	odd/even ?eld identi?cation
HSYNC	90	input	–	horizontal reference signal
VSYNC	91	input	–	vertical reference signal
V_{SS}	92	ground	–	ground for pad ring
VCLK	93	input	–	video clock input (27 MHz)
V_{DD}	94	supply	–	supply voltage for pad ring
V_{SS}	95	ground	–	ground for pad ring
RESETN	96	input	–	hard reset input (active LOW)
MAD	97	input	–	module address (I^2C-bus)
SDA	98	input/open drain output	6	serial data input/output (I^2C-bus)
SCL	99	input/open drain output	–	serial clock input (I^2C-bus)
V_{DD}	100	supply	–	supply voltage for pad ring
MEM_ST	101	output/3-state	3	do not use in the application (reserved)
FAD_RWN	102	input	–	ASIP port data read/$\overline{\text{write}}$
FAD_EN	103	input	–	ASIP port data enable
FAD_RDYN	104	open drain output	3	ASIP port data ready (active LOW)
V_{SS}	105	ground	–	ground for pad ring
GPIO0	106	input/output	3	ASIP port data bit 0 (LSB)
GPIO1	107	input/output	3	ASIP port data bit 1
GPIO2	108	input/output	3	ASIP port data bit 2
GPIO3	109	input/output	3	ASIP port data bit 3
V_{DD}	110	supply	–	supply voltage for pad ring
GPIO4	111	input/output	3	ASIP port data bit 4
GPIO5	112	input/output	3	ASIP port data bit 5
GPIO6	113	input/output	3	ASIP port data bit 6
GPIO7	114	input/output	3	ASIP port data bit 7
V_{SS}	115	ground	–	ground for pad ring
GPIO8	116	input/output	3	ASIP port data bit 8
GPIO9	117	input/output	3	ASIP port data bit 9
GPIO10	118	input/output	3	ASIP port data bit 10
GPIO11	119	input/output	3	ASIP port data bit 11 (MSB)

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
V_{DD}	120	supply	–	supply voltage for pad ring
LRQN	121	open drain output	3	output port lower watermark interrupt request (active LOW)
URQN	122	open drain/3-state	3	output port upper watermark interrupt request (active LOW)
DTACK_RDY	123	open drain output	3	output port data transfer acknowledge/ready/request
I_MN	124	input	–	output port Intel/Motorola bus style selection input (active LOW); with internal pull-up resistor
CSN	125	input	–	output port chip select for external address mode (active LOW); with internal pull-up resistor
V_{DDCO}	126	supply	–	supply voltage for core logic
V_{SSCO}	127	ground	–	ground for core logic
V_{DDCO}	128	supply	–	supply voltage for core logic
V_{SSCO}	129	ground	–	ground for core logic
V_{DDCO}	130	supply	–	supply voltage for core logic
V_{SSCO}	131	ground	–	ground for core logic
V_{DDCO}	132	supply	–	supply voltage for core logic
V_{SSCO}	133	ground	–	ground for core logic
V_{DDCO}	134	supply	–	supply voltage for core logic
AS_ALE	135	input	–	output port address strobe/address latch enable
DS_RDN	136	input	–	output port data strobe/$\overline{read}$
V_{SS}	137	ground	–	ground for pad ring
AD15	138	input/output	3	output port multiplexed address/data line bit 15 (MSB)
AD14	139	input/output	3	output port multiplexed address/data line bit 14
AD13	140	input/output	3	output port multiplexed address/data line bit 13
AD12	141	input/output	3	output port multiplexed address/data line bit 12
V_{DD}	142	supply	–	supply voltage for pad ring
AD11	143	input/output	3	output port multiplexed address/data line bit 11
AD10	144	input/output	3	output port multiplexed address/data line bit 10
AD9	145	input/output	3	output port multiplexed address/data line bit 9
AD8	146	input/output	3	output port multiplexed address/data line bit 8
V_{SS}	147	ground	–	ground for pad ring
AD7	148	input/output	3	output port multiplexed address/data line bit 7/data bus bit 7 (MSB)
AD6	149	input/output	3	output port multiplexed address/data line bit 6/data bus bit 6
AD5	150	input/output	3	output port multiplexed address/data line bit 5/data bus bit 5
AD4	151	input/output	3	output port multiplexed address/data line bit 4/data bus bit 4
V_{DD}	152	supply	–	supply voltage for pad ring
AD3	153	input/output	3	output port multiplexed address/data line bit 3/data bus bit 3
AD2	154	input/output	3	output port multiplexed address/data line bit 2/data bus bit 2
AD1	155	input/output	3	output port multiplexed address/data line bit 1/data bus bit 1
AD0	156	input/output	3	output port multiplexed address/data line bit 0 (LSB)/data bus bit 0 (LSB)

SYMBOL	PIN	INPUT/OUTPUT[1]	I_{max} (mA)	DESCRIPTION
V_{SS}	157	ground	–	ground for pad ring
TDO	158	output	3	boundary scan test data output; pin not active during normal operation; with 3-state output; note 2
TRST	159	input	–	boundary scan test reset; pin must be set to LOW for normal operation; with internal pull-up resistor; notes 2 and 3
TCK	160	input	–	boundary scan test clock; pin must be set to LOW during normal operation; with internal pull-up resistor; note 2
TMS	161	input	–	boundary scan test mode select; pin must ?oat or set to HIGH during normal operation; with internal pull-up resistor; note 2
V_{DDCO}	162	supply	–	supply voltage for core logic
TDI	163	input	–	boundary scan test data input; pin must ?oat or set to HIGH during normal operation; with internal pull-up resistor; note 2
CS_TEST	164	input	–	test mode for the internal RAMs; pin must be set to LOW during normal operation
TEST	165	input	–	test mode; pin must be set to LOW during normal operation
V_{DD}	166	supply	–	supply voltage for pad ring
DATA0	167	input/output	3	DRAM data interface bit 0 (LSB)
DATA1	168	input/output	3	DRAM data interface bit 1
DATA2	169	input/output	3	DRAM data interface bit 2
DATA3	170	input/output	3	DRAM data interface bit 3
V_{SS}	171	ground	–	ground for pad ring
DATA4	172	input/output	3	DRAM data interface bit 4
DATA5	173	input/output	3	DRAM data interface bit 5
DATA6	174	input/output	3	DRAM data interface bit 6
DATA7	175	input/output	3	DRAM data interface bit 7
V_{DD}	176	supply	–	supply voltage for pad ring
V_{SSCO}	177	ground	–	ground for core logic
V_{DDCO}	178	supply	–	supply voltage for core logic
V_{SSCO}	179	ground	–	ground for core logic
V_{DDCO}	180	supply	–	supply voltage for core logic
V_{SSCO}	181	ground	–	ground for core logic
V_{DDCO}	182	supply	–	supply voltage for core logic
V_{SSCO}	183	ground	–	ground for core logic
n.c.	184	–	–	reserved pin; do not connect
DATA8	185	input/output	3	DRAM data interface bit 8
DATA9	186	input/output	3	DRAM data interface bit 9
DATA10	187	input/output	3	DRAM data interface bit 10
DATA11	188	input/output	3	DRAM data interface bit 11
V_{SS}	189	ground	–	ground for pad ring
DATA12	190	input/output	3	DRAM data interface bit 12
DATA13	191	input/output	3	DRAM data interface bit 13

SYMBOL	PIN	INPUT/OUTPUT[1]	I_{max} (mA)	DESCRIPTION
DATA14	192	input/output	3	DRAM data interface bit 14
DATA15	193	input/output	3	DRAM data interface bit 15
V_{DD}	194	supply	–	supply voltage for pad ring
DATA16	195	input/output	3	DRAM data interface bit 16
DATA17	196	input/output	3	DRAM data interface bit 17
DATA18	197	input/output	3	DRAM data interface bit 18
DATA19	198	input/output	3	DRAM data interface bit 19
V_{SS}	199	ground	–	ground for pad ring
DATA20	200	input/output	3	DRAM data interface bit 20
DATA21	201	input/output	3	DRAM data interface bit 21
DATA22	202	input/output	3	DRAM data interface bit 22
DATA23	203	input/output	3	DRAM data interface bit 23
V_{DD}	204	supply	–	supply voltage for pad ring
DATA24	205	input/output	3	DRAM data interface bit 24
DATA25	206	input/output	3	DRAM data interface bit 25
DATA26	207	input/output	3	DRAM data interface bit 26
DATA27	208	input/output	3	DRAM data interface bit 27

Notes

1. All input, I/O (in input mode), output (in 3-state mode) and open drain output pins are 5.0 V tolerant.
2. In accordance with the *"IEEE 1149.1"* standard.
3. Special functionality of pin TRST:
   a) For board designs without boundary scan implementation, pin TRST must be connected to ground.
   b) Pin TRST provides easy initialization of the internal BST circuit. By applying a LOW it can be used to force the internal Test Access Port (TAP) controller to the Test-Logic-Reset state (normal operation) at once.

The 208 pins are divided in following groups:

Video input port (11 pins):

8 data pins

3 control pins.

Data output port (23 pins):

16 data pins

7 control pins.

GPIO port (15 pins):

12 data pins

3 control pins.

DRAM (77 pins):

64 data pins

9 address pins

4 control pins.

Others (14 pins):

1 video clock input pin

3 pins related to the I^2C-bus

1 pin for reset control

7 pins for test purposes

1 pin not connected

1 pin for internal test purposes.

Supply (68 pins):

16 core supply pins

18 I/O cell supply pins

16 core ground pins

18 I/O cell ground pins.

9.9.8 IC7552: SAA7118 (VIP)

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter, Component Video Input, VBI-Data Slicer and High Performance Scaler

SAA7118

1 FEATURES

The SAA7118 is a video capture device for application at the image port of VGA controller, with following feature high lights:

Video Acquisition/ Clock

Up to sixteen analog CVBS, split as desired (All of the CVBS inputs optionally can be used to convert VSB signals)

Up to eight analog Y+C inputs, split as desired

Up to four analog component inputs, with embedded or separate sync, split as desired

Four on-chip anti-aliasing filters in front of the ADC's

Automatic Clamp Control (ACC) for CVBS, Y and C (or VSB) and component signal

Switchable white Peak Control

Four 9 Bit Low Noise CMOS analog-to-digital converters at two-fold ITU-656 oversampling (27 MHz)

Digitized CVBS or Y+C-signals are available on the expansion port

Fully programmable static gain or automatic gain control, matching to the particular signal properties

On-Chip Line Locked Clock Generation according ITU601

Requires only one crystal (32.11 or 24.576 MHz) for all standards

Horizontal and vertical Sync Detection

Video Decoder

Digital PLL for Synchronization and Clock Generation from all Standards and Non- Standard Video Sources e.g. consumer grade VTR

Digital PLL for Synchronization and Clock Generation from all Standards and Non- Standard Video Sources e.g. consumer grade VTR

Automatic detection of any supported colour standard

Luminance and chrominance signal processing for PAL BGDHIN, Combination-PAL N, PAL M, NTSC M, NTSC-Japan, NTSC 4.43 and SECAM

Adaptive 2/4-line comb filter for two dimensional chrominance/luminance-separation, also with VTR signals

- Increased Luminance and Chrominance Bandwidth for all PAL and NTSC-standards
- Reduced cross colour and cross luminance artefacts

PAL delay line for correcting PAL phase errors

Brightness Contrast Saturation (BCS)- adjustment, separately for composite and baseband signals

User programmable sharpness control

Fast Blanking between component inputs and a CVBS input through a dedicated pin

Detection of copy-protected signals acc. to the Macrovision standard, indicating level of protection

Independent Gain and Offset - adjustment for raw data path

Component Video Processing

Synchronous Component Video (RGB) input via fast blanking, YCbCr input

Digital matrix

Video Scaler

Horizontal and Vertical Down-Scaling and Up-Scaling to randomly sized windows

Horizontal and Vertical Scaling range: variable zoom to 1/64 (icon)
(Note: H and V zoom are restricted by the transfer data rates)

Anti-Alias- and Accumulating Filter for Horizontal Scaling

Vertical Scaling with Linear Phase Interpolation and Accumulating Filter for Anti-Aliasing (6 bit phase accuracy)

Horizontal Phase Correct Up- and Down-Scaling for improved signal quality of scaled data, especially for compression and video phone applications, with 6 bit phase accuracy (1.2 nsec step width)

Two independent programming sets for scaler part, to define two "ranges" per field or sequences over frames

Fieldwise switching between Decoder-part and Expansion port (X-port) input

Brightness, contrast and saturation controls for scaled outputs

VBI-Data Decoder and Slicer

versatile VBI-data decoder, slicer, clock regeneration and byte synchronization

e.g. for WST, NABST, Close Caption, WSS, etc.

Audio Clock Generation

Generation of a field locked Audio Master Clock to support a constant number of audio clocks per video field

Generation of an audio serial and left/right (channel) clock signal

Digital I/O Interfaces

Real Time signal port (R - port), incl. continuous line locked reference clock and real time status information supporting RTC level 3.1 (refer to external document "RTC Functional Specification" for details)

Bidirectional Expansion Port (X - port) with half duplex functionality (D1), 8-bit YCbCr

- output from Decoder part, real time and unscaled, or
- input to Scaler part, e.g. video from MPEG-decoder (extension to 16 bit possible)

Video Image port (I - port) configurable for 8 - bit data (extension to 16 bit possible) in Master Mode (own clock), or Slave Mode (external clock), with auxiliary timing and hand shake signals

Discontinuous data streams supported

32-word * 4 Byte FIFO register for video output data

28-word * 4 Byte FIFO register for decoded VBI output data

Scaled 4:2:2, 4:1:1, *4:2:0, 4:1:0* YCbCr output

Scaled 8-bit luminance only and raw CVBS data output

sliced, decoded VBI data output

Miscellaneous

Power On Control

5 V tolerant digital inputs and I/O ports

Software controlled power saving stand-by modes supported

Programming via serial I^{2}C-bus, full read-back ability by an external controller, bit rate up to 400 kbit/s

Boundary Scan Test circuit complies to the IEEE Std. 1149.b1 -1994

BGA156 package

2 APPLICATIONS

Multimedia

Digital Television

Image Processing

Video Phone

PC- Editing cards

PC- Tuner cards

3 GENERAL DESCRIPTION

Philips X-VIP is a new Multistandard Comb Filter Video Decoder chip with additional component processing, providing high quality, optionally scaled, video.

The SAA7118 is a combination of a four channel analog preprocessing circuit including source selection, anti-aliasing filter and A/D-converter, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a Digital Multi Standard Decoder containing two-dimensional chrominance/luminance separation by an adaptive comb filter and a high performance scaler, including variable horizontal and vertical up and down scaling and a Brightness- Contrast- Saturation- Control circuit.

It is a highly integrated circuit for Desktop Video and similar applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into ITU-601 compatible colour component values. The SAA7118 accepts as analog inputs CVBS or S-Video (Y+C) from TV or VCR sources, including weak and distorted signals, as well as baseband component signals YCbCr or RGB. An expansion port (X-port) for digital video (bi-directional half duplex, D1 compatible) is also supported to connect to MPEG or video phone codec. At the so called image port (I-port) the 7118 supports 8 (16) bit wide output data with auxiliary reference data for interfacing to VGA controllers.

The target application for SAA7118 is to capture and optionally scale video images, to be provided as digital video stream through the image port of a VGA controller, for capture to system memory, or just to provide digital baseband video to any picture improvement processing.

SAA7118 also provides means for capturing the serially coded data in the vertical blanking interval (VBI-data). Two principal functions are available:
- to capture raw video samples, after interpolation to the required output data rate, via the scaler and
- a versatile data slicer (data recovery) unit.

SAA7118 incorporates also a field locked audio clock generation. This function ensures that there is always the same number of audio samples associated with a field, or a set of fields. This prevents the loss of sychronization between video and audio, during capture or playback.

All of the A/D- converters may be used to digitize a VSB signal for further for further decoding; a dedicated output port and a selectable VSB clock input is provided.

The circuit is controlled via I^{2}C-bus (full write / read capability for all programming registers, bit rate up to 400 kbits/s)

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter, Component Video Input, VBI-Data Slicer and High Performance Scaler — SAA7118

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DDx}	digital supply voltage	3.0	3.3	3.6	V
V_{DDCx}	digital core supply voltage	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	3.1	3.3	3.5	V
T_{amb}	ambient temperature	0	-	70	°C
P_{A+D}	analog and digital power dissipation(1)	-	t.b.d.	-	W

Note

1. Power consumption is measured in CVBS-input mode (only one ADC active) and 8 bit image port output mode, expansion port is tristated

5 ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7118	156	BGA156	Plastic	SOT 472-1(BB3)

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter, Component Video Input, VBI-Data Slicer and High Performance Scaler

SAA7118

6 SYSTEM BLOCK DIAGRAM

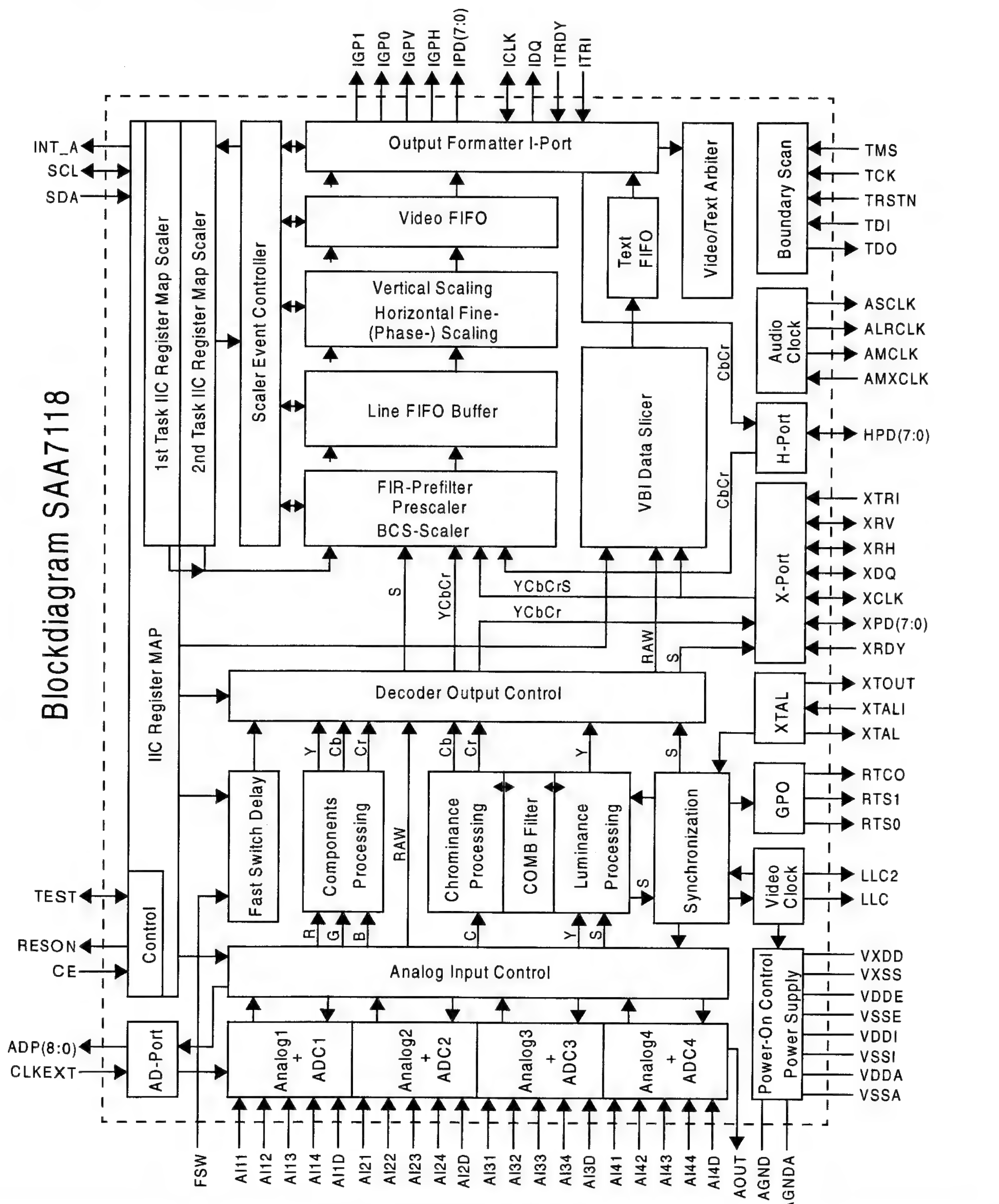


Fig.1 Blockdiagram SAA7118

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter, Component Video Input, VBI-Data Slicer and High Performance Scaler — SAA7118

7 PINNING AND CONFIGURATION

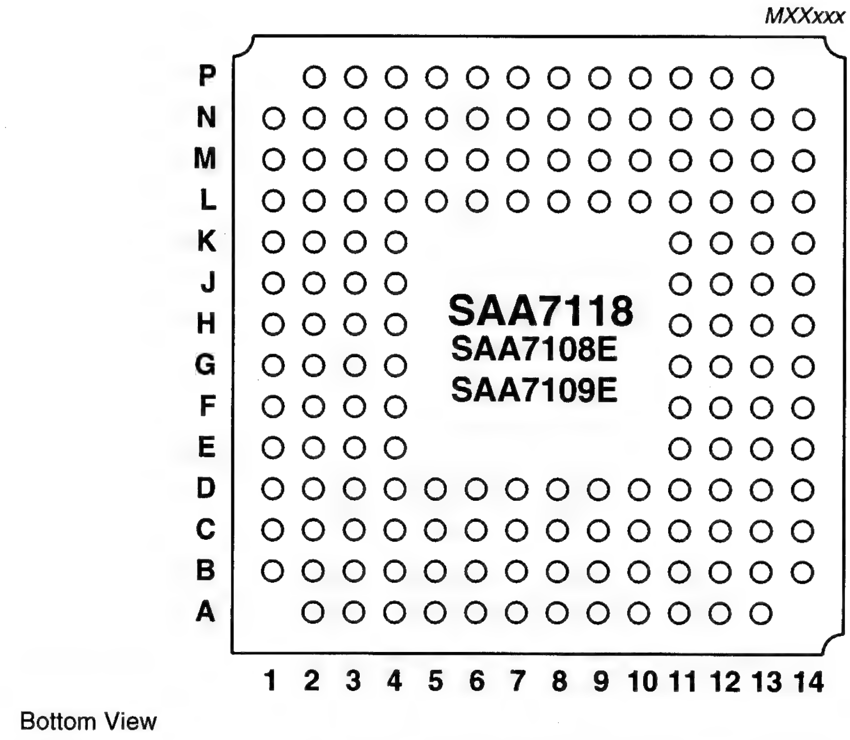


Fig.2 Package/Pinning SAA7118

7.1 Pinning List

Table 1 Pinning List SAA7118

PIN	NAME	TYPE	DESCRIPTION
A02	XTOUT	O	Crystal oscillator output signal
A03	XTAL	O	Connect output pin for quartz
A04	VXSS	P	Ground for crystal oscillator
A05	TDO	O	Test Data Output for Boundary Scan Test (2)
A06	XRDY	O	Status flag or ready signal from scaler
A07	XCLK	I/O	Clock I/O expansion port
A08	XPD0	I/O	LSB of expansion port bus
A09	XPD2	I/O	MSB-5 of expansion port bus
A10	XPD4	I/O	MSB-3 of expansion port bus
A11	XPD6	I/O	MSB-1 of expansion port bus
A12	TEST5	I/pu	Scan test input; do not connect
A13	TEST3	I/pu	Scan test input; do not connect
B01	AI41	I	Analog input #41
B02	RES1	O	Reserved pin for future extensions or testing, do not connect
B03	VXDD	P	Supply for crystal oscillator

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter, Component Video Input, VBI-Data Slicer and High Performance Scaler

SAA7118

PIN	NAME	TYPE	DESCRIPTION
B04	XTALI	I	Connect input pin for quartz
B05	TDI	I/pu	Test Data Input for Boundary Scan Test (with internal pull-up) (2)
B06	TCK	I/pu	Test Clock for Boundary Scan Test (with internal pull-up) (2)
B07	XDQ	I/O	Data qualifier for expansion port
B08	XPD1	I/O	MSB-6 of expansion port bus
B09	XPD3	I/O	MSB-4 of expansion port bus
B10	XPD5	I/O	MSB-2 of expansion port bus
B11	XTRI	I	X-port output control signal; effects (XPD[7:0], XRH, XRV, XDQ and XCLK)
B12	TEST4	O	Scan test output; do not connect
B13	RES2	NC	Reserved pin for future extensions or testing, do not connect
B14	RES3	NC	Reserved pin for future extensions or testing, do not connect
C01	VSSA4	P	Ground for analog input AI4x
C02	AGND	P	Analog Signal Ground
C03	RES4	NC	Reserved pin for future extensions or testing, do not connect
C04	RES5	NC	Reserved pin for future extensions or testing, do not connect
C05	VDDE1	P	Digital supply peripheral cells
C06	TRSTN	I/pu	Test ReSeT Not for Boundary Scan Test (with internal pull-up) (1)
C07	XRH	I/O	Horizontal reference expansion-port
C08	VDDI1	P	Digital supply core
C09	VDDE2	P	Digital supply peripheral cells
C10	VDDI2	P	Digital supply core
C11	XPD7	I/O	MSB of expansion port bus
C12	RES6	NC	Reserved pin for future extensions or testing, do not connect
C13	RES7	NC	Reserved pin for future extensions or testing, do not connect
C14	TEST2	I/pu	Scan test input; do not connect
D01	AI43	I	Analog input #43
D02	AI42	I	Analog input #42
D03	AI4D	I/O	Differential input for AI4x
D04	VDDA4	P	Supply for analog input AI4x
D05	VSSE1	P	Digital ground peripheral cells
D06	TMS	I/pu	Test Mode Select for Boundary Scan Test or Scan Test (with internal pull-up) (2)
D07	VSSI1	P	Digital ground core (Substrate connection)
D08	XRV	I/O	Vertical reference for expansion-port
D09	VSSE2	P	Digital ground peripheral cells
D10	VSSI2	P	Digital ground core
D11	VSSE3	P	Digital ground peripheral cells
D12	VDDE3	P	Digital supply peripheral cells
D13	TEST1	I/pu	Scan test input; do not connect
D14	HPD0	I/O	LSB of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
E01	AI44	I	Analog input #44

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter, Component Video Input, VBI-Data Slicer and High Performance Scaler SAA7118

PIN	NAME	TYPE	DESCRIPTION
E02	VDDA4A	P	Supply for analog input AI4x
E03	AI31	I	Analog input #31
E04	VSSA3	P	Ground for analog input AI3x
E11	HPD1	I/O	MSB-6 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
E12	HPD3	I/O	MSB-4 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
E13	HPD2	I/O	MSB-5 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
E14	HPD4	I/O	MSB-3 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
F01	AI3D	I/O	Differential input for AI3x
F02	AI32	I	Analog input #32
F03	AI33	I	Analog input #33
F04	VDDA3	P	Supply for analog input AI3x
F11	VSSI3	P	Digital ground core
F12	VDDI3	P	Digital supply core
F13	HPD5	I/O	MSB-2 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
F14	HPD6	I/O	MSB-1 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
G01	AI34	I	Analog input #34
G02	VDDA3A	P	Supply for analog input AI3x
G03	AI22	I	Analog input #22
G04	AI21	I	Analog input #21
G11	VSSE4	P	Digital ground peripheral cells
G12	IPD1	O	MSB-6 of Image port bus
G13	HPD7	I/O	MSB of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
G14	IPD0	O	LSB of Image port bus
H01	AI2D	I/O	Differential input for AI2x
H02	AI23	I	Analog input #23
H03	VSSA2	P	Ground for analog input AI2x
H04	VDDA2	P	Supply for analog input AI2x
H11	IPD2	O	MSB-5 of Image port bus
H12	VDDE4	P	Digital supply peripheral cells
H13	IPD4	O	MSB-3 of Image port bus
H14	IPD3	O	MSB-4 of Image port bus
J01	VDDA2A	P	Supply for analog input AI2x
J02	AI11	I	Analog input #11
J03	AI24	I	Analog input #24
J04	VSSA1	P	Ground for analog input AI1x

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter, Component Video Input, VBI-Data Slicer and High Performance Scaler

SAA7118

PIN	NAME	TYPE	DESCRIPTION
J11	VSSI4	P	Digital ground core
J12	VDDI4	P	Digital supply core
J13	IPD6	O	MSB-1 of Image port bus
J14	IPD5	O	MSB-2 of Image port bus
K01	AI12	I	Analog input #12
K02	AI13	I	Analog input #13
K03	AI1D	I/O	Differential input for AI1x
K04	VDDA1	P	Supply for analog input AI1x
K11	IPD7	O	MSB of Image port bus
K12	IGPH	O	Multi purpose horizontal reference signal
K13	IGP1	O	General purpose signal #1
K14	IGPV	O	Multi purpose vertical reference signal
L01	VDDA1A	P	Supply for analog input AI1x
L02	AGNDA	P	Analog signal ground connection
L03	AI14	I	Analog input #14
L04	VSSE5	P	Digital ground peripheral cells
L05	VSSI5	P	Digital ground core
L06	ADP6	O	MSB-2 of Direct A/D-converted output bus (VSB)
L07	ADP3	O	MSB-5 of Direct A/D-converted output bus (VSB)
L08	VSSE6	P	Digital ground peripheral cells
L09	VSSI6	P	Digital ground core
L10	RTCO	O/st/pd (3)	RTC output; strap to LOW (4k7) for first I^2C slave address 42h strap to HIGH (4k7) for second I^2C slave address 40h
L11	VSSE7	P	Digital ground peripheral cells
L12	ITRI	I/O	Image-port control signal, effects all Image port pins
L13	IDQ	O	Data qualifier for image port
L14	IGP0	O	General purpose signal #0
M01	AOUT	O	Analog test output (not for use in application)
M02	VSSA0	P	Ground for internal clock generator
M03	VDDA0	P	Supply for internal clock generator
M04	VDDE5	P	Digital supply peripheral cells
M05	VDDI5	P	Digital supply core
M06	ADP7	O	MSB-1 of Direct A/D-converted output bus (VSB)
M07	ADP2	O	MSB-6 of Direct A/D-converted output bus (VSB)
M08	VDDE6	P	Digital supply peripheral cells
M09	VDDI6	P	Digital supply core
M10	RTS0	O	Real time status or sync information
M11	VDDE7	P	Digital supply peripheral cells
M12	AMXCLK	I	Audio Master External clock input

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter, Component Video Input, VBI-Data Slicer and High Performance Scaler SAA7118

PIN	NAME	TYPE	DESCRIPTION
M13	FSW	I/pd	Fast Switch (Blanking), with internal pull-down, inserts component inputs into CVBS signal
M14	ICLK	I/O	Clock output signal for image-port, LCLK of LPB image port mode, or optional asynchronous backend clock input
N01	RES8	NC	Reserved pin for future extensions or testing, do not connect
N02	RES9	I/pu	Reserved pin for future extensions or testing, do not connect
N03	RES10	I/pd	Reserved pin for future extensions or testing, do not connect
N04	CE	I/pu	Chip Enable or Reset with internal pull-up
N05	LLC2	O	Line-locked clock at half frequency (13.5 MHz nominal)
N06	CLKEXT	I	External clock input intended for A/D-conversion of VSB signals (36 MHz)
N07	ADP5	O	MSB-3 of Direct A/D-converted output bus (VSB)
N08	ADP0	O	LSB of Direct A/D-converted output bus (VSB)
N09	SCL	I	I^2C Serial Clock
N10	RTS1	O	Real time status or sync information
N11	ASCLK	O	Audio serial clock
N12	ITRDY	I	Target Ready for image port bus
N13	RES11	NC	Reserved pin for future extensions or testing, do not connect
N14	RES12	NC	Reserved pin for future extensions or testing, do not connect
P02	RES13	I/O	Reserved pin for future extensions or testing, do not connect
P03	EXMCLR	I/pd	External Mode Clear, with internal pull-down
P04	LLC	O	Line-locked clock (27 MHz nominal)
P05	RESON	O	Reset Output Not signal
P06	ADP8	O	MSB of Direct A/D-converted output bus (VSB)
P07	ADP4	O	MSB-4 of Direct A/D-converted output bus (VSB)
P08	ADP1	O	MSB-7 of Direct A/D-converted output bus (VSB)
P09	INT_A	O/od	I^2C interrupt flag (Low if any enabled status bit has changed)
P10	SDA	I/O/od	I^2C Serial Data
P11	AMCLK	O	Audio Master clock, must be less than half the crystal clock frequency
P12	ALRCLK	O/st/pd	Audio left/right clock, strap to LOW (4k7) for 24.576 MHz crystal strap to HIGH (4k7) for 32.11 MHz crystal (3)
P13	TEST0	I/pu	Scan test input; do not connect
TYPE description: I=input, O=output, P=power, NC=not connected, st=strapping, pu=pull-up, pd=pull-down, od=open drain			

Notes

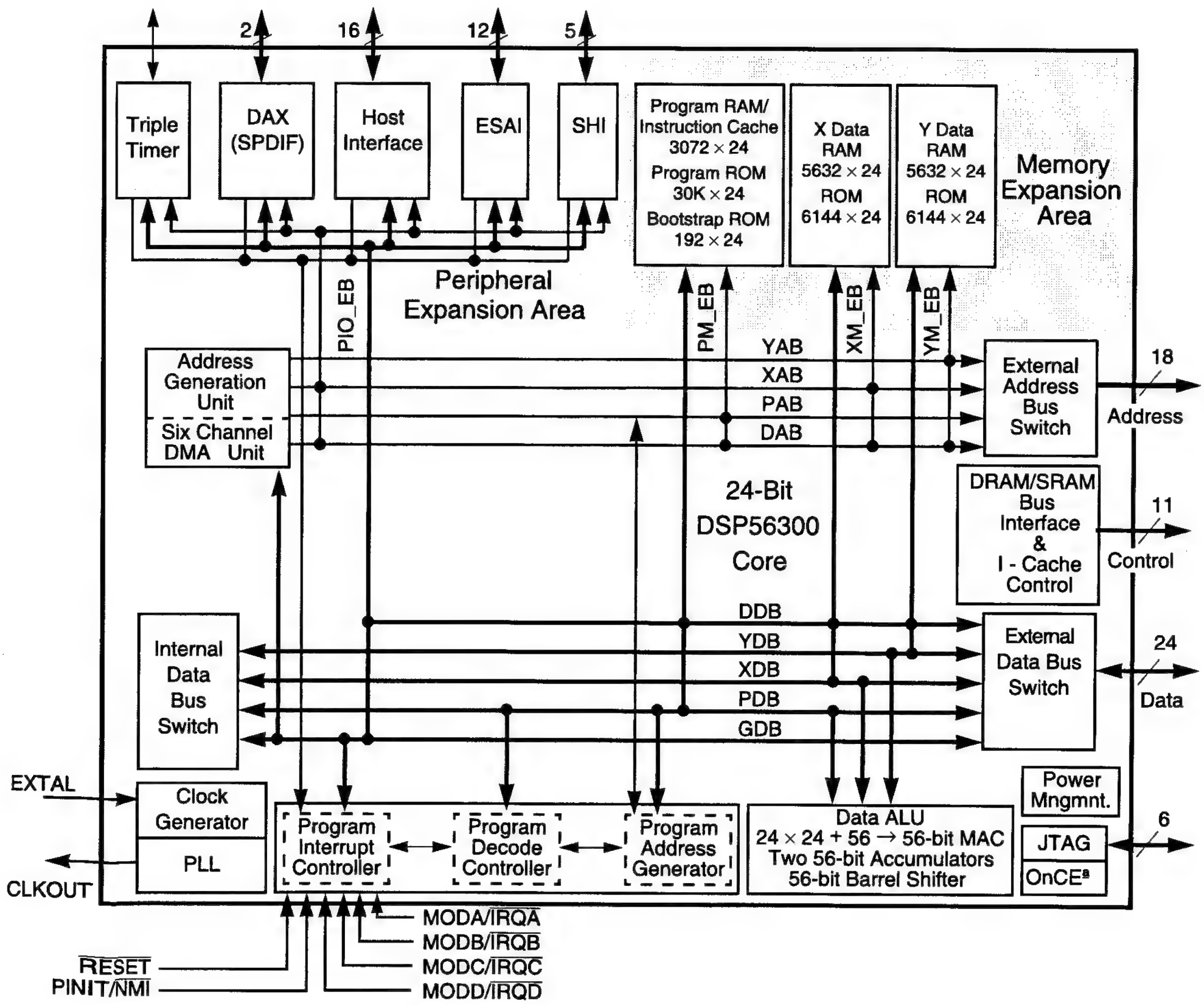
1. This pin provides easy initialization of BST circuitry. TRSTN can be used to force the TAP (Test Access Port) controller to the Test-Logic-Reset state (normal operation) at once
2. According to the IEEE1149.b1-1994 standard the pads TDI and TMS are input pads with a internal pull-up transistor and TDO a tri-state output pad. TCK, TRSTN are also built with internal pile-up
3. Strapping remark: If the strapping pin is unused, the internal pull-down resistor is sufficient for strap function. If pin is used in an application, an external strapping resistor (4,7k) is necessary to get a certain strap function.

9.9.9 IC7703: DSP56362

DSP56362

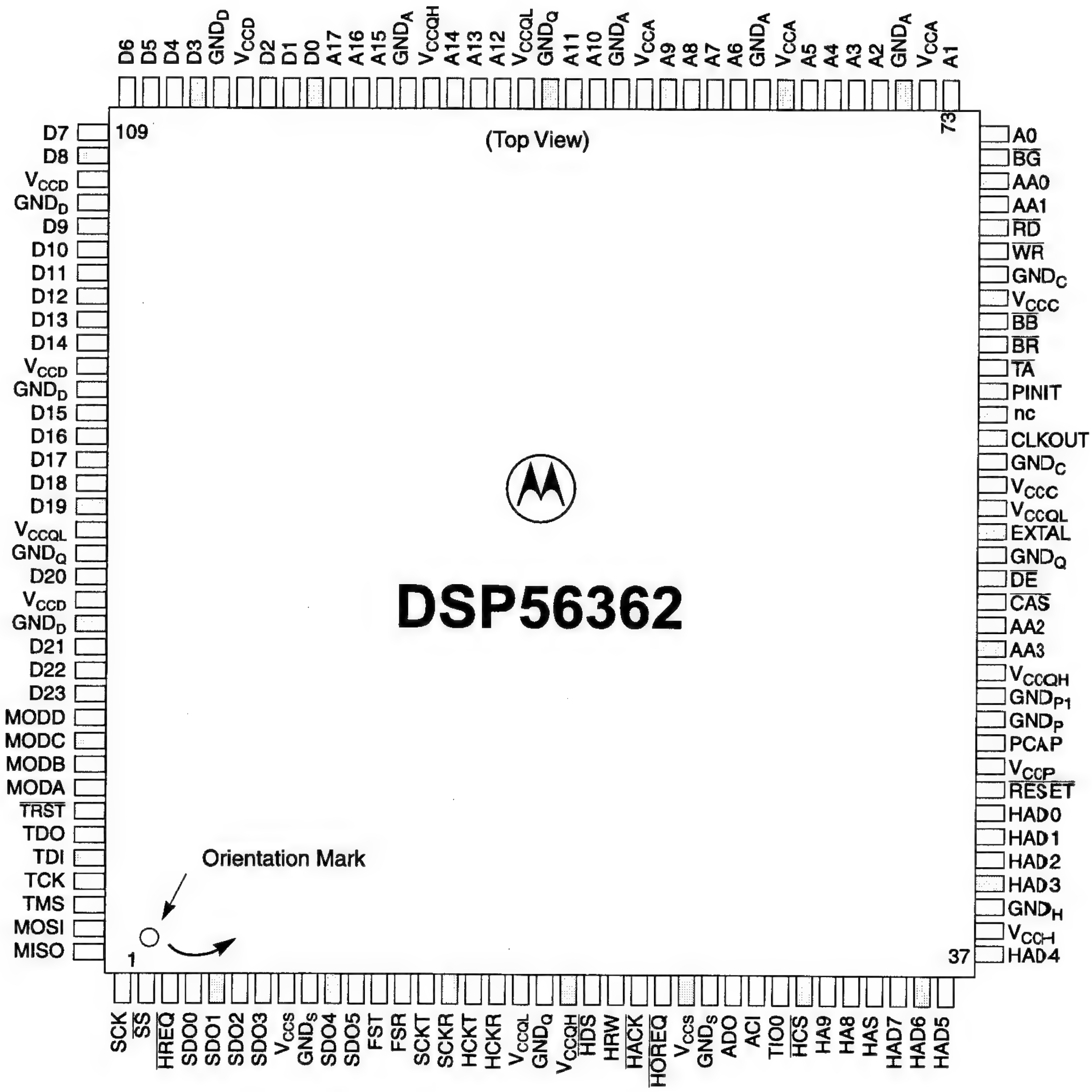
24-BIT AUDIO DIGITAL SIGNAL PROCESSOR

Motorola designed the DSP56362 to support digital audio applications requiring digital audio compression and decompression, sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56362 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Motorola Symphonyª DSP family, as shown in Figure 1. This design provides a two-fold performance increase over MotorolaÕs popular Symphony family of DSPs while retaining code compatibility. Significant architectural enhancements include a barrel shifter, 24-bit addressing, instruction cache, and direct memory access (DMA). The DSP56362 offers 80/100 million instructions per second (MIPS) using an internal 80/100 MHz clock at 3.3 V.



DSP56362 Block Diagram

SIGNAL DESCRIPTION



PIN NUMBER	SIGNAL NAME	TYPE	SIGNAL DESCRIPTION
1	SCK/SCL	I/O	SPI Serial Clock/I^2C Serial Clock
2	SS/HA2	I	SPI Slave Select/I^2C Slave Address 2
3	HREQ	I/O	Host Request
4	SDO0/PC11	I/O	Serial Data Output1/Port C10
5	SDO1/PC10	I/O	Serial Data Output0/Port C11
6	SDO2/SDI3/PC9	I/O	Serial Data Output2/Serial Data Input3/Port C9
7	SDO3/SDI2/PC8	I/O	Serial Data Output3/Serial Data Input2/Port C8
8	V_{CCS}	I	SHI, ESAI, DAX and Timer Power
9	GND_S		SHI, ESAI, DAX and Timer Ground
10	SDO4/SDI1/PC7	I/O	Serial Data Output4/Serial Data Input1/Port C7
11	SDO5/SDI0/PC6	I/O	Serial Data Output5/Serial Data Input0/Port C6
12	FST/PC4	I/O	Frame Sync for Transmitter/Port C4
13	FSR/PC1	I/O	Frame Sync for Receiver/Port C1
14	SCKT/PC3	I/O	Transmitter Serial Clock/Port C3
15	SCKR/PC0	I/O	Receiver Serial Clock/Port C0
16	HCKT/PC5	I/O	High Frequency Clock for Transmitter/Port C5
17	HCKR/PC2	I/O	High Frequency Clock for Receiver/Port C2
18	V_{CCQL}	I	Quiet Core Low Power
19	GND_Q		Quiet Ground
20	V_{CCQH}	I	Quiet External High Power
21	HDS/HWR/PB12	I/O	Host Data Strobe/Host Write Data/Port B12
22	HRW/HRD/PB11	I/O	Host Read Write/Host Read Data/Port B11
23	HACK/HRRQ/PB 15	I/O	Host Acknowledge/Receive Host Request
24	HOREQ/HTRQ/PB 14	I/O	Host Request/Transmit Host Request/Port B14
25	V_{CCS}	I	SHI, ESAI, DAX and Timer Power
26	GND_S		SHI, ESAI, DAX and Timer Ground
27	ADO/PD1	I/O	Digital Audio Data Output/Port D1
28	ACI/PD0	I/O	Audio Clock Input/Port D0
29	TIO0	I/O	Timer 0 Schmitt-Trigger Input/Output
30	HCS/HA10/PB13	I/O	Host Chip Select/Host Address10/Port B13
31	HA2/HA9/PB10	I/O	Host Address Input2/Host Address9/Port B10
32	HA1/HA8/PB9	I/O	Host Address Input1/Host Address8/Port B9
33	HA0/HAS/PB8	I/O	Host Address Input0/Host Address Strobe/Port B8
34	H7/HAD7/PB7	I/O	Host Data7/Host Address7/Port B7
35	H6/HAD6/PB6	I/O	Host Data6/Host Address6/Port B6
36	H5/HAD5/PB5	I/O	Host Data5/Host Address5/Port B5
37	H4/HAD4/PB4	I/O	Host Data4/Host Address4/Port B4
38	V_{CCH}	I	Host Power
39	GND_H		Host Ground
40	H3/HAD3/PB3	I/O	Host Data3/Host Address3/Port B3
41	H2/HAD2/PB2	I/O	Host Data2/Host Address2/Port B2
42	H1/HAD1/PB1	I/O	Host Data1/Host Address1/Port B1
43	H0/HAD0/PB0	I/O	Host Data0/Host Address0/Port B0
44	RESET	I	Reset
45	V_{CCP}	I	PLL Power
46	PCAP	I	PLL Capacitor
47	GND_P		PLL Ground
48	GND_{P1}		PLL Ground 1
49	V_{CCQH}	I	Quiet External High Power
50	AA3/RAS3	O	Address Attribute3/Row Address Strobe 3
51	AA2/RAS2	O	Address Attribute2/Row Address Strobe 2
52	CAS	O	Column Address Strobe
53	DE	I	Debug Event
54	GND_Q		Quiet Ground
55	EXTAL	I	External Clock Input

PIN NUMBER	SIGNAL NAME	TYPE	SIGNAL DESCRIPTION
56	V_{CCQL}	I	Quiet Core Low Power
57	V_{CCC}	I	Bus Control Power
58	GND_C		Bus Control Ground
59	CLKOUT	O	Clock Output
60	NC		Not Connected
61	PINIT/NMI	I	PLL Initial/Nonmaskable Intrrupt
62	TA	I	Transfer Acknowledge
63	BR	O	Bus Request
64	BB	I/O	Bus Busy
65	V_{CCC}	I	Bus Control Power
66	GND_C		Bus Control Power
67	WR	O	Write Enable
68	RD	O	Read Enable
69	AA1/RAS1	O	Address Attribute1/Row Address Strobe 1
70	AA0/RAS0	O	Address Attribute0/Row Address Strobe 0
71	BG	I	Bus Grant
72	A0	O	Address Bus
73	A1	O	Address Bus
74	V_{CCA}	I	Address Bus Power
75	GND_A		Address Bus Ground
76	A2	O	Address Bus
77	A3	O	Address Bus
78	A4	O	Address Bus
79	A5	O	Address Bus
80	V_{CCA}	I	Address Bus Power
81	GND_A		Address Bus Ground
82	A6	O	Address Bus
83	A7	O	Address Bus
84	A8	O	Address Bus
85	A9	O	Address Bus
86	V_{CCA}	I	Address Bus Power
87	GND_A		Address Bus Ground
88	A10	O	Address Bus
89	A11	O	Address Bus
90	GND_Q		Quiet Ground
91	V_{CCQL}	I	Quiet Core Low Power
92	A12	O	Address Bus
93	A13	O	Address Bus
94	A14	O	Address Bus
95	V_{CCQH}	I	Quiet External High Power
96	GND_A		Address Bus Ground
97	A15	O	Address Bus
98	A16	O	Address Bus
99	A17	O	Address Bus
100	D0	I/O	Data Bus
101	D1	I/O	Data Bus
102	D2	I/O	Data Bus
103	V_{CCD}	I	Data Bus Power
104	GND_D		Data Bus Ground
105	D3	I/O	Data Bus
106	D4	I/O	Data Bus
107	D5	I/O	Data Bus
108	D6	I/O	Data Bus
109	D7	I/O	Data Bus
110	D8	I/O	Data Bus

PIN NUMBER	SIGNAL NAME	TYPE	SIGNAL DESCRIPTION
111	V_{CCD}	I	Data Bus Power
112	GND_D		Data Bus Ground
113	D9	I/O	Data Bus
114	D10	I/O	Data Bus
115	D11	I/O	Data Bus
116	D12	I/O	Data Bus
117	D13	I/O	Data Bus
118	D14	I/O	Data Bus
119	V_{CCD}	I	Data Bus Power
120	GND_D		Data Bus Ground
121	D15	I/O	Data Bus
122	D16	I/O	Data Bus
123	D17	I/O	Data Bus
124	D18	I/O	Data Bus
125	D19	I/O	Data Bus
126	V_{CCQL}	I	Quiet Core Low Power
127	GND_Q		Quiet Ground
128	D20	I/O	Data Bus
129	V_{CCD}	I	Data Bus Power
130	GND_D		Data Bus Ground
131	D21	I/O	Data Bus
132	D22	I/O	Data Bus
133	D23	I/O	Data Bus
134	MODD/IRQD	I	Mode Select D/External Interrupt Request D
135	MODC/IRQC	I	Mode Select C/External Interrupt Request C
136	MODB/IRQB	I	Mode Select B/External Interrupt Request B
137	MODA/IRQA	I	Mode Select A/External Interrupt Request A
138	TRST	I	Test Reset
139	TDO	O	Test Data Output
140	TDI	I	Test Data Input
141	TCK	I	Test Clock
142	TMS	I	Test Mode Select
143	MOSI/HA0	I/O	SPI Master-Out-Slave-In/I^2C Slave address 0
144	MISO/SDA		SPI Master-In-Slave-Out/I^2C Data and acknowledge

9.9.10 IC7700: SRAM

CY7C1019V33

Features

- **High speed**
  - **— t_{AA} = 12, 15, 20 ns**
- **V_{CC} = 3.3V ± 10%**
- **Low active power**
  - **— 432 mW (max.)**
  - **— 288 mW (L version)**
- **Low CMOS standby power**
  - **— 18 mW (max.)**
  - **— 7.2 mW (L version)**
- **2.0V Data Retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

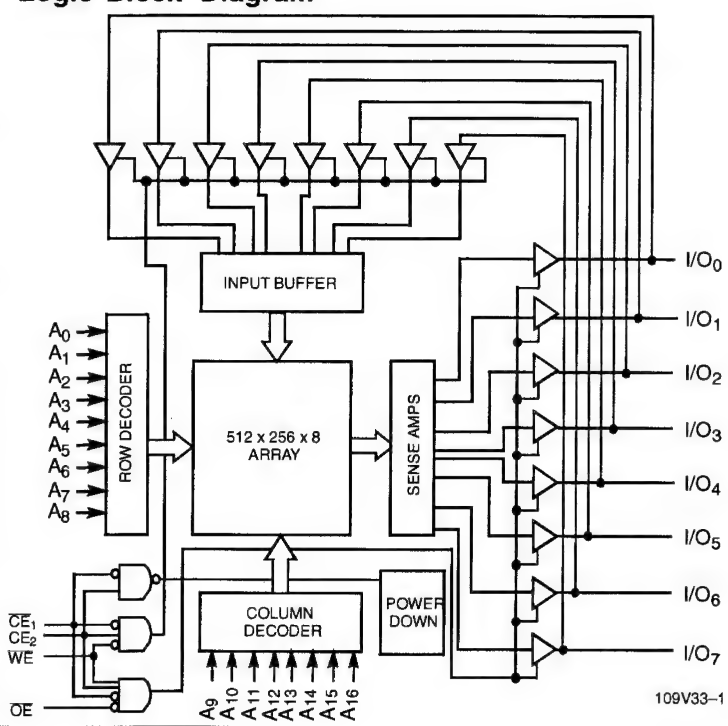
The CY7C109V33/CY7C1009V33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

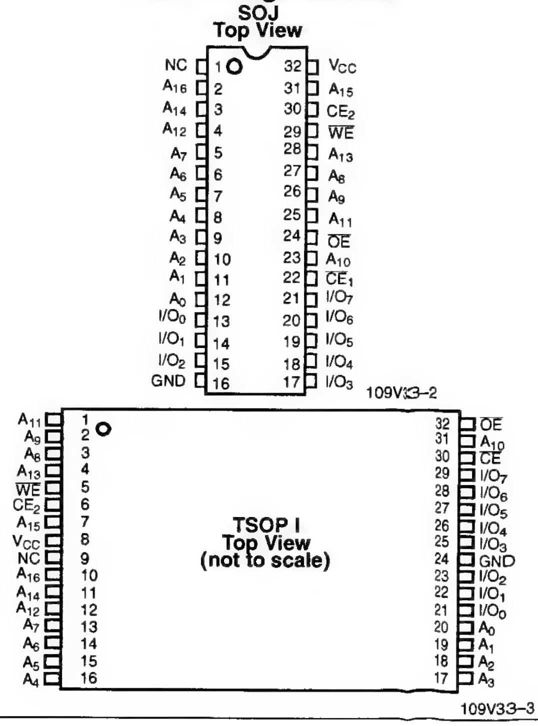
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C109V33 is available in standard 32-pin, 400-mil-wide SOJ package. The CY7C1009V33 is available in a 32-pin, 300-mil-wide SOJ package. The CY7C1009V33 and CY7C109V33 are functionally equivalent in all other respects.

Logic Block Diagram



Pin Configurations



9.10 IC's Divio

9.10.1 IC7101: 58PDI1394P11A

3-port physical layer interface PDI1394P11A

1.0 FEATURES

- 3 cable interface ports
- Supports 100Mb/s and 200Mb/s transfers
- Interfaces to any 1394 standard Link Layer Controller
- 5V tolerant I/Os with Bus Hold Circuitry
- Single 3.3V supply voltage
- Arbitrated (short) Bus Reset (1394a feature)
- Fully compatible with existing 100 Mbps Phys on the market
- Prevents a TpBias voltage driven into a non-powered PDI1394P11A from erroneously powering up the part

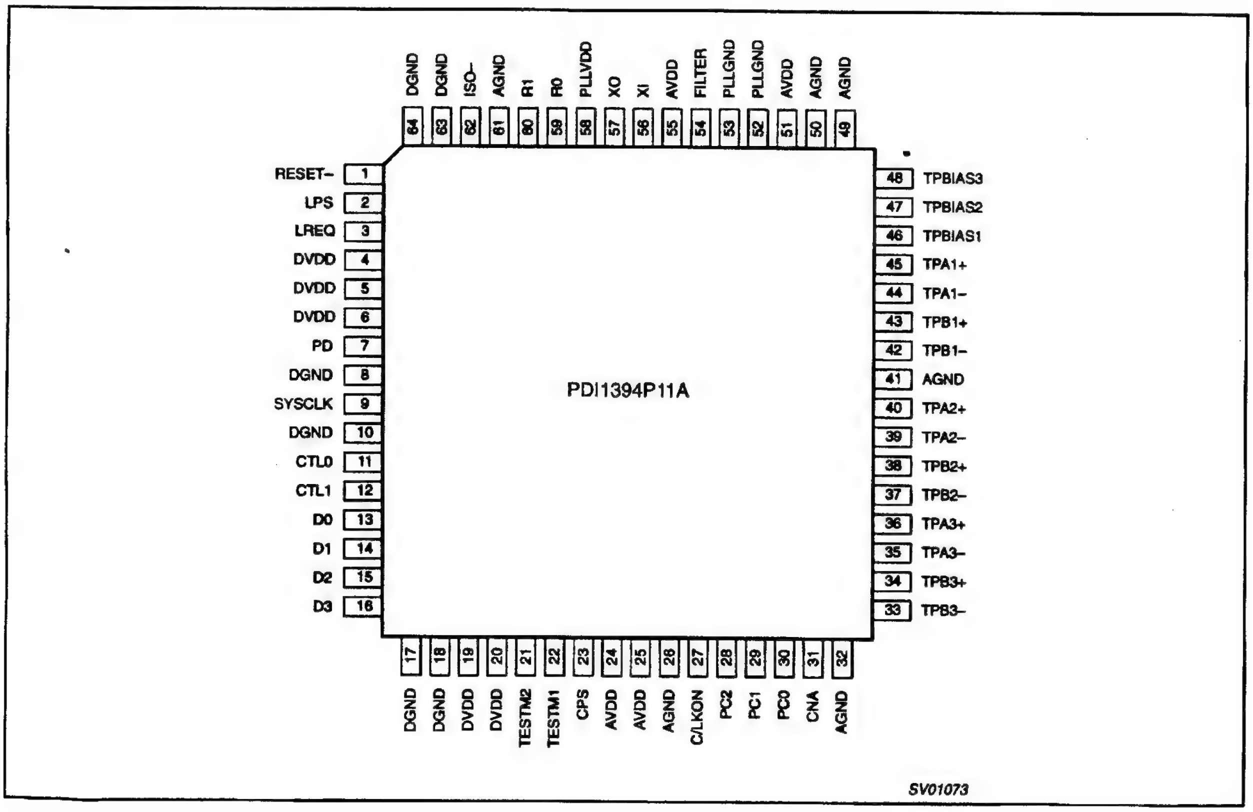
2.0 DESCRIPTION

The Philips Semiconductors PDI1394P11A is an IEEE1394-1995 compliant Physical Layer interface. The PDI1394P11A provides the analog physical layer functions needed to implement a three port node in a cable-based IEEE 1394–1995 network. Additionally, the device manages bus initialization and arbitration cycles, as well as transmission and reception of data bits. The Link Layer Controller interface is compatible with both 3V and 5V Link Controllers. While providing a maximum transmission data rate of 200 Mb/s, the PDI1394P11A is compatible with current 100 Mb/s Physical Layer ICs. The PDI1394P11A is available in the LQFP64 package.

3.0 ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
64-pin plastic LQFP	0°C to +70°C	PDI1394P11A BD	PD1394P11A BD	SOT314-2

4.0 PIN CONFIGURATION



3-port physical layer interface PDI1394P11A

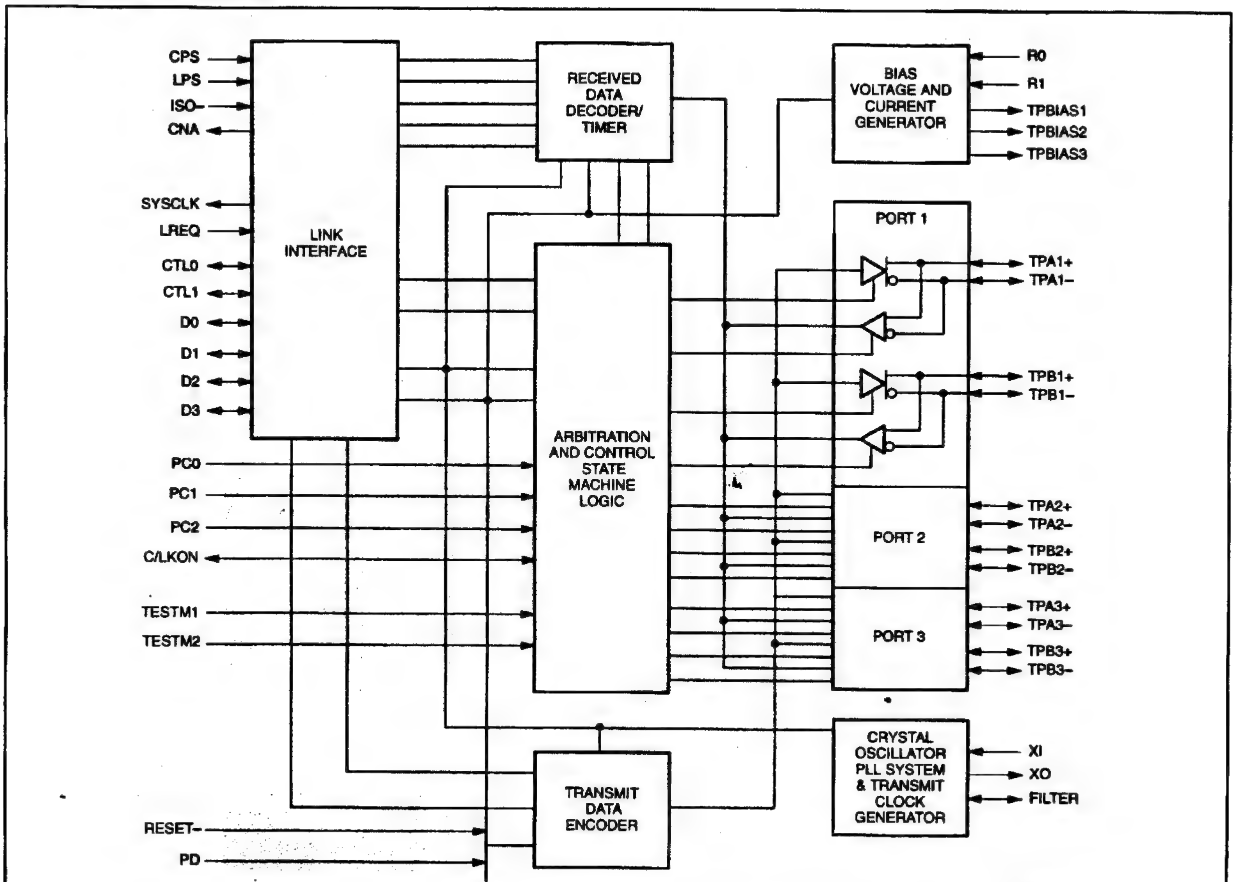
5.0 PIN DESCRIPTION

PIN NUMBER	PIN SYMBOL	I/O	NAME AND FUNCTION
1	RESET–	I*	Phy reset, active LOW
2	LPS	I*	Link Layer Controller (LLC) power status
3	LREQ	I*	Link request from controller
4	DVDD	I*	Should be connected to the LLC V_{DD} supply when a 5V LLC is connected to the Phy, and should be connected to the Phy DVDD when a 3V LLC is used.
5, 6, 19, 20	DVDD	I	Digital circuit power
7	PD	I*	Device power down input
8, 10, 17, 18, 63, 64	DGND	–	Digital circuit ground
9	SYSCLK	O*	49.152 MHz clock to link controller
11, 12	CTL[0:1]	I/O*	Link interface bi-directional control signals
13, 14, 15, 16	D[0:3]	I/O*	Link interface bi-directional data signals
22, 21	TESTM[1:2]	I*	Test/Mode Control pins 11 =1394–1995 mode 10 = 1394a mode 00/01 = Reserved
23	CPS	I	Cable power status
24, 25, 51, 55	AVDD	–	Analog circuit power
26, 32, 41, 49, 50, 61	AGND	–	Analog circuit ground
27	C/LKON	I/O*	Bus/Isochronous Resource Manager capable input, or LINK-ON signal output
30, 29, 28	PC[0:2]	I*	Power class bits 0 through 2 inputs
31	CNA	O*	Cable Not Active output
36, 40, 45	TPA[1:3]+	I/O	Port n cable pair A, positive signal
35, 39, 44	TPA[1:3]–	I/O	Port n cable pair A, negative signal
34, 38, 43	TPB[1:3]+	I/O	Port n cable pair B, positive signal
33, 37, 42	TPB[1:3]–	I/O	Port n cable pair B, negative signal
46, 47, 48	TPBIAS[1:3]	O	Cable termination voltage supplies
52, 53	PLLGND	–	PLL circuit ground
54	FILTER	I/O	PLL external filter capacitor
56	XI	I	Crystal oscillator connection
57	XO	O	Crystal oscillator connection
58	PLLVDD	–	PLL circuit power
59, 60	R[0:1]	–	External current setting resistor
62	ISO–	I*	Link interface isolation status input

NOTE:
* Indicates 5V tolerant structure.

3-port physical layer interface PDI1394P11A

6.0 BLOCK DIAGRAM



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7.0 FUNCTIONAL SPECIFICATION

The PDI1394P11A is an IEEE1394–1995 High Performance Serial Bus Specification compliant physical layer interface device. It provides an interface between an attached link layer controller and three 1394 cable interface ports. In addition to the interface function, the PDI1394P11A performs bus initialization and arbitration functions as well as monitoring line conditions and connection status.

7.1 Clocking

The PDI1394P11A utilizes a stable internal reference clock of 196.608 MHz. The reference clock is generated using an external 24.576 MHz crystal and an internal Phase Locked Loop (PLL). The PLL clock is divided down to 49.152 MHz and 98.304 MHz clock signals. The 49.152 MHz clock is used for internal logic and provided as an output to clock a link layer controller. The 196.608 MHz and 98.304 MHz clocks are used for synchronization of the transmitted strobe and data information.

7.2 Port Interfaces

The PDI1394P11A provides the transceiver functions needed to implement a three port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. In addition to transmission and reception of packet data, the line transceivers monitor conditions on the cable to determine connection status, data speed, and bus arbitration states.

The PDI1394P11A receives data to be transmitted over the bus from two or four parallel data paths to the Link Controller, D[0:3]. These data paths are latched and synchronized with the 49.152 MHz clock. The parallel bit paths are combined serially, encoded and transmitted at either 98.304 Mb/s or 196.608 Mb/s, depending whether the transaction is a 100 Mb/s or 200 Mb/s transfer, respectively. The transmitted data is encoded as data-strobe information, with the data information being transmitted on the TPB cable pairs and the strobe information transmitted on the TPA cable pairs.

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair and the strobe information is received on the TPB cable pair. The combination of the data and strobe signals is decoded to recover the receive clock signal and the serial data stream. The serial data stream is converted to two or four parallel bit streams, resynchronized to the internal 49.152 MHz clock and sent to the

3-port physical layer interface PDI1394P11A

associated link controller. The received data is also transmitted out the other active cable ports.

The cable status, bus initialization and arbitration states are monitored through the cable interface using differential comparators. The outputs of these comparators are used by internal logic to determine cable and arbitration status. The TPA channel monitors the incoming cable common-mode voltage value during arbitration to determine the speed of the next packet transmission. The TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage, indicating the cable connection status.

The PDI1394P11A provides a nominal 1.85 V for driver load termination. This bias voltage, when seen through a cable by a remote receiver, is used to sense the presence of an active connection. The value of this bias voltage has been chosen to allow inter-operability between transceiver chips operating from either 5 V nominal supplies, or 3.3 V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor. When not powered, the PDI1394P11A prevents the bias voltage from erroneously powering up the part as is seen in some other Phys.

8.0 RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	DC supply voltage	Source/non-source power node	2.7	3.3	3.6	V
V_{IH}	High level input voltage	CMOS inputs	2.0		5.5	V
V_{IL}	Low level input voltage	CMOS inputs			0.8	V
V_{ID-100}	Differential input voltage	Cable inputs, 100Mbit operation	142		260	mV
V_{ID-200}	Differential input voltage	Cable inputs, 200Mbit operation	132		260	mV
V_{ID-ARB}	Differential input voltage	Cable inputs, during arbitration	171		262	mV
V_{IC-100}	Common mode voltage	TPB cable inputs, 100Mbit or speed signaling OFF, source power node	1.165		2.515	V
		TPB cable inputs, 100Mbit or speed signaling OFF, non–source power node	1.165		2.015	
$V_{IC-200SP}$	Common mode voltage	TPB cable inputs, 200Mbit or speed signaling, source power node	0.935		2.515	V
		TPB cable inputs, 200Mbit or speed signaling, non–source power node	0.935		2.015	
	Receive input jitter	TPA, TPB cable inputs, 100Mbit operation			±1.08	ns
		TPA, TPB cable inputs, 200Mbit operation			±0.5	ns
	Receive input skew	Between TPA and TPB cable inputs, 100Mbit operation			±0.8	ns
		Between TPA and TPB cable inputs, 200Mbit operation			±0.55	ns
I_{OL}/I_{OH}	Output current, I_{OL}/I_{OH}	SYSCLK	–16		16	mA
		Control, Data, CNA, C/LKON	–12		12	
I_O	Output current	TPBIAS outputs	–3		1.3	mA
f_{XTAL}	Crystal frequency	Parallel resonant fundamental mode crystal	24.5735	24.576	24.5785	MHz
T_{amb}	Operating ambient temperature range in free air		0		+70	°C

9.10.2 IC7103: PDI1394L21

1394 full duplex AV link layer controller PDI1394L21

1.0 FEATURES

- IEEE 1394–1995 Standard Link Layer Controller
- Hardware Support for the IEC61883 International Standard of Digital Interface for Consumer Electronics
- Interface to any IEEE 1394–1995 Physical Layer Interface
- 5V Tolerant I/Os
- Single 3.3V supply voltage
- Full-duplex isochronous operation
- Operates with 400/200/100 Mbps physical layer devices
- Dual 4K Byte FIFOs for isochronous data
- Supports single capacitor isolation mode and IEEE 1394–1995, Annex J. isolation
- 4-field deep SYT buffer added to enhance real-time isochronous synchronization using the AVFSYNC pin
- Generates its own AV port clocks under software control. Select one of three frequencies: 24.576, 12.288, or 6.144 MHz

2.0 DESCRIPTION

The PDI1394L21, Philips Semiconductors Full Duplex 1394 Audio/Video (AV) Link Layer Controller, is an IEEE 1394–1995 compliant link layer controller featuring 2 embedded AV layer interfaces. The AV layers are designed to pack and un-pack application data packets for transmission over the IEEE 1394 bus using isochronous data transfers. Because of its full duplex architecture, the PDI1394L21 is capable of receiving and transmitting isochronous data during the same bus cycle. Two 8 bit AV ports, each with its own buffer (FIFO), receive and output isochronous data for transmission and reception of bus packets. Each port can be configured to receive or transmit, however, the other port always performs the opposite function. Half duplex operation is also permitted.

The application data is packetized according to the IEC 61883 International Standard of Interface for Consumer Electronic Audio/Video Equipment. Both AV layer interfaces are byte-wide ports capable of accommodating various MPEG–2 and DVC codecs. An 80C51 compatible byte-wide host interface is provided for internal register configuration as well as performing asynchronous data transfers.

The PDI1394L21 is powered by a single 3.3V power supply and the inputs and outputs are 5V tolerant. It is available in the LQFP100 and TQFP100 packages.

3.0 QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Functional supply voltage range		3.0	3.3	3.6	V
I_{DD}	Supply current @ V_{DD} = 3.3V	Operating		75		mA
SCLK	Device clock		49.147	49.152	49.157	MHz

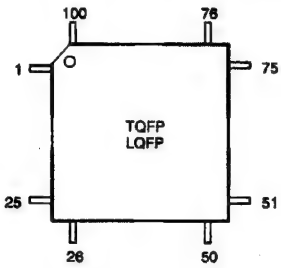
4.0 ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
100-pin plastic LQFP100	0°C to +70°C	PDI1394L21BE	PDI1394L21BE	SOT407 AB15
100-pin plastic TQFP100	0°C to +70°C	PDI1394L21BP	PDI1394L21BP	SOT386 BB2

NOTE:
This datasheet is subject to change.
Please visit our internet website www.semiconductors.philips.com/1394 for latest changes.

1394 full duplex AV link layer controller PDI1394L21

5.0 PIN CONFIGURATION



Pin	Function	Pin	Function	Pin	Function
1	HIF D7	35	PHY D6*	69	AV1 D1
2	HIF D6	36	PHY D5*	70	AV1 D2
3	HIF D5	37	PHY D4*	71	AV1 D3
4	HIF D4	38	GND	72	V_{DD}
5	GND	39	V_{DD}	73	GND
6	V_{DD}	40	PHY D3*	74	AV1 D4
7	HIF D3	41	PHY D2*	75	AV1 D5
8	HIF D2	42	PHY D1*	76	AV1 D6
9	HIF D1	43	PHY D0*	77	AV1 D7
10	HIF D0	44	GND	78	V_{DD}
11	CLK25	45	V_{DD}	79	GND
12	GND	46	PHY CTL1*	80	AV2ERR1
13	V_{DD}	47	PHY CTL0*	81	AV2ERR0
14	HIF A8	48	ISO_N	82	AV2ENDPCK
15	HIF A7	49	V_{DD}	83	AV2SYNC
16	HIF A6	50	GND	84	AV2CLK
17	HIF A5	51	N/C	85	AV2FSYNC
18	HIF A4	52	AV1ERR1	86	AV2VALID
19	HIF A3	53	AV1ERR0	87	GND
20	HIF A2	54	LREQ*	88	V_{DD}
21	HIF A1	55	SCLK	89	AV2 D0
22	HIF A0	56	AV1ENDPCK	90	AV2 D1
23	GND	57	AV1SYNC	91	AV2 D2
24	V_{DD}	58	AV1CLK	92	AV2 D3
25*	HIF CS_N	59	AV1FSYNC	93	GND
26	HIF WR_N	60	AV1ENKEY	94	V_{DD}
27	HIF RD_N	61	AV1VALID	95	AV2D4
28	HIF INT_N	62	N/C	96	AV2 D5
29	RESET_N	63	GND	97	AV2 D6
30	CYCLE IN	64	V_{DD}	98	AV2 D7
31	GND	65	RESESRVED	99	AV2ENKEY
32	V_{DD}	66	RESERVED	100	N/C
33	CYCLE OUT	67	RESERVED		
34	PHY D7*	68	AV1 D0		

* INDICATES PIN EQUIPPED WITH INTERNAL BUS HOLD CIRCUIT ACTIVATED BY THE STATE OF THE ISO_N PIN.

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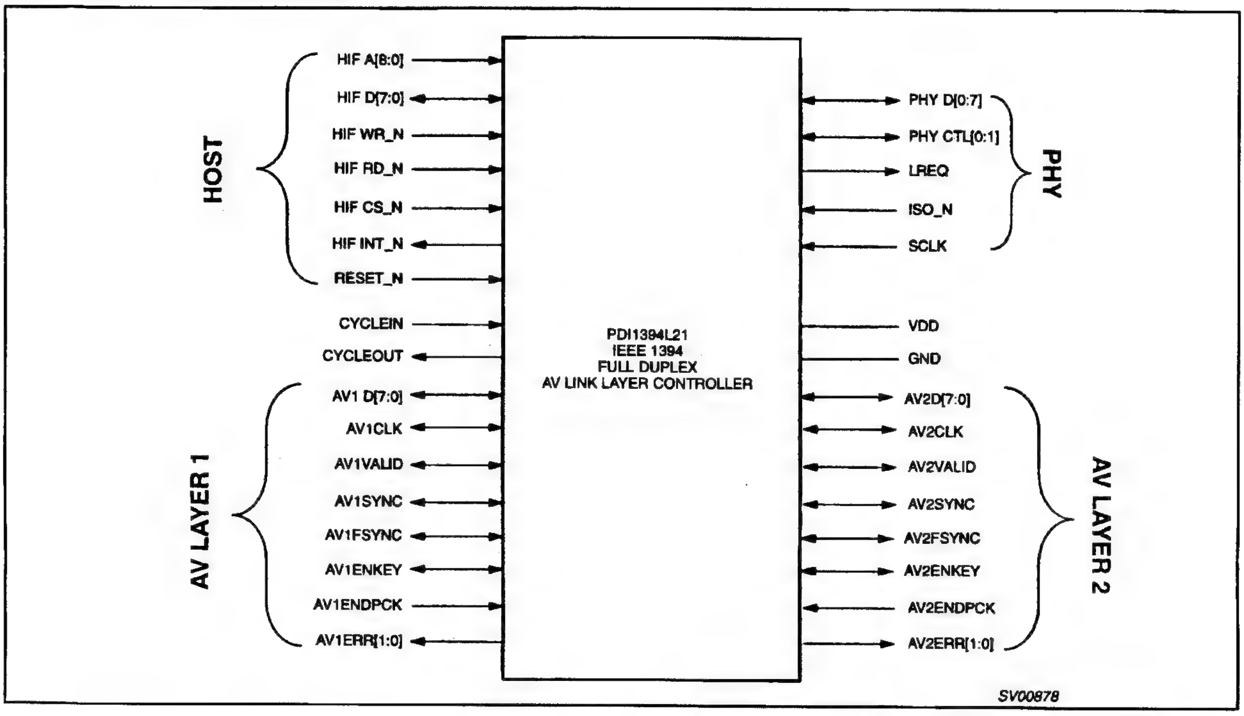
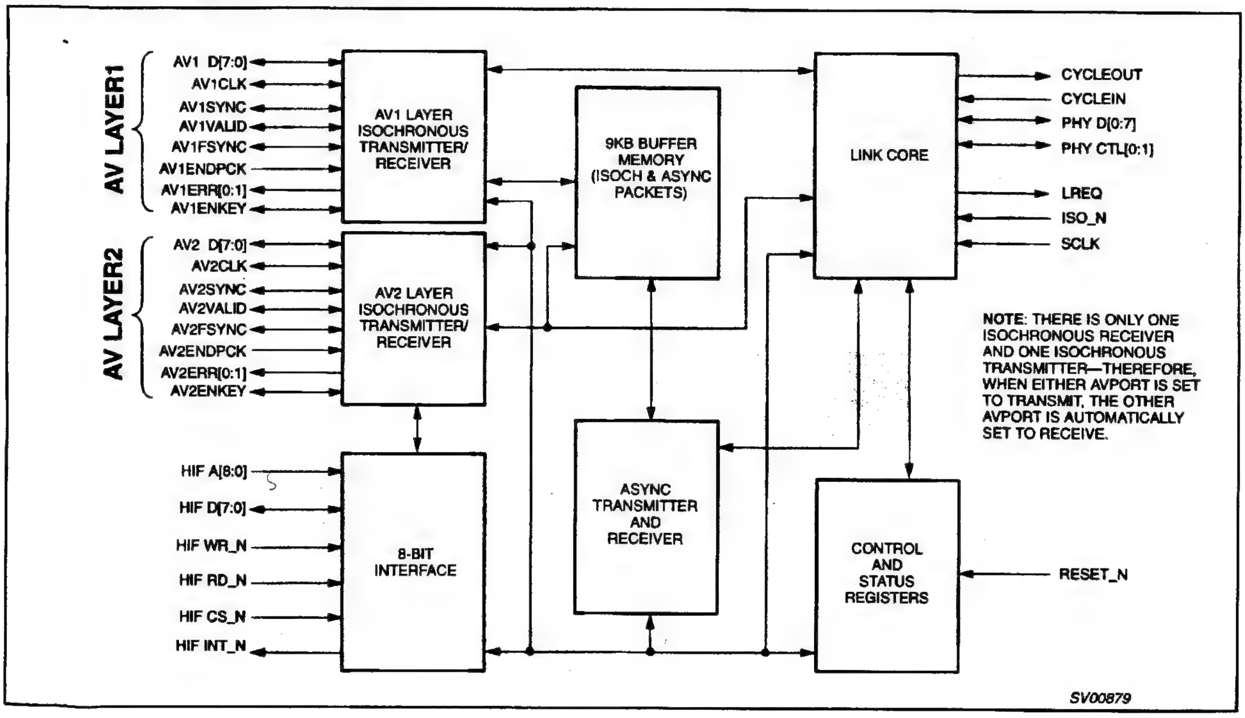
1394 full duplex AV link layer controller PDI1394L21

6.0 FUNCTIONAL DIAGRAM



7.0 INTERNAL BLOCK DIAGRAM



9.10.3 IC7203: P89C51

80C51 8-bit Flash microcontroller family

16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

P89C51RB2/P89C51RC2/ P89C51RD2

DESCRIPTION

The P89C51RB2/RC2/RD2 device contains a non-volatile 16kB/32kB/64kB Flash program memory that is both parallel programmable and serial In-System and In-Application Programmable. In-System Programming (ISP) allows the user to download new code while the microcontroller sits in the application. In-Application Programming (IAP) means that the microcontroller fetches new program code and reprograms itself while in the system. This allows for remote programming over a modem link. A default serial loader (boot loader) program in ROM allows serial In-System programming of the Flash memory via the UART without the need for a loader in the Flash code. For In-Application Programming, the user program erases and reprograms the Flash memory by use of standard routines contained in ROM.

This device executes one machine cycle in 6 clock cycles, hence providing twice the speed of a conventional 80C51. An OTP configuration bit lets the user select conventional 12 clock timing if desired.

This device is a Single-Chip 8-Bit Microcontroller manufactured in advanced CMOS process and is a derivative of the 80C51 microcontroller family. The instruction set is 100% compatible with the 80C51 instruction set.

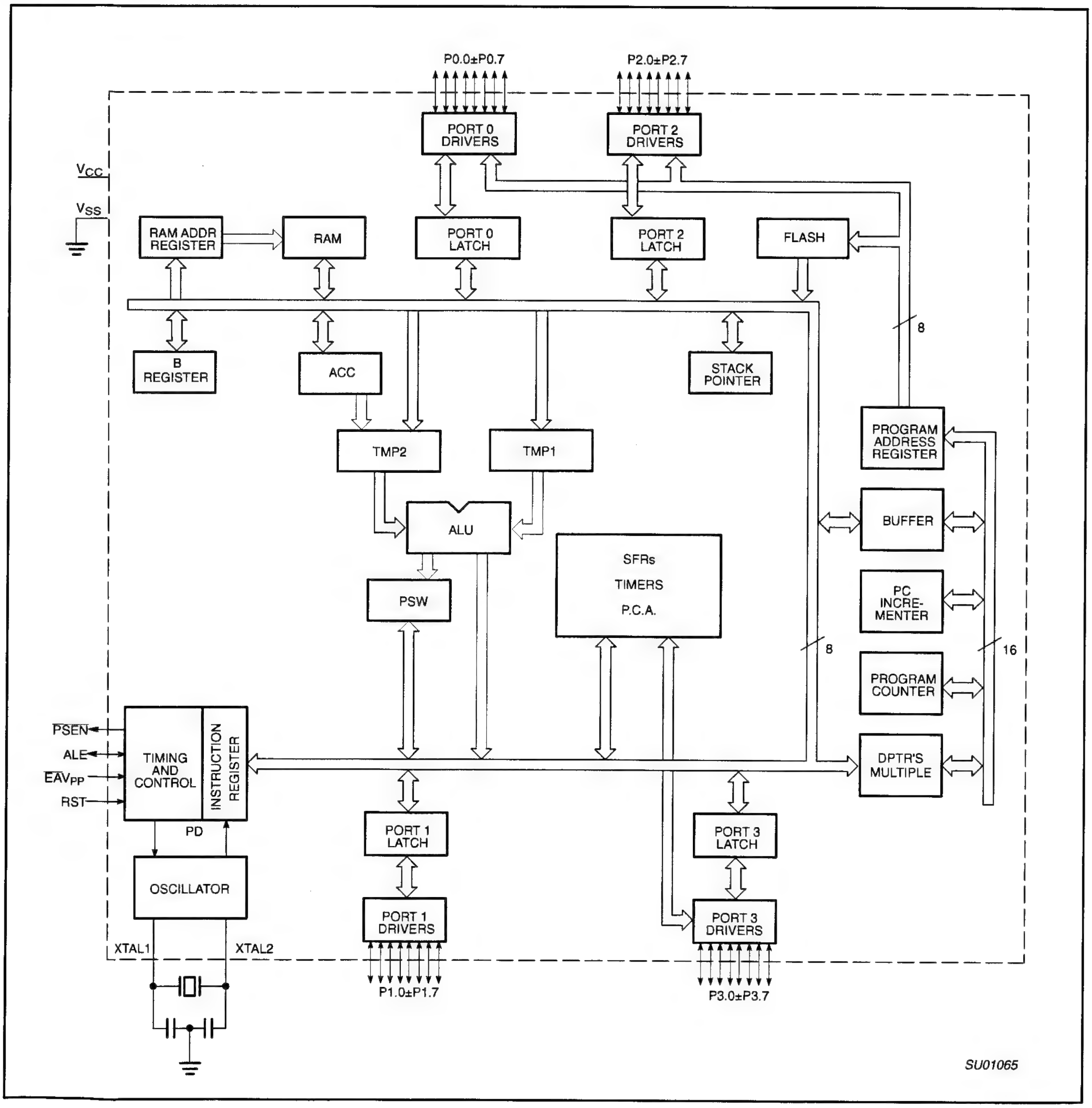
The device also has four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits.

The added features of the P89C51RB2/RC2/RD2 makes it a powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control.

FEATURES

- 80C51 Central Processing Unit
- On-chip Flash Program Memory with In-System Programming (ISP) and In-Application Programming (IAP) capability
- Boot ROM contains low level Flash programming routines for downloading via the UART
- Can be programmed by the end-user application (IAP)
- 6 clocks per machine cycle operation (standard)
- 12 clocks per machine cycle operation (optional)
- Speed up to 20 MHz with 6 clock cycles per machine cycle (40 MHz equivalent performance); up to 33 MHz with 12 clocks per machine cycle
- Fully static operation
- RAM expandable externally to 64 kB
- 4 level priority interrupt
- 7 interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
  - ± Framing error detection
  - ± Automatic address recognition
- Power control modes
  - ± Clock can be stopped and resumed
  - ± Idle mode
  - ± Power down mode
- Programmable clock out
- Second DPTR register
- Asynchronous port reset
- Low EMI (inhibit ALE)
- Programmable Counter Array (PCA)
  - ± PWM
  - ± Capture/compare

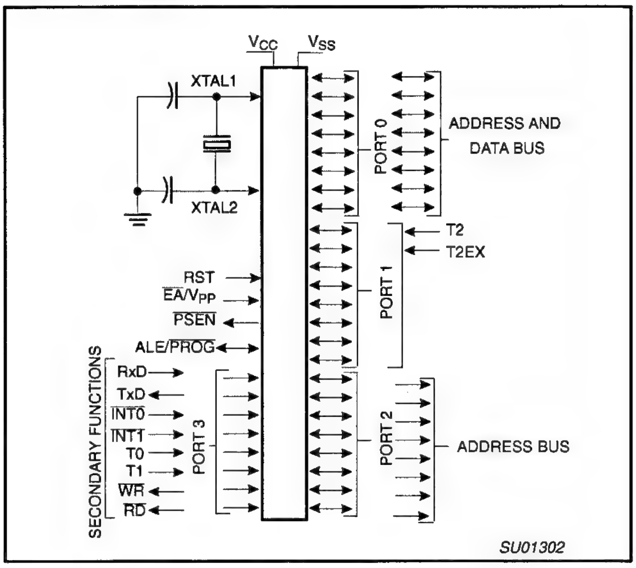
BLOCK DIAGRAM



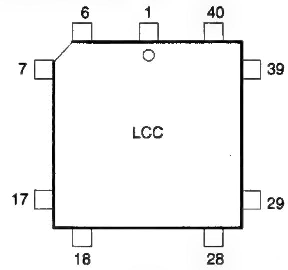
80C51 8-bit Flash microcontroller family
16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

P89C51RB2/P89C51RC2/ P89C51RD2

LOGIC SYMBOL



Plastic Leaded Chip Carrier



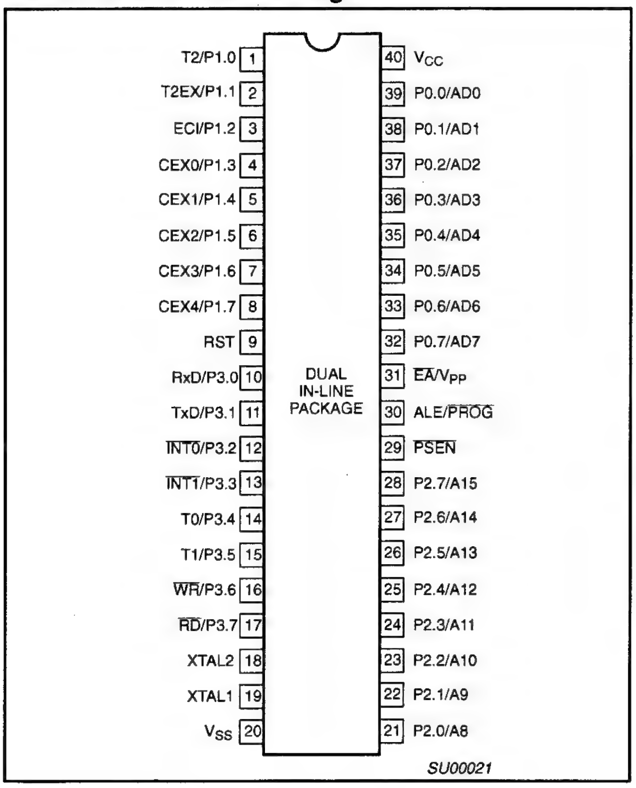
Pin	Function	Pin	Function	Pin	Function
1	NIC*	16	P3.4/T0	31	P2.7/A15
2	P1.0/T2	17	P3.5/T1	32	PSEN
3	P1.1/T2EX	18	P3.6/WR	33	ALE/PROG
4	P1.2/ECI	19	P3.7/RD	34	NIC*
5	P1.3/CEX0	20	XTAL2	35	EA/V_{PP}
6	P1.4/CEX1	21	XTAL1	36	P0.7/AD7
7	P1.5/CEX2	22	V_{SS}	37	P0.6/AD6
8	P1.6/CEX3	23	NIC*	38	P0.5/AD5
9	P1.7/CEX4	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NIC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/INT0	29	P2.5/A13	44	V_{CC}
15	P3.3/INT1	30	P2.6/A14		

* NO INTERNAL CONNECTION

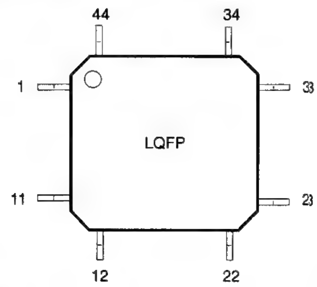
SU00023

PINNING

Plastic Dual In-Line Package



Plastic Quad Flat Pack



Pin	Function	Pin	Function	Pin	Function
1	P1.5/CEX2	16	V_{SS}	31	P0.6/AD6
2	P1.6/CEX3	17	NIC*	32	P0.5/AD5
3	P1.7/CEX4	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	P3.0/RxD	20	P2.2/A10	35	P0.2/AD2
6	NIC*	21	P2.3/A11	36	P0.1/AD1
7	P3.1/TxD	22	P2.4/A12	37	P0.0/AD0
8	P3.2/INT0	23	P2.5/A13	38	V_{CC}
9	P3.3/INT1	24	P2.6/A14	39	NIC*
10	P3.4/T0	25	P2.7/A15	40	P1.0/T2
11	P3.5/T1	26	PSEN	41	P1.1/T2EX
12	P3.6/WR	27	ALE/PROG	42	P1.2/ECI
13	P3.7/RD	28	NIC*	43	P1.3/CEX0
14	XTAL2	29	EA/V_{PP}	44	P1.4/CEX1
15	XTAL1	30	P0.7/AD7		

* NO INTERNAL CONNECTION

SU01400

80C51 8-bit Flash microcontroller family P89C51RB2/P89C51RC2/P89C51RD2

16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	PDIP	PLCC	LQFP		
V_{SS}	20	22	16	I	**Ground:** 0 V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0±0.7	39±32	43±36	37±30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0±P1.7	1±8	2±9	40±44, 1±3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups on all pins except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}).
					Alternate functions for 89C51RB2/RC2/RD2 Port 1 include:
	1	2	40	I/O	**T2 (P1.0):** Timer/Counter 2 external count input/Clockout (see Programmable Clock-Out)
	2	3	41	I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control
	3	4	42	I	**ECI (P1.2):** External Clock Input to the PCA
	4	5	43	I/O	**CEX0 (P1.3):** Capture/Compare External I/O for PCA module 0
	5	6	44	I/O	**CEX1 (P1.4):** Capture/Compare External I/O for PCA module 1
	6	7	1	I/O	**CEX2 (P1.5):** Capture/Compare External I/O for PCA module 2
	7	8	2	I/O	**CEX3 (P1.6):** Capture/Compare External I/O for PCA module 3
	8	9	3	I/O	**CEX4 (P1.7):** Capture/Compare External I/O for PCA module 4
P2.0±P2.7	21±28	24±31	18±25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
					P2.7 must be a ªlº to program and erase the device.
P3.0±P3.7	10±17	11, 13±19	5, 7±13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 89C51RB2/RC2/RD2, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE	30	33	27	O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted twice every machine cycle, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.

80C51 8-bit Flash microcontroller family
16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

P89C51RB2/P89C51RC2/ P89C51RD2

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	PDIP	PLCC	LQFP		
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}/V_{PP}$	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations. If $\overline{EA}$ is held high, the device executes from internal program memory. The value on the $\overline{EA}$ pin is latched when RST is released and any subsequent changes have no effect. This pin also receives the programming supply voltage (V_{PP}) during Flash programming.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid ªlatch-upº effect at power-on, the voltage on any pin (other than V_{PP}) must not be higher than V_{CC} + 0.5 V or less than V_{SS} ± 0.5 V.

9.10.4 IC7307; IC7308: CY2071AS

CY2071A

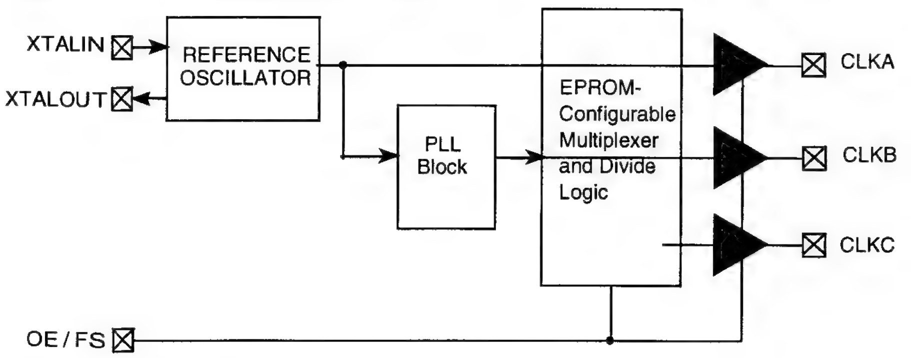
EPROM Programmable Clock Generator

Features	Benefits
Single phase-locked loop architecture	Generates a custom frequency from an external source
EPROM programmability	Easy customization and fast turnaround
Factory-programmable (CY2071A, CY2071AI) or field-programmable (CY2071AF, CY2071AFI) device options	Programming support available for all opportunities
Up to three configurable outputs	Generates three related frequencies from a single device
Low-skew, low-jitter, high-accuracy outputs	Meets critical industry standard timing requirements
Internal loop filter	Alleviates the need for external components
Power management (OE)	Supports low-power applications
Frequency select options	3 outputs with 2 user selectable frequencies
Configurable 5V or 3.3V operation	Supports industry standard design platforms
8-pin 150-mil SOIC package	Industry-standard packaging saves on board space

Selector Guide

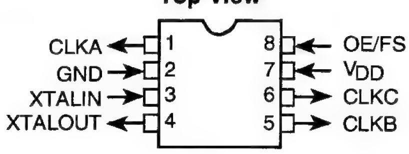
Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2071A	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–130 MHz (5V) 500 kHz–100 MHz (3.3V)	Factory Programmable Commercial Temperature
CY2071AI	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–100 MHz (5V) 500 kHz–80 MHz (3.3V)	Factory Programmable Industrial Temperature
CY2071AF	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–100 MHz (5V) 500 kHz–80 MHz (3.3V)	***Field Programmable*** Commercial Temperature
CY2071AFI	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–90 MHz (5V) 500 kHz–66.6 MHz (3.3V)	***Field Programmable*** Industrial Temperature

Logic Block Diagram for CY2071A



Pin Configuration

8-pin SOIC
Top View



Pin Summary

Name	Number	Description
CLKA	1	Configurable Clock Output
GND	2	Ground
XTALIN	3	Reference Crystal Input or External Reference Clock Input
XTALOUT	4	Reference Crystal Feedback
CLKB	5	Configurable Clock Output
CLKC	6	Configurable Clock Output
V_{DD}	7	Voltage Supply
OE / FS	8	Output Control Pin, either Output Enable or Frequency Select Input (Active-HIGH, internal pull-up resistor to V_{DD})

Notes:

1. For best accuracy, use a parallel-resonant crystal, C_L = 17 pF.
2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to an external crystal).

Functional Description

The CY2071A is a general-purpose clock synthesizer designed for use in applications such as modems, disk drives, CD-ROM drives, video CD players, games, set-top boxes, and data/telecommunications. The device offers up to three configurable clock outputs in an 8-pin, 150-mil SOIC package and can operate off either a 3.3V or 5V power supply. The on-chip reference oscillator is designed for 10-MHz to 25-MHz crystals. Alternatively, an external reference clock of frequency between 1 MHz and 30 MHz can be used.

The CY2071A has one PLL and outputs three factory-EPROM configurable clocks: CLKA, CLKB, and CLKC. The output clocks can originate either from the PLL or the reference, or selected dividers thereof. Additionally, pin 8 can be configured to be an Output Enable or a Select input.

The CY2071A can replace multiple Metal Can Oscillators (MCO) in a synchronous system, providing cost and board space savings to the manufacturer. Hence, these devices are ideally suited for applications that require multiple, accurate, and stable clocks synthesized from low-cost generators in small packages. A hard-disk drive is an example of such an application. In this case, CLKA drives the PLL in the Read Controller, while CLKB and CLKC drive the MCU and associated sequencers.

CyClocks™ Software

CyClocks is an easy-to-use software application that allows you to configure any one of the EPROM-Programmable Clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Please note the output frequency ranges in this data sheet when specifying them in CyClocks to ensure that you stay within the limits. You can download a copy of CyClocks free on the Cypress Semiconductor website at www.cypress.com.

Consider using the CY2081 for applications that require unrelated output frequencies. Consider using the CY2291, CY2292, or CY2907 for applications that require more than three output clocks.

Cypress FTG Programmer

The Cypress Frequency Timing Generator (FTG) Programmer is a portable programmer designed to custom program our family of EPROM **Field** Programmable Clock Devices. The FTG programmers connect to a PC serial port and allow users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. The ordering code for the Cypress FTG Programmer is CY3670.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .... –0.5V to +7.0V

DC Input Voltage .... –0.5V to V_{DD}+0.5V

Storage Temperature .... –65°C to +150°C

Max. Soldering Temperature (10 sec) .... 260°C

Junction Temperature .... 150°C

Static Discharge Voltage .... >2000V
(per MIL-STD-883, Method 3015)

9.10.5 IC7404: NW701

divio

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NW701

DV-SD CODEC Data Sheet

Enhanced "Blue Book" Features
- Fully "Blue Book" DV– SD Compliant
- Optional Low Data-Rate Modes: 3.0, 2.4, 1.8, 1.5, and 1.0 Mbytes /sec (for IDE disk drive compatibility)
- Double Clock Option: Capable of operation up to 54 MHz for dual stream applications.

Comprehensive Video and Audio I/O
- NTSC (4:1:1) and PAL (4:2:0) processing
- Integrated multi-tap video filter for 4:2:2 to 4:1:1 or 4:2:2 to 4:2:0 conversions
- Synchronous and "Handshake" Modes
- Glue-less connection to ITU-R-656 (8-bit) video bus
- Popular I2S audio interface
- 48, 44.1 and 32 kHz (12 and 16 bit) audio support

Low Power, Small Footprint
- Low Power Consumption: 0.4W at 27Mhz
- Power Down Mode (60 µW power)
- 3.3V Operating Voltage
- 0.35 Micron, 4 Level Metal Process
- Requires only one 256K x 32 EDO DRAM (Shuffle Memory)
- 160 Pin LQFP (20 x 20 x 1.4 mm) package

High Quality, Low Cost
- ISO9001 Quality Fab
- Extensive design verification

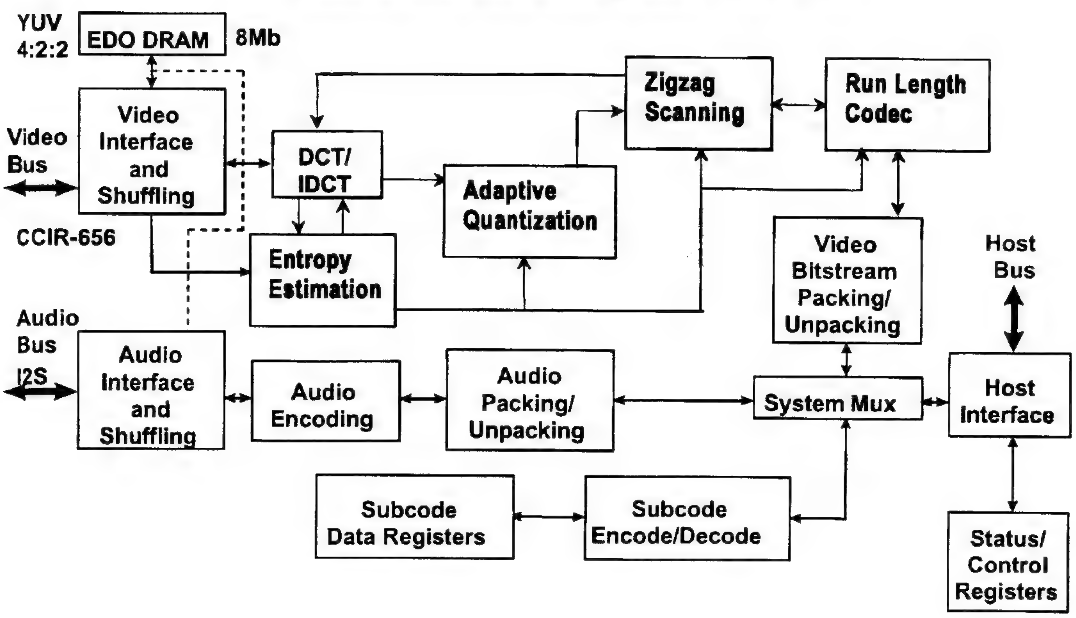
Integrated Solution
- Video I/O and Video Compression
- Audio I/O processing
- Full AUX Code support
- Integrated Shuffle Memory logic
- Glue-less interface to EDO DRAM

Simple Host Bus Connection
- One 16-Bit Asynchronous Host Bus Interface
- Multiplexed Address / Data Bus
- Register and "DV FIFO" access
- 512 Byte DV FIFO for ease of system integration
- Simple Register Programming
- 3 Interrupt pins for system control
- High Speed (33 Mbytes/sec) throughput

Comprehensive Application Support
- Full Applications Support
- Hardware Reference (demo board)
- Board schematics, layout, and Gerber files
- Telephone and e-mail support
- SDK (Software Developer Kit) for chip and demo board available, both source and object code
- Developer CD includes hardware and software support

Glue-less Connections
- Connects directly to decoders, encoder, audio CODECs
- Direct connection to Philips SAA7146A PCI Bridge

Functional Block Diagram – NW701



Section 1: Overview

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NW701 - DV CODEC: Functional Block Description

Video Interface/Shuffling:

This block provides glue-less connection to industry standard CCIR-656 compatible video bus. Processing of NTSC (4:1:1) and PAL (4:2:0) is perform by this block. Filtering from 4:2:2 down to 4:1:1 or 4:2:0 is perform using multi-tap video filters for maintaining "best" overall picture quality.
To obtain stable quantization for best overall performance, shuffling of Macro blocks are perform using an external memory (256x32 EDO DRAM). Shuffling is required to even out the data in the video image so that there is an even flow for the compression logic to achieve maximum performance.

DCT/IDCT – Discrete Cosine Transform / Inverse Discrete Cosine Transform

This block takes video stream, divided in 8x8 pixel blocks (Macro Block-MB), and performs fast DCT/IDCT operation. The Pixels informations in each block are converted from the "space" domain to "frequency" domain in DCT process in exact reverse in IDCT process.

Encoder Decision Block

To improve coding efficiency, selection is made between 8x8 and/or 2x4x8 DCT modes. Generally, 8x8 mode works best when a video stream contains fields with very small difference. 2x4x8 mode is selected for the opposite condition – namely, for fields containing large difference. 2x4x8 mode includes two 4x8-macro blocks – one MB is the sum of two fields and other is the difference between two fields.

Entropy Estimation

To improve coding efficiency, selection is made between 8x8 and 2x4x8 DCT modes based on the entropy calculation in each block. Class numbers are chosen according the maximum AC coefficients in DCT. These informations are critical to achieve the best quality possible.

Adaptive Quantization

Higher compression is achieved when many DCT AC coefficients are close to Zero. In order to achieve 5:1 compression ration, as specified by the DV standard, the adaptive quantization module will select the best quantization weighting coefficients based on the class number and best-fit bit stream during the selection process.

Zigzag Scanning

This process roughly approximates the selection from "low-frequency" coefficients to "high-frequency" coefficients.

Run Length Codec

The Run Length Coder (RLC) will further compress the bit stream after zigzag scanning by encoding the quantized coefficients and representing consecutive zero coefficients as "another" symbol. The Run Length Decoder (RLD) will restore the zeroes and amplitudes encoded in the bit stream.

Video Packing/Unpacking

This is a final stage for compression, which packs the encoded video data as specified by the DV standard. Or it works as the first stage during the decompression mode to extract video from the DIF stream.

Audio Blocks

This block provides glue-less interface to an industry standard I2S bus for an external Audio CODEC. Furthermore,
Audio shuffling and audio bit conversion from 16-bit 12-bit audio are also processed in these blocks.

System MUX

This block provides multiplexing and de-multiplexing of Video, Audio, and subcode DIFs into a legal DV DIF bit streams as specified in "blue-book" – DV standard.

Section 1: Overview

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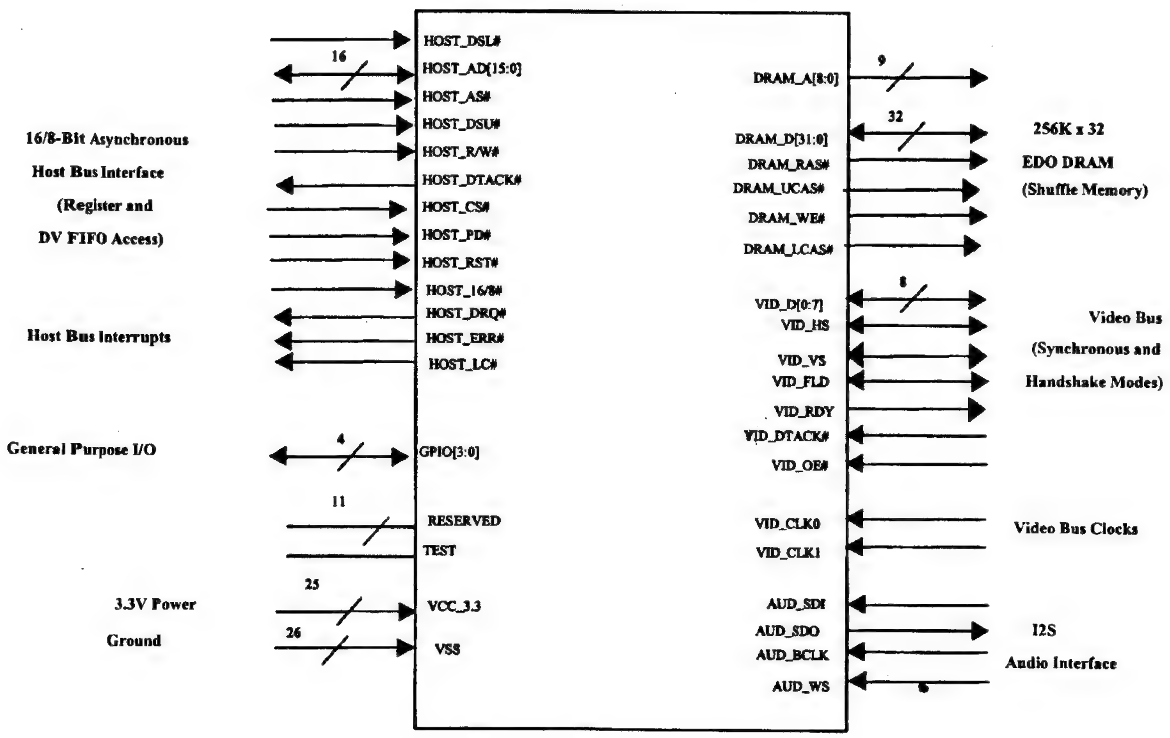
Figure 10: Functional Pin Diagram

NW701 - DV CODEC Pin Diagram



Section 1: Overview

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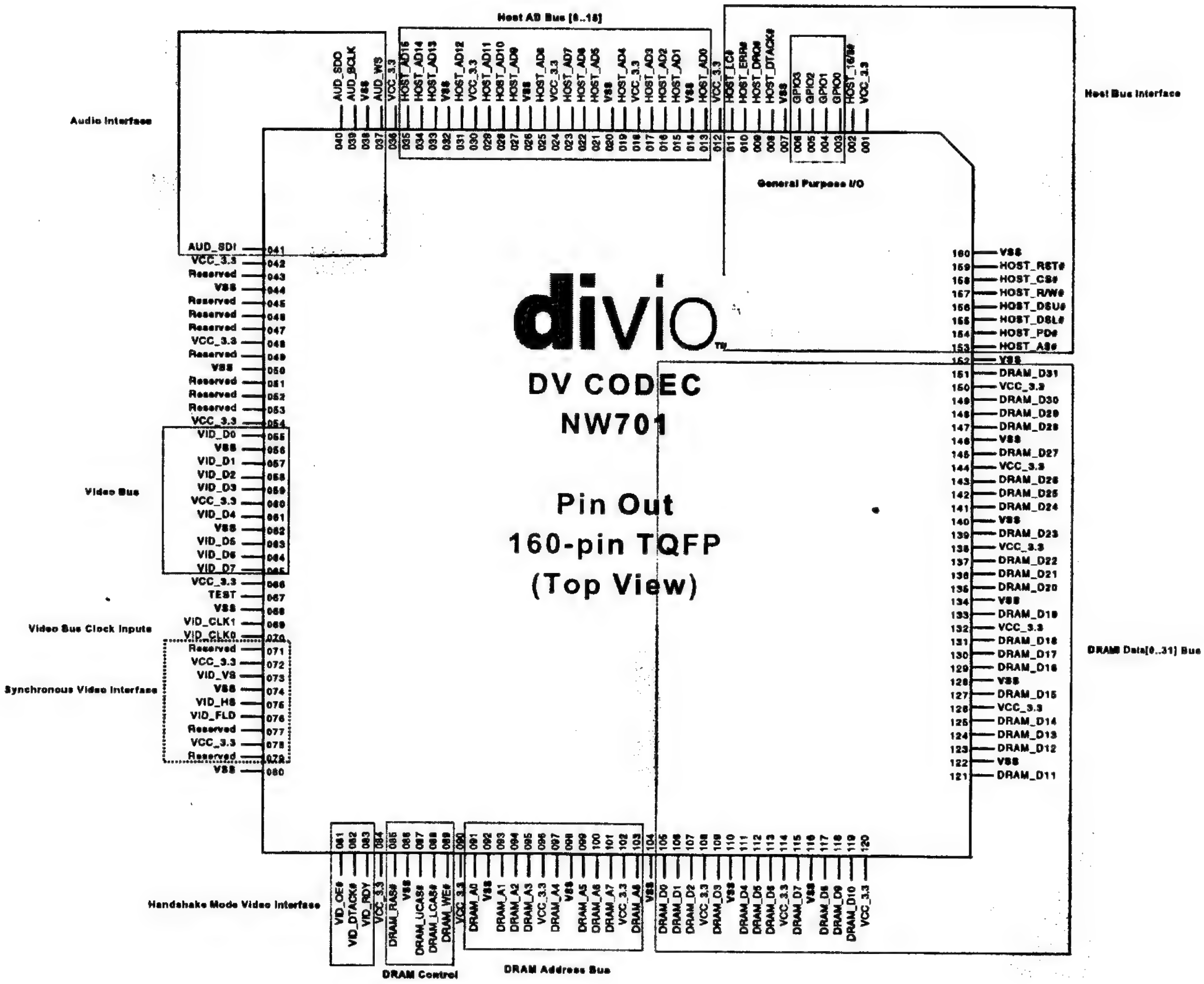

Section 2: Pin Definition

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Pin Numbers in Numerical Sequence

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	VCC_3.3	41	VCC_3.3	81	VID_OE#	121	DRAM_D11
2	HOST_16/8#	42	AUD_SDI	82	VID_DTACK	122	VSS
3	GPIO0	43	Reserved	83	VID_RDY	123	DRAM_D12
4	GPIO1	44	VSS	84	VCC_3.3	124	DRAM_D13
5	GPIO2	45	Reserved	85	DRAM_RAS#	125	DRAM_D14
6	GPIO3	46	Reserved	86	VSS	126	VCC_3.3
7	VSS	47	Reserved	87	DRAM_UCAS#	127	DRAM_D15
8	HOST_DTACK#	48	VCC_3.3	88	DRAM_LCAS#	128	VSS
9	HOST_DRQ#	49	Reserved	89	DRAM_WE#	129	DRAM_D16
10	HOST_ERR#	50	VSS	90	VCC_3.3	130	DRAM_D17
11	HOST_LC#	51	Reserved	91	DRAM_A0	131	DRAM_D18
12	VCC_3.3	52	Reserved	92	VSS	132	VCC_3.3
13	HOST_AD0	53	Reserved	93	DRAM_A1	133	DRAM_D19
14	VSS	54	VCC_3.3	94	DRAM_A2	134	VSS
15	HOST_AD1	55	VID_D0	95	DRAM_A3	135	DRAM_D20
16	HOST_AD2	56	VSS	96	VCC_3.3	136	DRAM_D21
17	HOST_AD3	57	VID_D1	97	DRAM_A4	137	DRAM_D22
18	VCC_3.3	58	VID_D2	98	VSS	138	VCC_3.3
19	HOST_AD4	59	VID_D3	99	DRAM_A5	139	DRAM_D23
20	VSS	60	VCC_3.3	100	DRAM_A6	140	VSS
21	HOST_AD5	61	VID_D4	101	DRAM_A7	141	DRAM_D24
22	HOST_AD6	62	VSS	102	VCC_3.3	142	DRAM_D25
23	HOST_AD7	63	VID_D5	103	DRAM_A8	143	DRAM_D26
24	VCC_3.3	64	VID_D6	104	VSS	144	VCC_3.3
25	HOST_AD8	65	VID_D7	105	DRAM_D0	145	DRAM_D27
26	VSS	66	VCC_3.3	106	DRAM_D1	146	VSS
27	HOST_AD9	67	TEST	107	DRAM_D2	147	DRAM_D28
28	HOST_AD10	68	VSS	108	VCC_3.3	148	DRAM_D29
29	HOST_AD11	69	VID_CLK1	109	DRAM_D3	149	DRAM_D30
30	VCC_3.3	70	VID_CLK0	110	VSS	150	VCC_3.3
31	HOST_AD12	71	Reserved	111	DRAM_D4	151	DRAM_D31
32	VSS	72	VCC_3.3	112	DRAM_D5	152	VSS
33	HOST_AD13	73	VID_VS	113	DRAM_D6	153	HOST_AS#
34	HOST_AD14	74	VSS	114	VCC_3.3	154	HOST_PD#
35	HOST_AD15	75	VID_HS	115	DRAM_D7	155	HOST_DSL#
36	VCC_3.3	76	VID_FLD	116	VSS	156	HOST_DSU#
37	AUD_WS	77	Reserved	117	DRAM_D8	157	HOST_R/W#
38	VSS	78	VCC_3.3	118	DRAM_D9	158	HOST_CS#
39	AUD_BCLK	79	Reserved	119	DRAM_D10	159	HOST_RST#
40	AUD_SDO	80	VSS	120	VCC_3.3	160	VSS

9.10.6 IC7506: UDA1334ATS

Low power audio DAC with PLL

UDA1334ATS

BITSTREAM CONVERSION

1 FEATURES

1.1 General

- 2.4 to 3.6 V power supply voltage
- On-board PLL to generate the internal system clock:
  - Operates as an asynchronous DAC, regenerating the internal clock from the WS signal (called audio mode)
  - Generates audio related system clock (output) based on 32, 48 or 96 kHz sampling frequency (called video mode).
- Integrated digital filter plus DAC
- Supports sample frequencies from 16 to 100 kHz in asynchronous DAC mode
- No analog post filtering required for DAC
- Easy application
- SSOP16 package.

1.2 Multiple format data interface

- I^2S-bus and LSB-justified format compatible
- $1f_s$ input data rate.

1.3 DAC digital features

- Digital de-emphasis for 44.1 kHz sampling frequency
- Mute function.

1.4 Advanced audio configuration

- High linearity, wide dynamic range and low distortion.

1.5 PLL system clock generation

- Integrated low jitter PLL for use in applications in which there is digital audio data present but the system cannot provide an audio related system clock. This mode is called audio mode.
- The PLL can generate 256 × 48 kHz and 384 × 48 kHz from a 27 MHz input clock. This mode is called video mode.

2 APPLICATIONS

This audio DAC is excellently suitable for digital audio portable application, specially in applications in which an audio related system clock is not present.

3 GENERAL DESCRIPTION

The UDA1334ATS is a single chip 2 channel digital-to-analog converter employing bitstream conversion techniques, including an on-board PLL. The extremely low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates a playback function.

The UDA1334ATS supports the I^2S-bus data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits.

The UDA1334ATS has basic features such as de-emphasis (44.1 kHz sampling frequency, only supported in audio mode) and mute.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1334ATS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

Low power audio DAC with PLL UDA1334ATS

6 BLOCK DIAGRAM

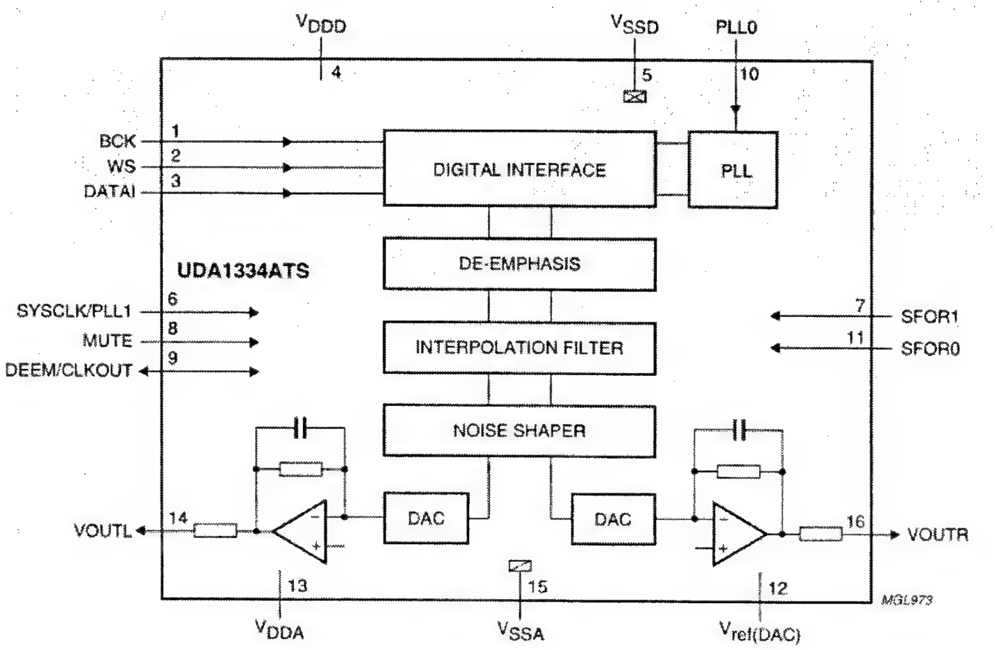


Fig.1 Block diagram.

Low power audio DAC with PLL UDA1334ATS

7 PINNING

SYMBOL	PIN	PAD TYPE	DESCRIPTION
BCK	1	5 V tolerant digital input pad	bit clock input
WS	2	5 V tolerant digital input pad	word select input
DATAI	3	5 V tolerant digital input pad	serial data input
V_{DDD}	4	digital supply pad	digital supply voltage
V_{SSD}	5	digital ground pad	digital ground
SYSCLK/PLL1	6	5 V tolerant digital input pad	system clock input in video mode/PLL mode control 1 input in audio mode
SFOR1	7	5 V tolerant digital input pad	serial format select 1 input
MUTE	8	5 V tolerant digital input pad	mute control input
DEEM/CLKOUT	9	5 V tolerant digital input/output pad	de-emphasis control input in audio mode/clock output in video mode
PLL0	10	3-level input pad; note 1	PLL mode control 0 input
SFOR0	11	digital input pad; note 1	serial format select 0 input
$V_{ref(DAC)}$	12	analog pad	DAC reference voltage
V_{DDA}	13	analog supply pad	DAC analog supply voltage
VOUTL	14	analog output pad	DAC output left
V_{SSA}	15	analog ground pad	DAC analog ground
VOUTR	16	analog output pad	DAC output right

Note

1. Because of test issues these pads are not 5 V tolerant and both pads should be at power supply voltage level or at a maximum of 0.5 V above that level.

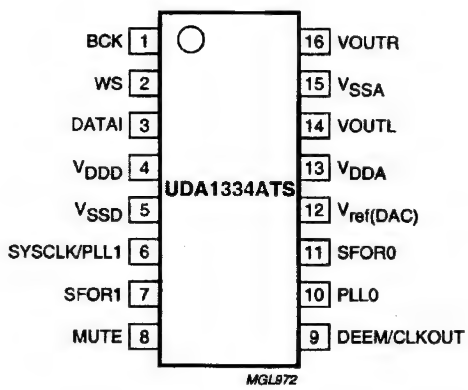


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1334ATS incorporates a PLL capable of generating the system clock. The UDA1334ATS can operate in 2 modes:

- It operates as an asynchronous DAC, which means the device regenerates the internal clocks using a PLL from the incoming WS signal. This mode is called audio mode.
- It generates the internal clocks from a 27 MHz clock input, based on 32, 48 and 96 kHz sampling frequencies. This mode is called video mode.

In video mode, the digital audio input is slave, which means that the system must generate the BCK and WS signals from the output clock available at pin CLKOUT of the UDA1334ATS. The digital audio signals should be frequency locked to the CLKOUT signal.

Remarks:

1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface
2. For LSB-justified formats it is important to have a WS signal with a duty factor of 50%.

8.1.1 AUDIO MODE

Audio mode is enabled by setting pin PLL0 to LOW. De-emphasis can be activated via pin DEEM/CLKOUT according to Table 5.

In audio mode, pin SYSCLK/PLL1 is used to set the sampling frequency range as given in Table 1.

Table 1 Sampling frequency range in audio mode

SYSCLK/PLL1	SELECTION
LOW	f_s = 16 to 50 kHz
HIGH	f_s = 50 to 100 kHz

8.1.2 VIDEO MODE

In video mode, the master clock is a 27 MHz external clock (as is available in video environment). A clock-out signal is generated at pin DEEM/CLKOUT. The output frequency can be selected using pin PLL0. The output frequency is either 12.228 MHz (256 × 48 kHz) with pin PLL0 being at MID level or 18.432 MHz (384 × 48 kHz) with pin PLL0 being HIGH, as given in Table 2.

Table 2 Clock output selection in video mode

PLL0	SELECTION
MID	12.228 MHz clock; note 1
HIGH	18.432 MHz clock; note 2
LOW	audio mode

Notes

1. The supported sampling frequencies are: 96, 48 and 24 kHz or 64, 32 and 16 kHz.
2. The supported sampling frequencies are: 96, 48 and 24 kHz; 72 and 36 kHz or 32 kHz.

8.2 Interpolation filter

The interpolation digital filter interpolates from $1f_s$ to $64f_s$ by cascading FIR filters (see Table 3).

Table 3 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	$0f_s$ to $0.45f_s$	±0.02
Stop band	$>0.55f_s$	−50
Dynamic range	$0f_s$ to $0.45f_s$	>114

8.3 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream DAC (FSDAC).

Low power audio DAC with PLL — UDA1334ATS

8.4 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally to the power supply voltage.

8.5 Power-on reset

The UDA1334ATS has an internal Power-on reset circuit (see Fig.3) which resets the test control block.

The reset time (see Fig.4) is determined by an external capacitor which is connected between pin $V_{ref(DAC)}$ and ground. The reset time should be at least 1 µs for $V_{ref(DAC)} < 1.25$ V. When V_{DDA} is switched off, the device will be reset again for $V_{ref(DAC)} < 0.75$ V.

During the reset time the system clock should be running.

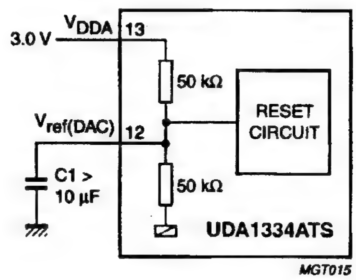


Fig.3 Power-on reset circuit.

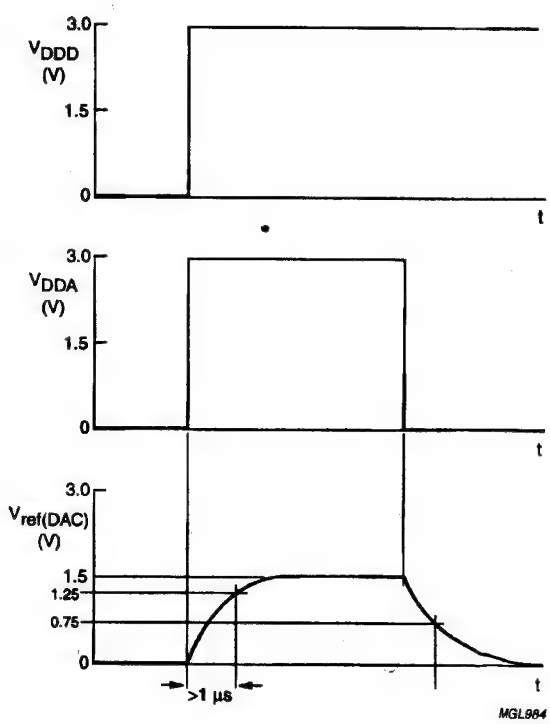


Fig.4 Power-on reset timing.

8.6 Feature settings

8.6.1 DIGITAL INTERFACE FORMAT SELECT

The digital audio interface formats (see Fig.5) can be selected via pins SFOR1 and SFOR0 as shown in Table 4.

For the digital audio interface holds that the BCK frequency can be maximum 64 times WS frequency.

The WS signal must change at the negative edge of the BCK signal for all digital audio formats.

Table 4 Data format selection

SFOR1	SFOR0	INPUT FORMAT
LOW	LOW	I^2S-bus input
LOW	HIGH	LSB-justified 16 bits input
HIGH	LOW	LSB-justified 20 bits input
HIGH	HIGH	LSB-justified 24 bits input

8.6.2 DE-EMPHASIS CONTROL

This function is only available in audio mode. In that case, pin DEEM/CLKOUT can be used to activate the digital de-emphasis for 44.1 kHz as given in Table 5.

Table 5 De-emphasis control (audio mode)

DEEM/CLKOUT	FUNCTION
LOW	de-emphasis off
HIGH	de-emphasis on

8.6.3 MUTE CONTROL

The output signal can be soft muted by setting pin MUTE to HIGH as given in Table 6.

Table 6 Mute control

MUTE	FUNCTION
LOW	mute off
HIGH	mute on

Low power audio DAC with PLL UDA1334ATS

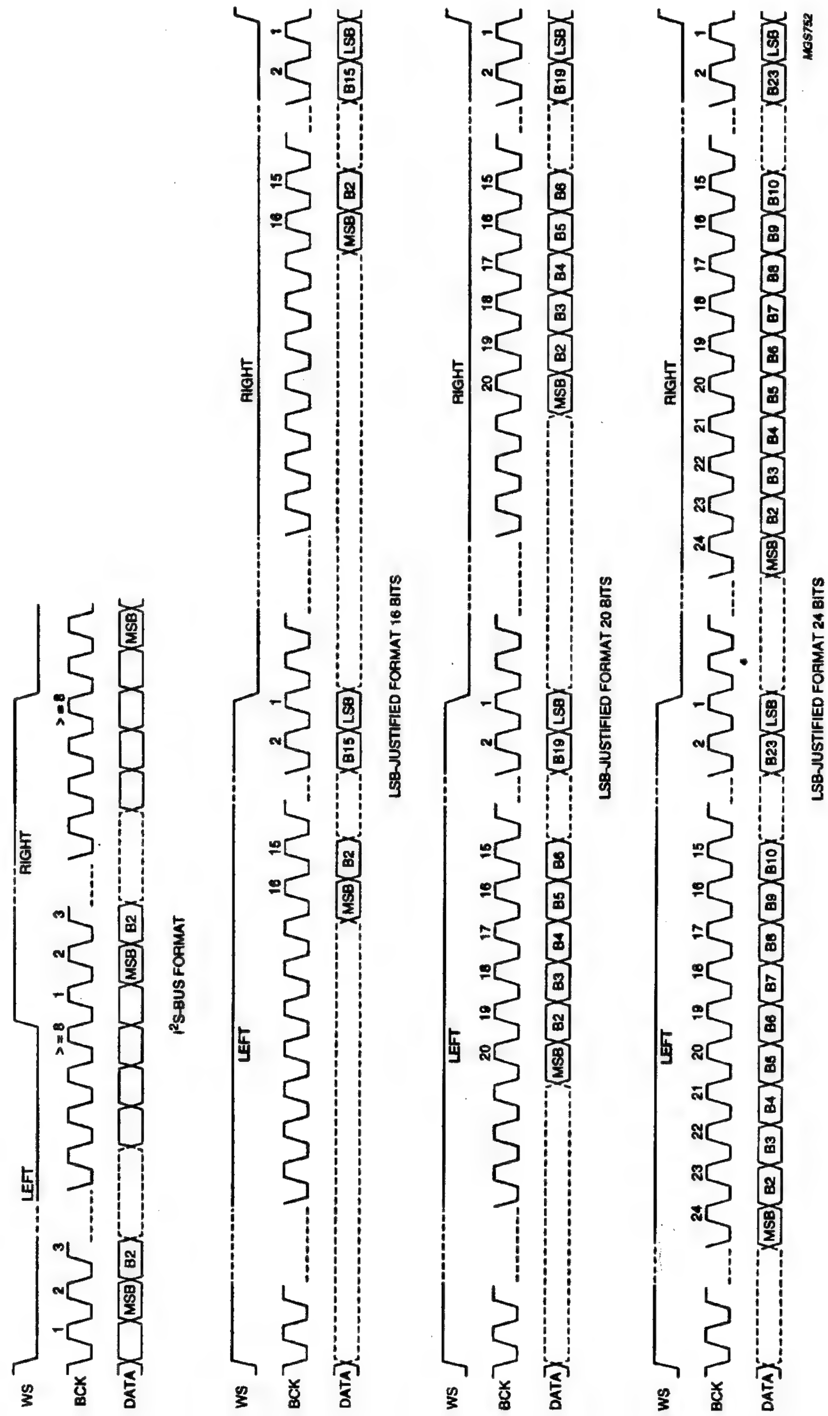


Fig.5 Digital audio formats.

9.11 IC's Progressive Scan

9.11.1 FLI2200

FLI2200

Description

The FLI2200 is a single chip implementation of Faroudja Laboratories' award winning deinterlacing and post-processing algorithms that produce the highest quality progressive video output from a variety of interlaced video inputs including 525/60 (NTSC) or 625/50 (PAL or SECAM). It uses patented and patent pending motion-adaptive deinterlacing that selects the optimal filtering on a per-pixel basis. This includes detection and proper interleaving of 3:2 and 2:2 pulldown for film-base sources, including continuous monitoring and compensation for bad edits that occur frequently in broadcast material due to poor scene cuts or insertion of commercials. Video material is processed by a set of content-sensitive spatio-temporal filters that adapt to the appropriate direction for smoothest interpolation using the patented Faroudja DCDi™ algorithm. The FLI2200 also includes motion-adaptive cross-color suppression that removes highly objectionable coloration artifacts produced by commonly used video decoders. Its internal processing uses 10 bits per channel to maintain the highest quality. Its inputs and outputs are 10 bits/channel for best quality but also supports 8 bits/channel for more cost-sensitive applications. The FLI2200 requires 4 MB of low cost SDRAM for best quality deinterlacing, but it can also be operated in an optimized intra-field mode without memory for more cost-sensitive applications. This makes possible the use of a single design for both high-end and low-end applications.

The FLI2200 integrates a number of functions to provide maximum flexibility in a low cost configuration. This includes an on-chip clock generator, SDRAM controller, display controller, input and output color-space converters. It uses a standard 2-wire serial control interface for easy control and access to the registers.

The FLI2200 can be connected without glue logic to the FLI2000 video decoder and FLI2220 Enhancer and OSD Generator to produce the highest quality video pipeline for premium applications. It is also fully compatible with other decoders having a ITU-R BT 656 output format.

Applications

Flat panel TV – LCD, PDP

Progressive scan TVs

Multimedia front/rear projectors

Home Theater

Scan Converters

Multimedia PCs/Workstations

DCDi™ is a Faroudja trademark

Features

Motion-adaptive cross-color suppression removes artifacts produced by improper Y/C separation in low-cost video decoders

Motion-adaptive video deinterlacing selects optimal filtering on a per-pixel basis

- Film-mode for proper handling of 3:2 and 2:2 pulldown material
- Bad-edit detection/correction compensates for poor scene cuts and insertions common in broadcast material
- Motion-weighted interpolation for video sources produces maximum resolution without introducing motion artifacts
- Directional Correlational Deinterlacing (DCDi™) minimizes jaggies on angled lines

8/10-bit Y/Cb/Cr (D1) (ITU-R BT 656), 16/20-bit Y Cb/Cr (ITU-R BT 601), 24/30-bit RGB or YCbCr/YPbPr interlaced input options

? Supports 525/60 (NTSC), 625/50 (PAL/SECAM)

? Accepts up to 1100 pixels/line

8/10-bit, 16/20-bit YUV, 24/30-bit RGB or YCbCr/YPbPr progressive output options

Supports 8- or 10-bit inputs and outputs

10-bit internal processing for highest quality

Includes color-space converters at input and output for maximum flexibility

Auto-detection of NTSC/PAL/SECAM inputs

High-order filtering produces smooth chroma output in 4:2:2 to 4:4:4 or 4:4:4 to 4:2:2 conversions

Resolution recovery maximizes output signal-to-noise ratio and dynamic range

Can be operated without glue logic with FLI2000 Video Decoder and FLI2220 Enhancer and OSD Generator ICs to produce highest quality video pipeline

Glue-less interface to most standard video decoders

Built-in display timing generator

On-chip clock generator eliminates external PLLs

On-chip SDRAM controller

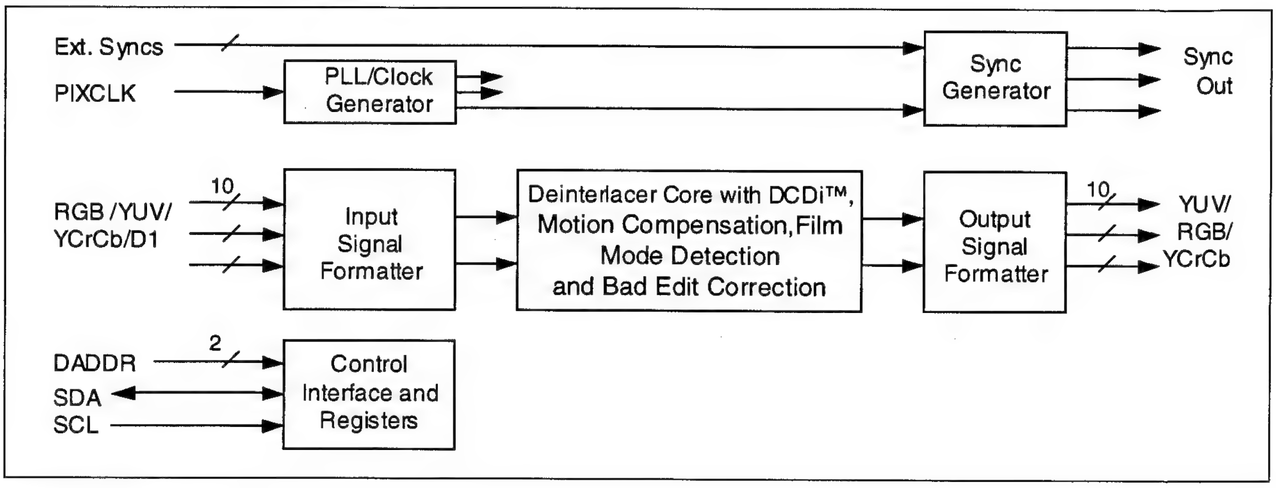
Uses low cost SDRAM as field memory – 4 MB

Optimized intra-field operation allows memory-less configuration for lowest cost applications with same design and layout as for high-end applications

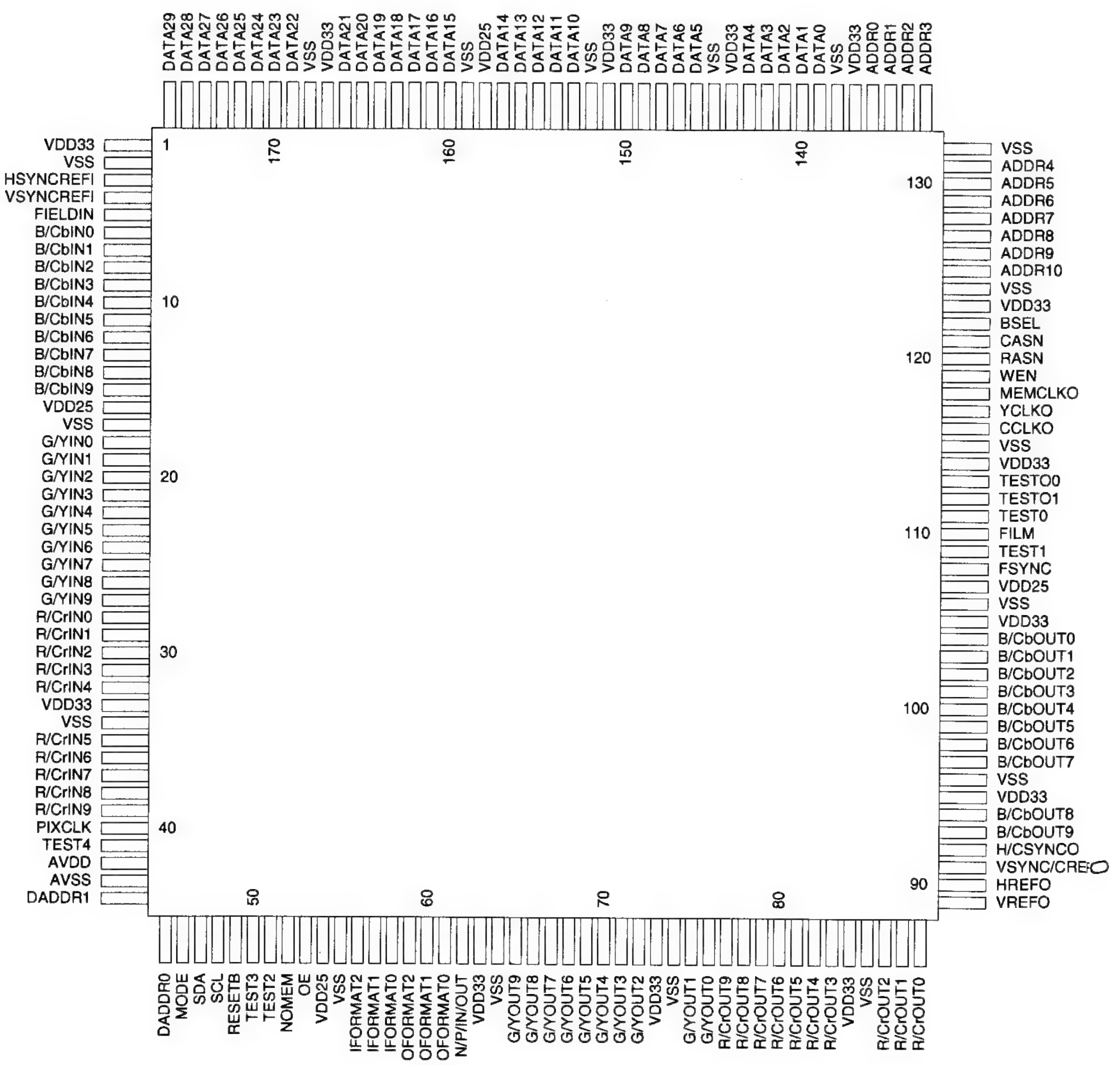
2-wire serial control interface for easy control

176-pin TQFP package

Simplified Block Diagram



Pin description



Pin Connections and Functions

Pin #	Name	Description
See list	V_{SS}	Ground connections. Connect to the digital ground plane. Pins: 2, 17, 34, 55, 64, 74, 85, 96, 106, 115, 124, 132, 138, 145, 152, 159, 168
See list	V_{DD33}	Pad Ring digital power connections. Connect to the digital 3.3 volt power supply and decouple to the digital ground plane. Pins: 1, 33, 63, 73, 84, 95, 105, 114, 123, 137, 144, 151, 167
See list	V_{DD25}	Core Logic digital power connections. Connect to the digital 2.5 volt power supply and decouple to the digital ground plane. Pins: 16, 54, 107, 158
43	AV_{SS}	Ground connection for the clock PLL circuits. Connect to the digital ground plane
42	AV_{DD}	Analog power connections for the clock PLL circuit. Connect to a separately decoupled 2.5 volt power supply and decouple directly to the AV_{SS} pin..
49	RESETB	Reset. When this input is set low it will reset all the internal registers to the default states. Refer to the section on the control registers for details of these states. The device must be reset after it is powered-up.
53	OE	When this pin is set high the outputs of the FLI2200 will be enabled; when it is set low the outputs will be set into a high-impedance state.
56-58	$IFORMAT_{2-0}$	Input signal format control. The settings of these pins set the format of the input signal. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details.
59-61	$OFORMAT_{2-0}$	Output signal format control. The settings of these pins set the format of the output signal. This can be overridden by the OFmtOvr bit, bit 3 in register 07_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 07_H for details.
44-45	$DADDR_{1-0}$	The settings of $DADDR_{1-0}$ allow the device address of the control bus to be programmed to prevent conflict with the other devices connected to the bus. $DADDR_{1-0}$ allow the device address to be set to any of the following values: $C0/C1_H$, $C2/C3_H$, $E0/E1_H$, $E2/E3_H$. Please refer to the section "Control Bus Operation and Protocol" for further information.
46	MODE	When this pin is set low the control bus will operate in the slave mode; allowing the device to programmed from an external controller. When it is set high the FLI2200 will self-program from an external I^2C memory connected to the bus. Please refer to the "Control Bus Operation and Control Protocol" section for more details.
47	SDA	2-wire serial control bus data. Data can be written to the control registers via this pin when it is in the input mode and data can be read from the status registers when it is in the output mode. Refer to the section on the serial port for timing and format details and to the section on the registers for programming information.
48	SCL	2-wire serial control bus clock. When the control port operates in slave mode this pin will be an input and when it operates in the self programming mode it will be an output.
40	PIXCLK	Pixel clock input. This clock is used to drive all the circuits in the FLI2200. An internal PLL is used to upconvert this clock to provide the master clock signal and other clocks used internally. Note that when the FLI2200 is used in the D1 input mode the PIXCLK input should run at the rate of two cycles per pixel (one for luma and one for chroma).
62	N/P/IN/OUT	NTSC/PAL input or output. The default function of this pin is NTSC/PAL signal indicator output. When the input video signal is a 525 line signal this pin will be set high and when it is a 625 line signal the pin is set low. This function of this pin can be programmed to be an input according to the setting of this pin if the $NPOp_{1-0}$ bits, bits 5-4 in register 03_H, are set to 00_H, overriding the internal line counter. i.e., it will treat the signal as a 525 line signal when it is set high and a 625 line signal when it is set low.

Pin #	Name	Description
[redacted]		
52	NOMEM	No Memory Mode control input. This pin controls the operation of the FLI2200 as follows: When this pin is set low the device is used with external field memories and operates in the full set of deinterlacing modes, i.e., motion adaptive video deinterlacing and full frame film source deinterlacing using 3:2 pulldown detection (2:2 pulldown for 625/50 sources). When this pin is set high the FLI2200 is forced into the intra-field only deinterlacing mode, which requires no external memories, allowing the FLI2200 to be used in low-cost applications where the ultimate video quality is not a requirement. ***To ensure proper startup of the SDRAMs this pin should be set high during the power-up sequence.*** This can be overridden by the NMOvr bit, bit 1 in register 05_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 05_H for details.
[redacted]		
27-18	$G/YIN_{9\text{-}0}$	10-bit green or luminance signal input bus. The mode is set by the $IFORMAT_{2\text{-}0}$ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details. This signal is sampled on the rising edge of PIXCLK.
15-6	$B/CbIN_{9\text{-}0}$	10-bit blue or Cb chroma signal input bus. The mode is set by the $IFORMAT_{2\text{-}0}$ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details. Bits 6, 4 and 3 in register 08_H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr and Y Pb Pr modes the Cb or Pb signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
39-35 32-28	$R/CrIN_{9\text{-}0}$	10-bit red or Cr chroma signal input bus. The mode is set by the $IFORMAT_{2\text{-}0}$ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details. Bits 6, 4 and 3 in register 08_H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr mode the Cr signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
3	HSYNCREFI	Horizontal sync or reference. The horizontal sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00_H. The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
4	VSYNCREFI	Vertical sync or reference. The vertical sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00_H. The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
5	FLDIN	Field identifier input. The field identifier output of the source signal should be connected to this pin. A low setting signifies an even field and a high level signifies an odd field. When bit 4 in register 00_H is set low, the input timing is based on HREF and VREF and this signal is required. When this bit is set high the input timing is based on HSYNC and VSYNC and this signal is generated internally and is not required. When bit 5 in register 06 is set high this signal is also used as the frame boundary identifier for 30 Hz film sources.

Pin #	Name	Description
65-72 75-76	$G/YOUT_{9\text{-}0}$	Green or luminance output bus. In the RGB mode this output is the Green signal and in the YCbCr mode it is the Y signal. The mode is set by the $OFORMAT_{2\text{-}0}$ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 07_H for details. The signal is clocked out on the falling edge of YCLKO.
93-94 97-104	$B/CbOUT_{9\text{-}0}$	Blue or Cb chrominance output bus. In the RGB mode this output is the Blue signal, in the Y Cb Cr mode it is the Cb signal. The mode is set by the $OFORMAT_{2\text{-}0}$ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 07_H for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08_H. The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
77-83 86-88	$R/CrOUT_{9\text{-}0}$	Red or Cr chrominance output bus. In the RGB mode this output is the Red signal, in the YCbCr mode it is the Cr signal. The mode is set by the $OFORMAT_{2\text{-}0}$ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 07_H for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08_H. The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
116	CCLKO	Chroma output sampling clock. This clock is derived from PIXCLK and will be at half the frequency of YCLKO. In 30-bit 4:2:2 output mode the chroma output signals will change on the falling edge of YCLKO prior to the next rising edge this clock.
117	YCLKO	Luma output sampling clock. This clock is derived from PIXCLK and is double the frequency of PIXCLK. In 30-bit and 20-bit output modes the output signals will change on the falling edge of this clock.
89	VREFO	Start of active field or frame indicator. This signal goes high to indicate the first active line in each field or frame and goes low during the vertical blanking interval. The polarity and timing of this signal are programmable.
90	HREFO	Start of active line indicator output. This signal goes high to indicate the first active pixel in each line and goes low during the horizontal blanking interval. The polarity and timing of this signal are programmable.
91	VSYNC/ CREFO	Vertical sync output. This signal provides the vertical sync function for the outputs. Its polarity is programmable to be active high or active low. It can also be programmed to be a composite reference for applications requiring this instead of sync.
92	H/CSYNCO	Horizontal or composite sync output. This signal provides the horizontal sync function for the outputs. Its polarity is programmable to be active high or active low. This signal can also be programmed to be the composite sync output, CSYNC.
108	FSYNC	Film mode sync output. When film mode is detected this pin will toggle in sync with the 3:2 (NTSC) or 2:2 (PAL and 30 Hz film in NTSC) pulldown sequence detected in the source.
110	FILM	Film mode detector output. This pin will be set high when the FLI2200 detects that the video input was converted from 24 fps film with a telecinė machine. If film mode is not detected this pin will be set low.

Pin #	Name	Description
125-131 133-136	$ADDR_{10\text{-}0}$	SDRAM Address bus. This signal bus is used to address the external SDRAM(s) used for field memories. It should be connected to the $A_{10\text{-}0}$ bus of the memory chip(s). Please refer to the Applications section of this data sheet for further details.
176-169 166-160 157-153 150-146 143-139	$DATA_{29\text{-}0}$	SDRAM Data bus. This signal bus is used to transfer the data to and from the external SDRAM(s) used for field memories. It should be connected to the $DQ_{29\text{-}0}$ bus of the memory chip when using a 64 Mbit SDRAM. When using two 16 Mbit SDRAMs this 30-bit bus may be connected to the two 16-bit data busses of the memories in two ways: either connect 16 lines to one chip and 14 to the other, or connect 15 to both. In all cases the two unused data lines on the memory chip(s) should be connected to ground via 22 k? resistors. Please refer to the Applications section of this data sheet for further details.
118	MEMCLKO	SDRAM clock and 2x output sampling clock. This clock is derived from PIXCLK and will be at double the frequency of YCLKO. This active signal should be connected to the CLK pin(s) on the SDRAM(s). When the 10-bit output mode selected the output signals will also change at this clock rate and this should then be used as the output clock..
119	WEN	SDRAM Write Enable. This active low signal should be connected to the WE pin(s) on the SDRAM(s).
120	RASN	SDRAM Row Address Select. This active low signal should be connected to the RAS pin(s) on the SDRAM(s).
121	CASN	SDRAM Column Address Select. This active low signal should be connected to the CAS pin(s) on the SDRAM(s).
122	BSEL	SDRAM Bank Select. When using two 16 Mbit SDRAMs this signal should be connected to the BA (also called BS or A_{11}) pin on both SDRAMs. When using a 64 Mbit SDRAM this signal should be connected to the BA0 (also called BS0 or A_{11}) pin on the SDRAM and BA1/ BS1 (also called BA when BA0 is referred to as A_{11}) should be tied low.
41, 50, 51, 109, 111	$TEST_{4\text{-}0}$	These pins are used for test purposes only and should always be tied low for normal operation.
112, 113	$TESTO_{1\text{-}0}$	These pins are test outputs and should be left unconnected in normal operation.

9.11.2 ADV7196

ADV7196A

INPUT FORMATS
- YCrCb in 2x10-Bit (4:2:2) or 3x10-Bit (4:4:4) format compliant to SMPTE-293M (525p), ITU-R.BT1358 (625p), SMPTE274M (1080i), SMPTE296M (720p) and any other High Definition standard using Async Timing Mode
- RGB in 3x10 Bit 4:4:4 format

OUTPUT FORMATS
- YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
- YPrPb HDTV (EIA 770.3)
- RGB levels compliant to RS-170 and RS-343A
- 11-Bit + Sync (DAC A)
- 11-Bit DACs (DAC B, DAC C)

PROGRAMMABLE FEATURES
Internal Testpattern Generator with Color Control
Y/C delay (+/-)
Gamma Correction
Individual DAC on/off control
54MHz Output (2xOversampling)
Sharpness filter with programmable gain/attenuation
Programmable Adaptive Filter Control
Undershoot Limiter
VBI Open Control
I2C Filter

Macrovision Rev 1.0 (525p)
CGMS-A (525p)
2 Wire Serial MPU Interface

Single Supply +3.3 V Operation
52-MQFP package

APPLICATIONS
Progressive Scan / HDTV Display Devices
DVD Players
Progressive Scan/HDTV Projection Systems
MPEG2@81MHz
Digital Video Systems
High Resolution Color Graphics
Image Processing/ Instrumentation
Digital Radio Modulation/ Video Signal Reconstruction

GENERAL DESCRIPTION
The ADV7196A is a triple high speed, digital-to-analog encoder on a single monolithic chip. It includes of three high speed video D/A converters with TTL compatible inputs.

The ADV7196A has three separate 10-Bit wide input ports which accept data in 4:4:4 10-Bit YCrCb or RGB or 4:2:2 10-Bit YCrCb. This data is accepted in progressive scan format at 27MHz or HDTV format at 74.25MHZ or 74.1758MHz. For any other High Definition standard but SMPTE 293M, ITU-R BT.1358, SMPTE274M or SMPTE296M the Async Timing Mode can be used to input data to the ADV7196A. For all standards, external horizontal, vertical and blanking signals or EAV/SAV codes control the insertion of appropriate synchronisation signals into the digital data stream and therefore the output signals.

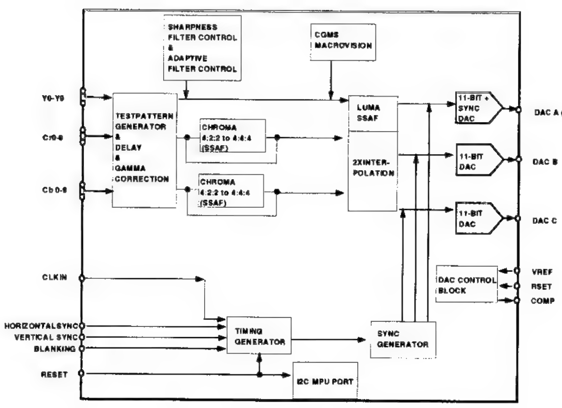
The ADV7196A outputs analog YPrPb progressive scan format complying to EIA770.1, EIA 770.2 or YPrPb HDTV complying to EIA 770.3 or RGB complying to RS-170/RS 343A.

The ADV7196A requires a single 3.3V power supply, an optional external 1.235 V reference and a 27 MHz clock in Progressive Scan Mode or a 74.25MHz (or 74.1758MHz) clock in HDTV mode.

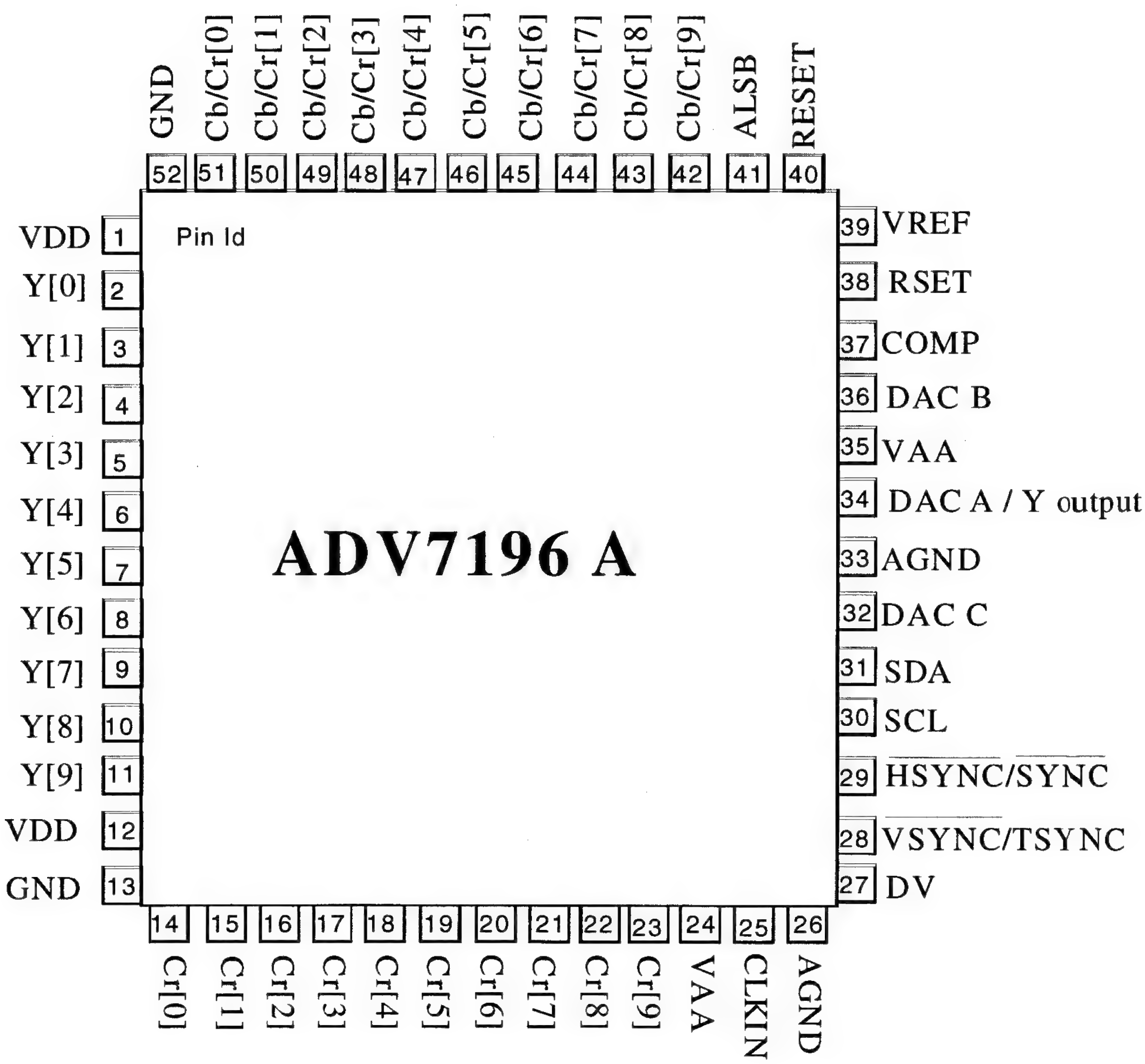
In Progressive Scan Mode, a Sharpness Filter with programmable gain allows high frequency enhancement on the luminance signal. Programmable Adaptive Filter Control which may be used, allows removal of ringing on the incoming Y data. The ADV7196A supports CGMS-A data control generation and the Macrovision Anticopy algorithm in 525p mode.

The ADV7196A is packaged in a 52-Pin MQFP package.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Mnemonic	Input/Output	Function
GND	G	Digital Ground
AGND	G	Analog Ground
ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address. When this pin is tied high the I2C filter is activated which reduces noise on the I2C interface. When this pin is tied low, the input bandwidth on the I2C lines is increased.
DV	I	Video Blanking Control Signal Input.
CLKIN	I	Pixel Clock Input. Requires a 27MHz reference clock for standard operation in Progressive Scan Mode or a 74.25MHz (74.1758MHz) reference clock in HDTV mode.
COMP	O	Compensation Pin for DACs. Connect 0.1µF Capacitor from COMP pin to V_{AA}.
DAC A	O	Y analog output.
DAC B	O	Color component analog output of input data on Cr 9-0 input pins.
DAC C	O	Color component analog output of input data on Cb/Cr 9-0 input pins.
HSYNC/ SYNC	I	HSYNC, horizontal sync control signal input or SYNC input control signal in Async Timing Mode.
Cr 9-0	I	10-Bit Progressive scan/ HDTV input port for color data in 4:4:4 input mode. In 4:2:2 mode this input port is not used. Input port for R data when RGB data is input.
Cb/Cr 9-0	I	10-Bit Progressive scan/ HDTV input port for color data. In 4:2:2 mode the multiplexed CrCb data must be input on these pins. Input port for B data when RGB is input.
RESET	I	This input resets the on-chip timing generator and sets the ADV7196A into Default Register setting. Reset is an active low signal.
R_{SET}	I	A 2470 Ohms resistor (for input ranges 64-940 and 64-960, output standards EIA770.1-3)must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs. For input ranges 0 -1023 (RS-170,RS-343A) the R_{SET} value must be 2820 Ohms.
SCL	I	MPU Port Serial Interface Clock Input
SDA	I/O	MPU Port Serial Data Input/Output
VSYNC/ TSYNC	I	VSYNC , vertical sync control signal input or TSYNC input control signal in AsyncTiming Mode.
V_{DD}	P	Digital power supply
V_{AA}	P	Analog power supply
V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235V).
Y9 -Y0	I	10-Bit Progressive scan/ HDTV input port for Y data. Input for G data when RGB data is input.

9.12 List of Abbreviations

9.12.1 Digital Board

+12V	+12V Power Supply
+3V3	+3V3 Power Supply
+5V	+5V Power Supply
+5V_BUFFER	+5V Power Supply for Video Filters
24M576_OUT	24M576 X-tal frequency output from Video Input Processor
27M_CLK_PS	27MHz clock to Progressive Scan
5505_HS	Horizontal Synchronisation from Host Decoder to Progressive Scan
5505_ODD_EVEN	Odd - Even control from Host Decoder to Progressive Scan
5505_VS_PS	Vertical Synchronisation from Host Decoder to Progressive Scan
-5V	-5V Power Supply
ACC_ACLK_OSC	Audio Clock PLL output sync with incoming video for record
ACC_ACLK_PLL	Audio Clock PLL output for play back
AD_ACLK	Audio Decoder Clock
AD_BCLK	Audio Decoder I2S bit clock
AD_DATA(0:2)	Audio Decoder data (PCM)
AD_SPDIF	Audio digital output to the analog board
AD_WCLK	Audio Decoder I2S word clock
ADC_ENABLEN	Analog Digital converter enable
AE_BCLK	Audio Encoder I2S bit clock
AE_CSN	Audio Encoder chip select(LOW active)
AE_DATAI	Audio Encoder I2S data input from analog board
AE_DATAO	Compressed I2S audio data from DSP to Host Decoder
AE_IRQN	Audio Encoder interrupt request
AE_WCLK	Audio Encoder I2S word clock
ANA_WE	Analog write enable
B_IN_7118	Video blue input to Video Input Processor
B_OUT	Video blue output from Host Decoder
B_OUT_B	Filtered blue video output
BCLK_CTRL	Basic Engine I2S Bit clock control
BE_BCLK	Basic Engine I2S bit clock
BE_BCLK_VSM	Basic Engine I2S bit clock to VSM
BE_CPR	Basic Engine Control Processor ready to accept data
BE_DATA_RD	Basic Engine Data read
BE_DATA_WR	Basic Engine Data write
BE_FAN	Basic Engine FAN
BE_FLAG	Basic Engine error flag
BE_IRQ	Basic Engine interrupt request
BE_LOADN	Basic Engine LOAD(LOW active)
BE_RXD	Basic Engine S2B received data
BE_SUR	Basic Engine servo unit ready to accept data (S2B)
BE_SYNC	Basic Engine sector/abs time sync
BE_TXD	Basic Engine S2B transmitted data
BE_V4	Basic Engine versatile input pin
BE_WCLK	Basic Engine I2S word clock
C_IN	Video Chrominance input
C_IN_7118	Chrominance input to Video Input Processor
C_OUT	Chrominance output from Host Decoder
C_OUT_B	Filtered Chrominance output
CENTRE_ON_STEREO	Control signal from Host Decoder to AV board to switch Stereo Output cinch to mono.
COAX_IN	Coaxial input
CPU_ANALYSE	Control processor unit analyse
CPU_RESET	Control processor unit reset
CPUINT(0-1)	Control processor unit interrupt
CTS1P	Clear to send (Service Interface)
CVBS_OUT	Composite video output out of the Host Decoder
CVBS_OUT_B	Filtered Composite video output
CVBS_OUT_B_7118	Composite video output to Video Input Processor(digital board video loop)
CVBS_Y_IN	Composite video/Luminance input
CVBS_Y_IN_7118_A	Composite video/Luminance input to Video Input Processor
CVBS_Y_IN_7118_B	Composite video/Luminance input to Video Input Processor
CVBS_Y_IN_7118_C	Composite video/Luminance input to Video Input Processor
D_PAR_D(7:0)	Front-end parallel interface data (record)
D_PAR_DVALID	Front-end parallel interface data valid
D_PAR_REQ	Front-end parallel interface request
D_PAR_STR	Front-end parallel interface strobe
D_PAR_SYNC	Front-end parallel interface sync
D_V4	Digital versatile input pin Front-end I2S versatile signal
D_WCLK	Front-end I2S word clock
DSP_A(0-9)	Digital sound processor address bus
DSP_CE	Digital sound processor chip enable
DSP_D(0-23)	Digital Sound Processor data bus
DSP_MA16	Digital Sound Processor Memory Address 16 line
DSP_RDN	Digital Sound Processor read enable(LOW active)
DSP_WRN	Digital Sound Processor write enable(LOW active)
DV_IN_CLK	Digital Video in clock from DVIO board
DV_IN_DATA(7:0)	Digital Video in data bus from DVIO
DV_IN_HS	Digital Video in horizontal synchronisation from DVIO
DV_IN_VS	Digital Video in vertical synchronisation from DVIO
EMI_A(1-21)	External Memory Interface Address Bus(Host Decoder)
EMI_BE1N	External Memory Interface Upper byte enable(Host Decoder)
EMI_BEON	External Memory Interface Lower byte enable(Host Decoder)
EMI_CASN	External Memory Interface SDRAM column address strobe(Host Decoder)
EMI_CE1N	External Memory Interface VSM Lower bank enable
EMI_CE2N	External Memory Interface VSM Higher bank enable
EMI_CE3N	External Memory Interface flash IC's enable
EMI_D(0-15)	External Memory Interface Data Bus(Host Decoder)
EMI_OEN	External Memory Interface Output enable(Host Decoder)
EMI_PROCCLK	External Memory Interface Processor Clock(Host Decoder)
EMI_RASN	External Memory Interface SDRAM row address strobe(Host Decoder)
EMI_RWN	External Memory Interface Read/ Write control signal(Host Decoder)
EMI_WAIT	External Memory Interface Wait state request(Host Decoder)
ERROROUT	Control port P3 I/O from Host Decoder

FB	Fast Blanking
FLASH_OEN	FLASH output enable control signal
G_IN_7118	Video green input to Video Input Processor
G_OUT	Video green output from Host Decoder
G_OUT_B	Filtered green video output from Host Decoder
HD_M_AD(11:0)	Host Decoder SDRAM address bus
HD_M_CASN	Host Decoder SDRAM column address strobe
HD_M_CLK	Host Decoder SDRAM clock
HD_M_CSN	Host Decoder SDRAM chip select
HD_M_DQ(15:0)	Host Decoder SDRAM data bus
HD_M_DQML	Host Decoder SDRAM data mask enable(Lower)
HD_M_DQMU	Host Decoder SDRAM data mask enable(Upper)
HD_M_RASN	Host Decoder SDRAM row address strobe
HD_M_WEN	Host Decoder SDRAM write enable
ION	Inverted ON: Enable the power supply for the digital board when LOW
IRESET_DIG	Initialisation of the digital board, high when power on
JTAG_TCK	JTAG Test Clock
JTAG_TD_AE_TO_CON	JTAG Transmitted Data Audio Encoder to Connector
JTAG_TD_CON_TO_AE	JTAG Transmitted Data Connector to Audio Encoder
JTAG_TD_CON_TO_HD	JTAG Transmitted Data Connector to Host Decoder
JTAG_TD_CON_TO_VSM	JTAG Transmitted Data Connector to Versatile Stream Manager
JTAG_TD_HD_TO_CON	JTAG Transmitted Data Host Decoder to Connector
JTAG_TD_VE_TO_CON	JTAG Transmitted Data Video Encoder to Connector
JTAG_TD_VIP_TO_VE	JTAG Transmitted Data Video Input Processor to Video Encoder
JTAG_TD_VSM_TO_VIP	JTAG Transmitted Data Versatile Stream Manager to Video Input Processor
JTAG_TMS	JTAG Test Mode Select
JTAG_TRSTN	JTAG Test part ResetN
LOAD_DVN	LOAD Digital Video(LOW active)
MUTEN	Mute enable
OPT_IN	Audio Optical in
R_IN_7118	Video Red input to Video Input Processor
R_OUT	Video red output from Host Decoder
R_OUT_B	Filtered red Video output from Host Decoder
RESETN_5505	Reset Host Decoder
RESETN_BE	System reset basic engine
RESETN_DSP	System reset Digital Sound Processor
RESETN_DVIO	System reset Digital Video Input Output
RESETN_EMPIRE	Hardware reset input(active LOW) of the EMPIRE
RESETN_VIP	System reset Video Input Processor
RESETN_VSM	System reset Versatile Stream Manager
RESN_BEN	Reset Basic Engine
RESN_DSP	Reset Digital Sound Processor
RTS1P	Ready To Send data to service serial interface
RX1P	Receive data from service serial interface
SCL	I2C bus clock
SDA	I2C bus data
SEL_ACLK(1-2)	Select audio clock(playback)
SERVICES	Control signal of service serial interface
SYSCLK_5505	Video system Clock Host Decoder
SYSCLK_VSM	System clock Versatile Stream Manager
TX1P	Transmit data to service serial interface
U_IN	Video U input
U_IN_7118	Video U input to Video Input Processor
V_IN	Video V input
V_IN_7118	Video V input to Video Input Processor
VCC3_CLK_BUF	Power supply 3V3 clock buffer
VCC3_VE_MEM	Power supply 3V3 Video Encoder Memory
VCC3_VSM	Power supply 3V3 Versatile Stream Manager
VCC3_VSM_MEM	Power supply 3V3 Versatile Stream Manager Memory
VCC5_4046	Power supply 5V to PLL IC7806
VDD_EMPIRE	Power Supply of EMPIRE IC
VDD_MEM	Power Supply for Host Decoder flashes(7302,7304)
VDD_MEM1	Power Supply for Host Decoder DRAMS(7300, 7301)
VDD_MEM2	Power Supply for Host Decoder SDRAM's(7306 and 7307)
VDD_STI	Power Supply for Host Decoder
VDD5_MK2703	Power supply +5V IC7800
VDD5_OSC	Power supply +5V IC7802
VDDE_7118	Power supply +3V3 Video Input Processor
VDDE_LVC32	Power supply +3V3 IC7551
VDSP	Power supply +3V3 Digital Sound Processor
VE_DATA(15:0)	Video Encoder data Bus
VE_DSN	Video Encoder Data Strobe
VE_DTACKN	Video Encoder Data Transfer acknowledge
VE_M_A(8:0)	Video Encoder Memory address bus
VE_M_CASN	Video Encoder DRAM column address strobe
VE_M_D(63:0)	Video Encoder DRAM data Bus
VE_M_OEN	Video Encoder DRAM output enable
VE_M_RASN	Video Encoder DRAM row address strobe
VE_M_WEN	Video Encoder DRAM write enable
VIP _ICLK	Video Input Processor input Clock
VIP_ERROR	Video Input Processor error
VIP_FB	Video Input Processor Fast Blanking
VIP_HS	Video Input Processor horizontal synchronisation
VIP_IGP1	Video Input Processor input general purpose 1
VIP_RTS	Video Input Processor ready to send
VIP_VS	Video Input Processor vertical synchronisation
VIP_YUV(7:0)	Video Input Processor digital video(CC7R 656)
VSM_M_A(13:0)	Versatile Stream Manager SDRAM address
VSM_M_CASN	Versatile Stream Manager SDRAM column address strobe
VSM_M_CLKEN	Versatile Stream Manager SDRAM clock enable
VSM_M_CLKOUT	Versatile Stream Manager SDRAM clock out

VSM_M_D(0-15)	Versatile Stream Manager SDRAM data bus
VSM_M_LDQM	Versatile Stream Manager SDRAM lower data mask enable
VSM_M_RASN	Versatile Stream Manager SDRAM row address strobe
VSM_M_UDQM	Versatile Stream Manager SDRAM upper data mask enable
VSM_M_WEN	Versatile Stream Manager SDRAM write enable
VSM_UART_CTSN1	Versatile Stream Manager UART clear to send to analog board UART1
VSM_UART_CTSN2	Versatile Stream Manager UART clear to send to DVIO UART2
VSM_UART_RTSN1	Versatile Stream Manager UART ready to send to analog board UART1
VSM_UART_RTSN2	Versatile Stream Manager UART ready to send to DVIO UART2
VSM_UART_RX1	Versatile Stream Manager UART received data to analog board UART1
VSM_UART_RX2	Versatile Stream Manager UART received data to DVIO UART2
VSM_UART_TX1	Versatile Stream Manager UART transmitted data to analog board UART1
VSM_UART_TX2	Versatile Stream Manager UART transmitted data to DVIO UART2
Y_IN	Luminance input from analog board
Y_IN_7118	Luminance input to Video Input Processor
Y_OUT	Luminance output from Host Decoder
YC(0-7)	Digital Video Bus for progressive scan board

9.12.2 Divio Board

+35V_DV_EDO	+3V3 Power supply EDO Bus IC7404
+3V3_DLY	+3V3 Power supply for IC7500
+3V3_DV	+3V3 Power supply for IC7404
+3V3_FPGAINT	+3V3 Internal Power supply for IC7303
+3V3_FPGAIO	+3V3 Power supply for I/O pins of IC 7303
+3V3_IEEE	+3V3 Isolated Power supply for PHY domain
+3V3_LINK	+3V3 Power supply IC7103
+3V3_PLL	+3V3 Power supply IC7307 & IC7308
+3V3_SRAM	+3V3 Power supply IC7301, IC7302, IC7305 & IC7306
+5V_PROC	+5V Power supply IC7200, IC7201, IC7203 & IC7208
+VCC_DV_RAM	+3V3 Power supply for DV_RAM(IC7400--> IC7404)
1394_RSTN	Reset of LINK IC(7103) and PHY IC(7101)
A(0:8)	Address lines
AUD_BCLK	Audio Bit Clock
AUD_MUTE	Audio Mute
AUD_SDI	Audio Serial Data Input
AUD_SDO	Audio Serial Data Output
AUD_WS	Audio Word Select
BUFENN_AUD	Buffer Enable Audio
BUFENN_VID	Buffer Enable Video
CEN	Control Enable
CLK27M_CON	27MHz Clock to Digital Board
CLK27M_DV	27MHz Clock Digital Video Codec
CLK27M_OSC	27MHz Clock IC7304
CLOCKGENAUD	Clock generator Audio
CLOCKGENVID	Clock generator Video
CTSN	Clear to Send
DATA	Data from config ROM
DCLK	Data Clock from config ROM
DV_ASN	DVCODEC Address Strobe
DV_DRQN	DVCODEC Data Request Interrupt
DV_DSLN	DVCODEC Data Strobe Lower 8 bits
DV_DSUN	DVCODEC Data Strobe Upper 8 Bits
DV_DTACKN	DVCODEC Data Transfer Acknowledge
DV_ERRN	DVCODEC Error Interrupt
DV_HS_IN	DVCODEC Horizontal synchronisation In
DV_HS_OUT	DVCODEC Horizontal synchronisation Out
DV_LCN	DVCODEC Last Code Interrupt
DV_PDN	DVCODEC Power Down
DV_RSTN	DVCODEC System Reset for NW701
DV_RWN	DVCODEC Read/Write control signal
DV_VS	DVCODEC Vertical synchronisation
FIFOA_A(0:15)	FIFO buffer A Address bus
FIFOA_CEN(0:1)	FIFO buffer A Chip enable
FIFOA_D(0:7)	FIFO buffer A Data bus
FIFOA_OEN	FIFO buffer A Output enable
FIFOA_WEN	FIFO buffer A Write enable
FIFOB_A(0:15)	FIFO buffer B Address bus
FIFOB_CEN(0:1)	FIFO buffer B Chip enable
FIFOB_D(0:7)	FIFO buffer B Data bus
FIFOB_OEN	FIFO buffer B Output enable
FIFOB_WEN'	FIFO buffer B Write enable
HAD(0:7)	Host Address/Data bus for register settings of IC7404
INIT_CONFN	Initiate Configuration of IC7300
IO(0:30)	Data bus of IC7404
ISPN	In System Program Line(used for programming IC7203)
LCASN	Lower Column Address strobe for IC7404 DRAMS
LINKFIFO_DQ(0:7)	Audio/Video data
LINK_AVCLK	LINK IC Audio/Video Interface Clock
LINK_AVERR0	LINK IC indicates an CRC error
LINK_AVERR1	LINK IC Audio/Video sequence error
LINK_AVFSYNC	LINK IC Audio/Video frame sync
LINK_AVSYNC	LINK IC Audio/Video packet sync
LINK_AVVALID	LINK IC Audio/Video data valid
LINK_CSN	LINK IC chip select
LINK_CYCLEOUT	LINK IC Cycle clock
LINK_INTN	LINK IC interrupt
OE	Output enable
PA(0:15)	SRAM processor address
PAD(0:7)	SRAM processor data
PALE	Processor Address Latch Enable
PHY_CNA	PHY 1394 cable not active
PHY_LPS	LINK IC power status
PINT0N	Processor interrupt 0
PINT1N	Processor interrupt 1
PORT1_1	Unused free port
PPSENN'	Program store enable
PRDN	Processor read
PRSTN	Processor reset
PT0	Processor timer 0
PT1	Processor timer 1
PWRN	Processor write
RASN	Row address strobe
RESETN	DVIO board reset
RTSN	System Reset
RXD	Receive Data
SRAMCE0N	SRAM processor chip enable 0

SRAMCE1N	SRAM processor chip enable 1
SRAMRDN	SRAM processor output enable
TCK	Boundary scan Test Clock
TDI	Boundary scan Test Data Input
TDO	Boundary scan Test Data Output
TMS	Boundary scan Test Mode Select
TXD	Transmitted Data
UCASN	Upper column address strobe
WEN	Write Enable control signal to SRAM
YUV(0:7)	Digital Video
GND	Ground
GND_IEEE	Ground IEEE

9.12.3 Progressive Scan

+2V5_FLI	+2V5 Power Supply for IC7101
+2V5_PLL	+2V5 Power Supply for PLL
+3V3	+3V3 Power Supply
+3V3_ANA	+3V3 Power Supply Analogue
+3V3_DD	+3V3 Power Supply Digital
+3V3_FLI	+3V3 Power Supply for IC7101
+5V	+5V Power Supply
BA	Bank Address
CAS	Column Address strobe
CB_OUT(0:9)	Chrominance Blue out
CLK_27MHZ	27MHz Clock
CLK4	SDRAM clock
CR_OUT(0:9)	Chrominance Red out
D_ADDR(0:10)	Address bus
D_DATA(0:29)	Data bus
FRAME_IN	Picture FrAME
GND	Ground
HS_IN	Horizontal synchronisation IN
HSOUT	Horizontal synchronisation OUT
RAS	Row Address strobe
SCL	I2C bus clock
SDA	I2C bus data
VS_IN	Vertical synchronisation IN
VSOUT	Vertical synchronisation OUT
WE	Write Enable
Y_OUT(0:9)	Luminance output from FLI
YUV_IN(0:7)	Digital Video bus

10. Spare Parts List

VARIOUS

Various

0027	3104 120 00370	VIDEO PLUS EUR SILVER (/051)
0027	3104 120 00380	G-CODE ASIA SILVER (/691)
0027	3104 120 00390	SHOW VIEW EUR SILVER
0050	3104 120 00272	RW BADGE
0065	3104 127 11143	TRAY FRONT ASSY COMPLETE
0081	9305 025 81001	VAE8010/01
0151	3104 127 11162	COVER ASSY
0191	3104 124 07455	FILTER AIR INLED BOTTOM
0197	3104 123 30002	DUST FILTER
0198	3104 124 07733	FILTER AIR INLET COVER
0199	3104 128 93031	DC BRUSHLESS FAN
0251	3104 127 10740	FOOT SILVER ASSY
0252	3104 127 10740	FOOT SILVER ASSY
0253	3104 127 10740	FOOT SILVER ASSY
0254	3104 127 10740	FOOT SILVER ASSY
0309	3104 125 24080	UM DVDR1000/001 MID EU
0309	3104 125 24090	UM DVDR1000/051 UK
0309	3104 125 24100	UM DVDR1000/021 NORDIC
0309	3104 125 24120	UM DVDR1000/691 ASIA
0324	3111 170 21592	CORDON ANT. L.1,50M
1001	3104 128 06710	DVDR 4278 DIGITAL BOARD MODULE
1002	3122 427 22711	PSU DVDR1000-2 EURO 50PS203
1003	3103 608 50010	DVDR ANALOG BOARD EUROP
1005	3104 128 07760	DVDR 4316 DVIO BOARD
8001	3104 157 11641	CWAS FLEX DVD 22 70 32S
8002	3104 157 11641	CWAS FLEX DVD 22 70 32S
8003	3104 157 11790	CWAS SPLIT FLEX 30 100 32S
8004	3104 157 11531	CWAS FLEX DVD 10 110 32S
8013	3104 128 92921	CABLE IEEE-1394 4P AMP

TOOL	3104 128 07770	PCB EXTENDER DVIO ASSY

FRONT ASSY

Various

0001	3104 127 12993	FRONT & DOOR ASSY
0003	3104 127 12287	FRONT ASSY
0004	3104 127 12880	WINDOW ASSY
0006	3104 127 12292	HOLDER RIGHT COMPLETE
0010	3104 124 05450	LIGHT CONDUCTOR
0012	3104 127 12873	HOLDER LEFT COMPLETE
0014	3104 120 00340	WORDMARK PHILIPS SILVER
0016	4822 380 20505	LIGHT TRANSMITTER
0019	3104 127 11132	INNER DOOR ASSY
0020	3104 127 11912	INNER DOOR ASSY LEFT
0029	3104 124 07213	IR-WINDOW
0051	3104 127 11883	MOTOR ASSY
1004	3103 608 50030	DVDR DISPLAY BOARD
1006	3104 128 07610	PCB ASSY 4319 DVIO-FRONT

DISPLAY PWB

Various

1140	4822 276 13732	SWITCH TACT PUSH
1150	2422 086 10947	PROT DEV 65V 250MA PSC A
1153	5322 242 73686	CST12,00MTW-TF01
1156	2422 527 00513	BUZZER PIEZO CB13PA-X5
1157	4822 276 13732	SWITCH TACT PUSH
1158	4822 276 13732	SWITCH TACT PUSH
1159	4822 276 13732	SWITCH TACT PUSH
1160	4822 276 13732	SWITCH TACT PUSH
1161	4822 276 13732	SWITCH TACT PUSH
1162	4822 276 13732	SWITCH TACT PUSH
1163	4822 276 13732	SWITCH TACT PUSH
1165	4822 276 13732	SWITCH TACT PUSH
1166	4822 276 13732	SWITCH TACT PUSH
1167	4822 276 13732	SWITCH TACT PUSH
1168	4822 276 13732	SWITCH TACT PUSH
1169	4822 276 13732	SWITCH TACT PUSH
1170	4822 276 13732	SWITCH TACT PUSH
1171	4822 276 13732	SWITCH TACT PUSH
1172	4822 276 13732	SWITCH TACT PUSH
1173	4822 276 13732	SWITCH TACT PUSH
1174	4822 276 13732	SWITCH TACT PUSH
1175	4822 276 13732	SWITCH TACT PUSH
1176	4822 276 13732	SWITCH TACT PUSH
1177	4822 276 13732	SWITCH TACT PUSH
1178	2422 128 02947	SWI DET 1P 0,1A 30V SPP85
1179	2422 128 02947	SWI DET 1P 0,1A 30V SPP85
1910	2422 033 00355	YKC22-0489
1911	2422 025 10185	CON BM H 9P M 2.00 PH B
1916	2422 025 10772	CON BM V 12P M 2.00 PH B
1917	3103 140 27931	CABLE TREE ASSY 7P
1918	2412 020 00724	CON BM V 2P M 2.50 EH B

2102	4822 126 14241	0603 50V 330P COL R
2105	4822 126 14241	0603 50V 330P COL R
2106	4822 126 14305	100nF 10% 16V 0603
2120	4822 124 80791	470µF 16V 20% 105C DXH=8X11.5
2121	4822 126 14305	100nF 10% 16V 0603
2122	5322 126 11583	10nF 10% 50V 0603
2123	5322 126 11583	10nF 10% 50V 0603
2124	5322 126 11583	10nF 10% 50V 0603
2140	4822 124 11946	22µF 20% 16V
2150	4822 124 80231	47µF 20% 16V
2151	4822 126 14305	100nF 10% 16V 0603
2152	4822 121 43526	47nF 5% 250V
2154	4822 124 40849	330µF 20% 16V
2155	4822 126 14305	100nF 10% 16V 0603
2156	2238 586 59812	0603 50V 100NP80M
2157	5322 126 11583	10nF 10% 50V 0603
2158	4822 126 14305	100nF 10% 16V 0603
2159	2238 586 59812	0603 50V 100NP80M
2160	4822 126 14305	100nF 10% 16V 0603
2161	4822 126 14305	100nF 10% 16V 0603
2165	5322 126 11583	10nF 10% 50V 0603
2167	4822 126 13881	470pF 5% 50V
2168	4822 122 31765	100pF 2% 63V
2170	5322 126 11583	10nF 10% 50V 0603
2171	4822 126 13879	220nF 20% 16V
2173	5322 126 11583	10nF 10% 50V 0603
2174	4822 126 14305	100nF 10% 16V 0603
2175	3198 017 41050	0603 10V 1µF COL R
2177	5322 126 11583	10nF 10% 50V 0603
2179	5322 126 11583	10nF 10% 50V 0603
2180	4822 126 14305	100nF 10% 16V 0603

3101	4822 051 30102	1k 5% 0.062W
3102	4822 051 30105	1M 5% 0.062W
3106	4822 051 30102	1k 5% 0.062W
3107	4822 051 30105	1M 5% 0.062W
3110	4822 116 83868	150Ω 5% 0.5W
3111	4822 051 30759	75Ω 5% 0.062W
3112	4822 051 30759	75Ω 5% 0.062W
3113	4822 051 30759	75Ω 5% 0.062W
3121	4822 051 30101	100Ω 5% 0.062W
3122	4822 051 30103	10k 5% 0.062W
3123	4822 051 30223	22k 5% 0.062W
3124	4822 051 30682	6k8 5% 0.062W
3125	4822 051 30392	3k9 5% 0.063W 0603
3126	4822 117 12917	1Ω 5% 0.062W CASE0603
3127	4822 117 12864	82k 5% 0.6W
3128	4822 051 30103	10k 5% 0.062W
3129	4822 051 30103	10k 5% 0.062W
3130	4822 051 30103	10k 5% 0.062W
3131	4822 050 11002	1k 1% 0.4W
3132	4822 050 11002	1k 1% 0.4W
3133	4822 051 30223	22k 5% 0.062W
3134	4822 051 30103	10k 5% 0.062W
3135	4822 117 12063	NTC DC 5W 10k 5%
3136	4822 051 30472	4k7 5% 0.062W
3137	4822 051 30472	4k7 5% 0.062W
3138	4822 051 30103	10k 5% 0.062W
3139	4822 051 30391	390Ω 5% 0.062W
3140	4822 051 30221	220Ω 5% 0.062W
3141	4822 051 30472	4k7 5% 0.062W
3142	4822 117 12925	47k 1% 0.063W 0603
3143	4822 051 30103	10k 5% 0.062W
3144	4822 051 30391	390Ω 5% 0.062W
3145	4822 051 30103	10k 5% 0.062W
3146	4822 051 30103	10k 5% 0.062W
3147	4822 051 30103	10k 5% 0.062W
3148	4822 051 30222	2k2 5% 0.062W
3149	4822 051 30472	4k7 5% 0.062W
3150	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3151	4822 051 30102	1k 5% 0.062W
3152	4822 116 52257	22k 5% 0.5W
3153	2322 704 65608	RST SM 603 RC22H 5Ω6 PM1
3154	4822 050 21003	10k 1% 0.6W
3155	4822 051 30222	2k2 5% 0.062W
3156	4822 050 21003	10k 1% 0.6W
3157	4822 116 83884	47k 5% 0.5W
3158	4822 051 30223	22k 5% 0.062W
3159	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3160	2322 704 65608	RST SM 603 RC22H 5Ω6 PM1
3161	4822 116 52297	68k 5% 0.5W
3162	4822 051 30683	68k 5% 0.062W
3163	4822 051 30103	10k 5% 0.062W
3164	4822 050 21003	10k 1% 0.6W
3165	4822 051 30222	2k2 5% 0.062W
3166	4822 116 83876	270Ω 5% 0.5W
3167	4822 116 83876	270Ω 5% 0.5W
3168	4822 116 52175	100Ω 5% 0.5W
3169	4822 051 30103	10k 5% 0.062W
3171	4822 051 30222	2k2 5% 0.062W
3172	4822 051 30472	4k7 5% 0.062W
3173	4822 051 30103	10k 5% 0.062W
3174	4822 051 30475	4M7 5% 0.062W
3175	4822 051 30103	10k 5% 0.062W
3176	4822 051 30471	470Ω 5% 0.062W
3177	4822 051 30102	1k 5% 0.062W
3178	4822 051 30222	2k2 5% 0.062W
3179	4822 116 52283	4k7 5% 0.5W
3180	4822 051 30103	10k 5% 0.062W
3182	4822 051 30152	1k5 5% 0.062W
3183	4822 051 30222	2k2 5% 0.062W
3184	4822 051 30221	220Ω 5% 0.062W
3185	4822 051 30471	470Ω 5% 0.062W
3186	4822 051 30102	1k 5% 0.062W
3187	4822 051 30222	2k2 5% 0.062W
3188	4822 051 30472	4k7 5% 0.062W
3189	4822 051 30103	10k 5% 0.062W
3190	4822 117 12925	47k 1% 0.063W 0603
3191	4822 051 30221	220Ω 5% 0.062W
3192	4822 051 30102	1k 5% 0.062W
3193	4822 051 30103	10k 5% 0.062W
3194	4822 051 30222	2k2 5% 0.062W
3195	4822 051 30102	1k 5% 0.062W
3196	4822 051 30222	2k2 5% 0.062W
3197	4822 051 30221	220Ω 5% 0.062W
3198	4822 051 30472	4k7 5% 0.062W
3199	4822 051 30471	470Ω 5% 0.062W
4xxx	4822 051 10008	0Ω 5% 0.25W (1206)
4xxx	4822 051 20008	0Ω 5% 0.25W (0805)

5150	4822 157 51462	10µH 10% 4X9.8MM LAL04T100K
5151	4822 157 51462	10µH 10% 4X9.8MM LAL04T100K
5153	2422 531 02423	TRANSFORMER HEATER

6100	9322 146 61685	DIO RG SM DF3A6.8FU TOSJ
6101	9322 146 61685	DIO RG SM DF3A6.8FU TOSJ
6102	9322 146 61685	DIO RG SM DF3A6.8FU TOSJ

6103	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6104	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6140	9322 140 17676	LED VS LTL-14CHJ(LITO)A
6150	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6151	4822 130 83757	BAS216
6152	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6154	9322 102 64685	DIO REG SM UDZ2.7B (RHM0) R
6155	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6156	4822 130 83757	BAS216
6157	4822 130 30621	1N4148
6158	4822 130 30621	1N4148
6159	4822 130 30621	1N4148
6160	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6161	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6164	4822 130 30621	1N4148
6165	4822 130 30621	1N4148
6166	4822 130 30621	1N4148
6167	4822 130 30621	1N4148
6168	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6169	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6170	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6171	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6172	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6173	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6174	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6175	4822 130 30621	1N4148
6176	4822 130 30621	1N4148
6177	4822 130 30621	1N4148
6178	4822 130 30621	1N4148
6179	4822 130 30621	1N4148
6180	4822 130 30621	1N4148
6181	4822 130 30621	1N4148
6182	4822 130 30621	1N4148
6183	4822 130 30621	1N4148
6184	4822 130 30621	1N4148
6185	4822 130 30621	1N4148
6186	4822 130 30621	1N4148
6187	4822 130 30621	1N4148
6188	4822 130 30621	1N4148
6189	4822 130 30621	1N4148
6190	4822 130 30621	1N4148
6191	4822 130 30621	1N4148
6192	4822 130 30621	1N4148
6193	4822 130 30621	1N4148
6194	4822 130 30621	1N4148
6195	4822 130 30621	1N4148
6196	4822 130 30621	1N4148
6197	4822 130 30621	1N4148
6198	4822 130 83757	BAS216

7120	4822 209 30146	L2722
7140	9322 155 22667	
7141	4822 130 61553	DTC124EU
7142	3198 010 42310	BC847BW
7143	5322 130 42756	BC857C
7144	5322 130 42756	BC857C
7145	3198 010 42310	BC847BW
7150	2722 171 07721	VFD BJ-801GNK 120X32
7151	3198 010 42310	BC847BW
7152	9322 148 79668	FET POW SM STN3NE06(ST00)
7153	3198 010 42310	BC847BW
7155	3198 010 42310	BC847BW
7156	3103 178 56451	OTPROM ASSY DDCP1-1U
7157	3198 010 42310	BC847BW
7160	5322 209 11147	HEF4093BT
7164	3198 010 42310	BC847BW
7165	4822 130 61553	DTC124EU
7166	3198 010 42310	BC847BW

DIVIO FRONT

Various

1000	2422 033 00363	CON BM H 4P F 0.8 B
1001	2422 025 17106	CON BM H 4P F 0.8 IEEE R

2000	5322 126 10511	1nF 5% 50V
2001	5322 126 10511	1nF 5% 50V
2002	2020 557 90732	250V 4N7 PM10 R
2003	2020 557 90732	250V 4N7 PM10 R
2004	2020 557 90732	250V 4N7 PM10 R
2005	2020 557 90732	250V 4N7 PM10 R

3000	4822 051 20105	1M 5% 0.1W

5000	2422 549 44768	IND FXD SM EMI 100mH z 90R R
5001	2422 549 44768	IND FXD SM EMI 100mH z 90R R

6000	4822 130 11395	TLMH3100
6001	9322 172 97668	DIO SUP SM6T39CA (ST00) R

ANALOG PWB

Various

1324▲	2422 086 10954	PROT DEV 65V 1A PSC
1325▲	2422 086 10951	PROT DEV 65V 500MA PSC
1326▲	2422 086 10954	PROT DEV 65V 1A PSC
1327▲	2422 086 10951	PROT DEV 65V 500MA PSC
1600	4822 242 10434	L1101-95263-0E1(18,432MHz)
1700	4822 242 81436	OFWK3953M
1701	4822 242 10307	OFWG3956M
1702	2422 549 44341	FIL SAW 38MHz 9 OFWK9656M
1703	4822 242 72586	TPS5,5MB-TF20
1705	3139 147 17001	TUNER UV1316MK3(NON EURO)
1802	2422 543 01153	RES XTL 32KHZ768 12P5 DT-38 B
1900	4822 265 11154	52030-2210 (22P)
1932	2422 025 11244	CON BM V 07P M 2.50 EH B
1943	9322 155 28667	OPT FIB CON GP1FA550TZ (SRPJ)L
1945	2422 026 05197	CON BM CINCH H 1P F BK B
1950	2422 033 00334	CON BM EURO H 42P F BK GRND-L
1953	2422 025 10769	CON BMT 9P VERT PH-B
1954	4822 265 11154	52030-2210 (22P)
1955	2422 026 05046	CON BM MDIN 8P F TCX0310B
1958	2422 026 05093	CON BM CINCH 4P F 2*WHRD
1959	2422 026 05096	CON BM CINCH H 2P F YEYE
1960	4822 267 10565	4P
1982	4822 267 11031	10P. FEM. V
1983▲	2422 086 10919	PROT DEV 65V 125MA MP13
1984	2412 020 00724	CON BM V 2P M 2.50 EH B
1987	2422 025 10772	CON BM V 12P M 2.00 PH B
1990	4822 242 73552	13,875 000 MHz
1994	4822 242 10956	20MHz 20P AT-49

2000	4822 126 14494	22nF 10% 25V 0603
2002	4822 126 14241	0603 50V 330P COL R
2003	4822 126 14494	22nF 10% 25V 0603
2004	4822 124 40433	47µF 20% 25V
2005	4822 126 14305	100nF 10% 16V 0603
2006	4822 124 40433	47µF 20% 25V
2007	4822 126 13883	220pF 5% 50V
2008	4822 126 14241	0603 50V 330P COL R
2009	4822 126 14305	100nF 10% 16V 0603
2010	4822 126 14305	100nF 10% 16V 0603
2011	4822 124 40433	47µF 20% 25V
2012	4822 126 14305	100nF 10% 16V 0603
2013	4822 124 40433	47µF 20% 25V
2014	4822 126 14305	100nF 10% 16V 0603
2015	4822 124 40433	47µF 20% 25V
2016	4822 126 14305	100nF 10% 16V 0603
2017	4822 124 40433	47µF 20% 25V
2018	4822 126 13883	220pF 5% 50V
2019	4822 126 14305	100nF 10% 16V 0603
2024	4822 122 33777	47pF 5% 63V
2030	4822 124 41584	100µF 20% 10V
2321	4822 126 14305	100nF 10% 16V 0603
2322	4822 126 14305	100nF 10% 16V 0603
2323	3198 017 34730	0603 16V 47nF COL
2324	2020 552 96327	16V 330nF PM10
2325	4822 126 14305	100nF 10% 16V 0603
2328	4822 124 41584	100µF 20% 10V
2329	3198 017 44740	0603 10V 470nF COL
2332	4822 124 40207	100µF 20% 25V
2400	5322 126 11583	10nF 10% 50V 0603
2401	4822 126 14305	100nF 10% 16V 0603
2402	4822 126 14305	100nF 10% 16V 0603
2403	4822 124 40433	47µF 20% 25V
2404	5322 126 11583	10nF 10% 50V 0603
2405	5322 126 11583	10nF 10% 50V 0603
2406	5322 126 11578	1nF 10% 50V 0603
2407	4822 126 14305	100nF 10% 16V 0603
2408	5322 126 11578	1nF 10% 50V 0603
2430	5322 126 11583	10nF 10% 50V 0603
2431	4822 124 40433	47µF 20% 25V
2432	5322 126 11583	10nF 10% 50V 0603
2433	4822 124 81151	22µF 50V
2434	4822 124 40207	100µF 20% 25V
2436	4822 124 81151	22µF 50V
2437	4822 126 14305	100nF 10% 16V 0603
2438	4822 126 14305	100nF 10% 16V 0603
2439	4822 124 81151	22µF 50V
2440	4822 124 40207	100µF 20% 25V
2441	4822 124 81151	22µF 50V
2442	4822 124 11947	10µF 20% 16V
2443	4822 124 11947	10µF 20% 16V
2446	4822 126 13881	470pF 5% 50V
2447	4822 126 13881	470pF 5% 50V
2460	4822 124 40433	47µF 20% 25V
2461	4822 124 40769	4.7µF 20% 100V
2462	4822 124 40433	47µF 20% 25V
2463	4822 124 40769	4.7µF 20% 100V
2464	4822 126 14305	100nF 10% 16V 0603
2465	4822 126 14305	100nF 10% 16V 0603
2466	5322 126 11583	10nF 10% 50V 0603
2467	4822 126 13881	470pF 5% 50V
2468	4822 126 13881	470pF 5% 50V
2469	3198 017 41050	0603 10V 1µF COL R
2470	4822 126 14305	100nF 10% 16V 0603
2473	4822 122 33753	150pF 5% 50V
2474	4822 126 14305	100nF 10% 16V 0603
2477	4822 126 14305	100nF 10% 16V 0603
2481	2222 867 15339	0603 50V 33P PM5
2483	3198 017 41050	0603 10V 1µF COL R
2484	5322 126 11578	1nF 10% 50V 0603
2500	4822 126 14305	100nF 10% 16V 0603
2501	4822 126 14305	100nF 10% 16V 0603
2502	4822 124 40769	4.7µF 20% 100V
2503	4822 124 40769	4.7µF 20% 100V
2505	4822 126 14305	100nF 10% 16V 0603
2506	4822 126 14305	100nF 10% 16V 0603
2507	4822 126 14305	100nF 10% 16V 0603
2508	4822 124 40433	47µF 20% 25V
2509	4822 124 40769	4.7µF 20% 100V
2510	4822 124 40433	47µF 20% 25V
2511	4822 122 33777	47pF 5% 63V
2512	4822 122 33777	47pF 5% 63V
2513	4822 126 14305	100nF 10% 16V 0603
2514	4822 126 14305	100nF 10% 16V 0603
2515	4822 124 40769	4.7µF 20% 100V
2516	3198 017 41050	0603 10V 1µF COL R
2517	3198 017 41050	0603 10V 1µF COL R
2518	3198 017 41050	0603 10V 1µF COL R
2519	3198 017 41050	0603 10V 1µF COL R
2520	4822 124 41584	100µF 20% 10V
2521	4822 126 14305	100nF 10% 16V 0603
2522	3198 017 41050	0603 10V 1µF COL R
2523	4822 126 14305	100nF 10% 16V 0603
2524	3198 017 41050	0603 10V 1µF COL R
2525	3198 017 41050	0603 10V 1µF COL R
2526	4822 126 14305	100nF 10% 16V 0603
2527	4822 126 14305	100nF 10% 16V 0603
2528	3198 017 41050	0603 10V 1µF COL R

2529	4822 126 14305	100nF 10% 16V 0603
2530	3198 017 41050	0603 10V 1µF COL R
2531	4822 126 14305	100nF 10% 16V 0603
2532	4822 124 11947	10µF 20% 16V
2533	4822 124 11947	10µF 20% 16V
2534	4822 126 14305	100nF 10% 16V 0603
2535	4822 124 11947	10µF 20% 16V
2536	3198 017 41050	0603 10V 1µF COL R
2537	3198 017 41050	0603 10V 1µF COL R
2538	3198 017 41050	0603 10V 1µF COL R
2539	4822 124 11947	10µF 20% 16V
2540	5322 126 11578	1nF 10% 50V 0603
2541	4822 126 14305	100nF 10% 16V 0603
2542	4822 126 13879	220nF 20% 16V
2544	4822 126 14305	100nF 10% 16V 0603
2545	4822 126 13881	470pF 5% 50V
2546	4822 126 13881	470pF 5% 50V
2549	3198 017 41050	0603 10V 1µF COL R
2550	3198 017 41050	0603 10V 1µF COL R
2551	5322 126 11583	10nF 10% 50V 0603
2600	4822 124 40248	10µF 20% 63V
2601	5322 126 11583	10nF 10% 50V 0603
2602	4822 124 40248	10µF 20% 63V
2603	4822 126 14305	100nF 10% 16V 0603
2604	5322 126 11583	10nF 10% 50V 0603
2605	4822 124 40248	10µF 20% 63V
2606	5322 126 11583	10nF 10% 50V 0603
2607	4822 126 14225	56pF 5% 50V 0603
2608	4822 124 40248	10µF 20% 63V
2609	4822 126 14225	56pF 5% 50V 0603
2610	5322 126 11583	10nF 10% 50V 0603
2612	4822 124 40769	4.7µF 20% 100V
2614	3198 017 41050	0603 10V 1µF COL R
2614	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2615	3198 017 41050	0603 10V 1µF COL R
2615	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2618	3198 017 41050	0603 10V 1µF COL R
2619	3198 017 41050	0603 10V 1µF COL R
2620	3198 016 33380	0603 50V 3P3 COL
2621	3198 016 33380	0603 50V 3P3 COL
2622	4822 124 40248	10µF 20% 63V
2623	5322 126 11583	10nF 10% 50V 0603
2624	3198 017 41050	0603 10V 1µF COL R
2624	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2625	3198 017 41050	0603 10V 1µF COL R
2625	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2626	3198 017 41050	0603 10V 1µF COL R
2627	3198 017 41050	0603 10V 1µF COL R
2700	4822 124 81151	22µF 50V
2701	5322 122 33861	120pF 10% 50V
2702	4822 126 13883	220pF 5% 50V
2703	5322 124 41379	2.2µF 20% 50V
2704	4822 126 13881	470pF 5% 50V
2705	4822 126 14305	100nF 10% 16V 0603
2706	4822 126 14305	100nF 10% 16V 0603
2707	5322 126 11583	10nF 10% 50V 0603
2708	4822 124 40248	10µF 20% 63V
2709	4822 126 13879	220nF 20% 16V
2710	2020 552 94523	0603 50V 8P2 PM0P5
2711	5322 126 11578	1nF 10% 50V 0603
2712	5322 126 11578	1nF 10% 50V 0603
2713	3198 024 44730	47nF 50V 0603
2714	4822 124 22652	2.2µF 20% 50V
2715	5322 126 11578	1nF 10% 50V 0603
2716	4822 124 41584	100µF 20% 10V
2717	4822 124 22652	2.2µF 20% 50V
2718	4822 124 40433	47µF 20% 25V
2800	3198 017 44740	0603 10V 470nF COL
2801	4822 126 14238	0603 50V 2N2 COL R
2802	4822 126 13482	470nF 80/20% 16V
2803	4822 126 13883	220pF 5% 50V
2806	3198 017 44740	0603 10V 470nF COL
2807	4822 126 13482	470nF 80/20% 16V
2810	5322 126 11578	1nF 10% 50V 0603
2811	4822 124 11968	220mF 20% 5.5V
2812	4822 126 14305	100nF 10% 16V 0603
2814	5322 126 11583	10nF 10% 50V 0603
2815	4822 126 14507	18pF 5% 50V 0603
2816	3198 017 41050	0603 10V 1µF COL R
2817	5322 126 11578	1nF 10% 50V 0603
2818	5322 126 11583	10nF 10% 50V 0603
2819	3198 017 44740	0603 10V 470nF COL
2820	3198 017 44740	0603 10V 470nF COL
2821	2020 552 96305	4U7 20% 10V
2822	2020 552 96305	4U7 20% 10V
2823	4822 126 14305	100nF 10% 16V 0603
2831	4822 124 40433	47µF 20% 25V
2832	4822 126 14305	100nF 10% 16V 0603
2900	5322 126 11583	10nF 10% 50V 0603
2901	4822 124 40433	47µF 20% 25V
2902	4822 126 14305	100nF 10% 16V 0603
2903	4822 126 13879	220nF 20% 16V
2904	3198 017 41050	0603 10V 1µF COL R
2905	4822 124 40433	47µF 20% 25V
2906	4822 126 14305	100nF 10% 16V 0603
2907	5322 126 11583	10nF 10% 50V 0603
2908	4822 126 11669	27pF
2909	4822 126 14305	100nF 10% 16V 0603
2910	4822 126 11669	27pF
2911	2222 867 15339	0603 50V 33P PM5
2914	4822 126 14305	100nF 10% 16V 0603
2915	4822 126 14305	100nF 10% 16V 0603
2916	4822 126 14305	100nF 10% 16V 0603
2917	4822 126 14305	100nF 10% 16V 0603
2918	4822 126 14305	100nF 10% 16V 0603
2950	4822 126 14305	100nF 10% 16V 0603
2951	4822 124 40248	10µF 20% 63V
2952	4822 126 14238	0603 50V 2N2 COL R
2953	4822 126 14238	0603 50V 2N2 COL R
2954	4822 126 14508	180pF 5% 50V 0603
2955	4822 126 14508	180pF 5% 50V 0603
2956	3198 017 41050	0603 10V 1µF COL R
2957	3198 017 41050	0603 10V 1µF COL R
2970	4822 124 11947	10µF 20% 16V
2980	4822 124 40207	100µF 20% 25V
2981	4822 126 14305	100nF 10% 16V 0603
2982	4822 124 40207	100µF 20% 25V
2983	5322 126 11583	10nF 10% 50V 0603
2984	3198 016 31020	0603 25V 1nF
2990	4822 126 14305	100nF 10% 16V 0603
2991	4822 124 40433	47µF 20% 25V
2992	4822 126 14305	100nF 10% 16V 0603
2993	4822 126 14305	100nF 10% 16V 0603
2994	4822 126 14305	100nF 10% 16V 0603
2995	4822 122 33761	22pF 5% 50V
2996	4822 122 33761	22pF 5% 50V

3000	4822 051 30472	4k7 5% 0.062W
3001	4822 117 13632	100k 1% 0603 0.62W
3002	4822 051 30103	10k 5% 0.062W
3003	4822 051 30103	10k 5% 0.062W
3004	4822 051 30103	10k 5% 0.062W
3005	4822 051 30472	4k7 5% 0.062W
3005	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3006	4822 051 30472	4k7 5% 0.062W
3006	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3007	4822 051 30472	4k7 5% 0.062W
3007	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3008	2120 108 94006	RST SM 0603 ERJ3G 1Ω5 PM5
3009	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3009	4822 051 30332	3k3 5% 0.062W
3010	2120 108 94006	RST SM 0603 ERJ3G 1Ω5 PM5
3011	4822 051 30472	4k7 5% 0.062W
3011	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3012	4822 051 30472	4k7 5% 0.062W
3012	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3013	4822 117 12139	22Ω 5% 0.062W
3014	4822 117 12139	22Ω 5% 0.062W
3015	4822 117 12139	22Ω 5% 0.062W
3016	4822 117 12139	22Ω 5% 0.062W
3017	4822 051 30472	4k7 5% 0.062W
3017	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3018	2120 108 94006	RST SM 0603 ERJ3G 1Ω5 PM5
3019	2120 108 94006	RST SM 0603 ERJ3G 1Ω5 PM5
3020	4822 051 30123	12k 5% 0.062W
3020	5322 117 13028	12k 1% 0.063W 0603 RC22H
3021	4822 051 30123	12k 5% 0.062W
3021	5322 117 13028	12k 1% 0.063W 0603 RC22H
3022	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3022	4822 051 30332	3k3 5% 0.062W
3023	4822 117 12925	47k 1% 0.063W 0603
3024	4822 117 12925	47k 1% 0.063W 0603
3025	4822 117 12139	22Ω 5% 0.062W
3026	4822 117 12139	22Ω 5% 0.062W
3027	4822 117 12139	22Ω 5% 0.062W
3028	4822 117 13608	4.7Ω 5% 0603 0.0016W
3029	4822 051 30008	0Ω jumper
3029	4822 117 12903	1k8 1% 0.063W 0603
3030	4822 117 12139	22Ω 5% 0.062W
3032	4822 051 30008	0Ω jumper
3032	4822 117 12903	1k8 1% 0.063W 0603
3321	4822 117 12891	220k 1% ERJ3Ω
3325	4822 117 12891	220k 1% ERJ3Ω
3326	4822 051 30103	10k 5% 0.062W
3335	4822 051 30472	4k7 5% 0.062W
3336	4822 051 30103	10k 5% 0.062W
3337	4822 117 13632	100k 1% 0603 0.62W
3338	4822 117 12891	220k 1% ERJ3Ω
3339	4822 117 12891	220k 1% ERJ3Ω
3340	4822 117 12891	220k 1% ERJ3Ω
3402	4822 117 13632	100k 1% 0603 0.62W
3403	4822 051 30101	100Ω 5% 0.062W
3404	4822 051 30101	100Ω 5% 0.062W
3405	4822 051 30759	75Ω 5% 0.062W
3406	4822 051 30759	75Ω 5% 0.062W
3407	4822 051 30101	100Ω 5% 0.062W
3408	4822 051 30759	75Ω 5% 0.062W
3409	4822 051 30103	10k 5% 0.062W
3410	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3411	4822 117 13632	100k 1% 0603 0.62W
3412	4822 051 30103	10k 5% 0.062W
3413	4822 051 30103	10k 5% 0.062W
3414	4822 051 30103	10k 5% 0.062W
3415	4822 117 13632	100k 1% 0603 0.62W
3416	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3417	4822 117 13632	100k 1% 0603 0.62W
3418	4822 117 13632	100k 1% 0603 0.62W
3419	4822 117 13632	100k 1% 0603 0.62W
3423	4822 117 12864	82k 5% 0.6W
3424	4822 051 30474	470k 5% 0.062W
3425	4822 051 30474	470k 5% 0.062W
3426	4822 051 30474	470k 5% 0.062W
3428	4822 051 30101	100Ω 5% 0.062W
3429	4822 051 30561	560Ω 5% 0.062W
3431	4822 051 30472	4k7 5% 0.062W
3432	4822 051 30759	75Ω 5% 0.062W
3433	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3434	4822 117 12864	82k 5% 0.6W
3435	4822 117 13632	100k 1% 0603 0.62W
3436	4822 051 30759	75Ω 5% 0.062W
3437	4822 117 12864	82k 5% 0.6W
3438	4822 117 13632	100k 1% 0603 0.62W
3439	4822 051 30471	470Ω 5% 0.062W
3440	4822 051 30101	100Ω 5% 0.062W
3441	4822 117 13632	100k 1% 0603 0.62W
3442	4822 051 30472	4k7 5% 0.062W
3443	4822 051 30479	47Ω 5% 0.062W
3445	4822 051 30471	470Ω 5% 0.062W
3446	4822 051 30101	100Ω 5% 0.062W
3450	4822 117 13632	100k 1% 0603 0.62W
3451	4822 051 30472	4k7 5% 0.062W
3455	4822 117 13632	100k 1% 0603 0.62W
3458	4822 051 30152	1k5 5% 0.062W
3459	4822 051 30472	4k7 5% 0.062W
3460	4822 051 30471	470Ω 5% 0.062W
3461	4822 051 30472	4k7 5% 0.062W
3462	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3463	4822 117 13632	100k 1% 0603 0.62W
3464	4822 117 13632	100k 1% 0603 0.62W
3465	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3466	4822 051 30471	470Ω 5% 0.062W
3467	4822 051 30472	4k7 5% 0.062W
3468	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3469	4822 117 13632	100k 1% 0603 0.62W
3470	4822 117 13632	100k 1% 0603 0.62W
3471	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3472	4822 051 30471	470Ω 5% 0.062W
3473	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3474	4822 051 30471	470Ω 5% 0.062W
3475	4822 051 30102	1k 5% 0.062W
3476	5322 117 13068	82Ω 1% 0.063W 0603 RC22H
3477	4822 117 12925	47k 1% 0.063W 0603
3478	4822 051 30759	75Ω 5% 0.062W
3479	4822 051 30472	4k7 5% 0.062W
3480	4822 051 30759	75Ω 5% 0.062W
3481	4822 051 30759	75Ω 5% 0.062W
3482	4822 051 30101	100Ω 5% 0.062W
3483	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3484	4822 051 30759	75Ω 5% 0.062W
3485	4822 051 30102	1k 5% 0.062W
3486	4822 051 30151	150Ω 5% 0.062W

3487	4822 051 30101	100Ω 5% 0.062W
3488	4822 051 30101	100Ω 5% 0.062W
3489	4822 051 30103	10k 5% 0.062W
3490	4822 051 30471	470Ω 5% 0.062W
3492	4822 117 13632	100k 1% 0603 0.62W
3494	4822 051 30759	75Ω 5% 0.062W
3495	4822 051 30222	2k2 5% 0.062W
3497	4822 051 30101	100Ω 5% 0.062W
3499	4822 051 30331	330Ω 5% 0.062W
3500	4822 051 30272	2k7 5% 0.062W
3501	4822 051 30272	2k7 5% 0.062W
3503	4822 051 30221	220Ω 5% 0.062W
3504	4822 051 30222	2k2 5% 0.062W
3505	4822 051 30222	2k2 5% 0.062W
3506	4822 051 30221	220Ω 5% 0.062W
3515	4822 117 13632	100k 1% 0603 0.62W
3516	4822 051 30471	470Ω 5% 0.062W
3517	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3518	4822 051 30472	4k7 5% 0.062W
3519	4822 117 13632	100k 1% 0603 0.62W
3520	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3521	4822 051 30102	1k 5% 0.062W
3522	4822 051 30471	470Ω 5% 0.062W
3523	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3524	4822 051 30101	100Ω 5% 0.062W
3525	4822 051 30101	100Ω 5% 0.062W
3526	4822 117 13632	100k 1% 0603 0.62W
3527	4822 051 30472	4k7 5% 0.062W
3528	4822 051 30471	470Ω 5% 0.062W
3529	4822 117 13632	100k 1% 0603 0.62W
3530	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3531	4822 051 30471	470Ω 5% 0.062W
3532	4822 051 30471	470Ω 5% 0.062W
3533	4822 117 12925	47k 1% 0.063W 0603
3534	4822 051 30101	100Ω 5% 0.062W
3535	4822 051 30471	470Ω 5% 0.062W
3536	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3537	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3538	4822 051 30102	1k 5% 0.062W
3539	4822 051 30102	1k 5% 0.062W
3540	5322 117 13068	82Ω 1% 0.063W 0603 RC22H
3541	4822 051 30471	470Ω 5% 0.062W
3542	4822 051 30471	470Ω 5% 0.062W
3543	4822 051 30101	100Ω 5% 0.062W
3544	4822 051 30472	4k7 5% 0.062W
3545	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3546	4822 051 30102	1k 5% 0.062W
3547	4822 051 30151	150Ω 5% 0.062W
3548	4822 051 30101	100Ω 5% 0.062W
3549	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3550	4822 051 30102	1k 5% 0.062W
3551	4822 051 30101	100Ω 5% 0.062W
3552	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3553	4822 051 30102	1k 5% 0.062W
3554	4822 051 30759	75Ω 5% 0.062W
3555	4822 051 30103	10k 5% 0.062W
3556	4822 117 12925	47k 1% 0.063W 0603
3557	4822 117 12925	47k 1% 0.063W 0603
3558	4822 051 30223	22k 5% 0.062W
3559	4822 051 30392	3k9 5% 0.063W 0603
3560	4822 117 12891	220k 1% ERJ3Ω
3561	4822 051 30332	3k3 5% 0.062W
3562	4822 051 30101	100Ω 5% 0.062W
3563	4822 051 30101	100Ω 5% 0.062W
3567	4822 051 30103	10k 5% 0.062W
3568	4822 051 30472	4k7 5% 0.062W
3570	4822 117 13632	100k 1% 0603 0.62W
3600	4822 051 30103	10k 5% 0.062W
3601	4822 051 30101	100Ω 5% 0.062W
3602	4822 051 30472	4k7 5% 0.062W
3603	4822 051 30101	100Ω 5% 0.062W
3604	4822 051 30102	1k 5% 0.062W
3605	4822 051 30102	1k 5% 0.062W
3606	4822 051 30102	1k 5% 0.062W
3607	4822 051 30102	1k 5% 0.062W
3700	4822 051 30333	33k 5% 0.062W
3701	4822 051 30681	680Ω 5% 0.062W
3702	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3703	4822 051 30154	150k 5% 0.062W
3704	4822 051 30472	4k7 5% 0.062W
3705	4822 051 30183	18k 5% 0.062W
3706	4822 051 30331	330Ω 5% 0.062W
3707	4822 100 12158	22k 30%
3708	4822 051 30101	100Ω 5% 0.062W
3709	4822 051 30183	18k 5% 0.062W
3710	4822 051 30101	100Ω 5% 0.062W
3711	4822 051 30008	0Ω jumper
3712	4822 051 30222	2k2 5% 0.062W
3713	4822 051 30682	6k8 5% 0.062W
3714	4822 051 30472	4k7 5% 0.062W
3715	4822 051 30101	100Ω 5% 0.062W
3716	4822 051 30101	100Ω 5% 0.062W
3717	4822 051 30102	1k 5% 0.062W
3718	4822 051 30472	4k7 5% 0.062W
3719	4822 051 30472	4k7 5% 0.062W
3720	4822 051 30101	100Ω 5% 0.062W
3721	4822 051 30271	270Ω 5% 0.062W
3722	4822 051 30332	3k3 5% 0.062W
3723	4822 117 13632	100k 1% 0603 0.62W
3724	4822 051 30681	680Ω 5% 0.062W
3725	4822 051 30472	4k7 5% 0.062W
3726	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3727	4822 051 30272	2k7 5% 0.062W
3728	4822 051 30331	330Ω 5% 0.062W
3729	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3730	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3800	4822 051 30103	10k 5% 0.062W
3801	4822 051 30273	27k 5% 0.062W
3803	4822 051 30682	6k8 5% 0.062W
3804	4822 051 30222	2k2 5% 0.062W
3805	4822 051 30222	2k2 5% 0.062W
3807	5322 117 13052	2k7 1% 0.063W 0603 RC22H
3808	4822 051 30333	33k 5% 0.062W
3809	4822 051 30103	10k 5% 0.062W
3810	4822 117 13632	100k 1% 0603 0.62W
3811	4822 051 30472	4k7 5% 0.062W
3812	4822 051 30221	220Ω 5% 0.062W
3813	4822 051 30684	680k 5% 0.062W
3815	5322 117 13018	1k0 1% 0.063W 0603 RC22H
3816	4822 051 30101	100Ω 5% 0.062W
3817	4822 051 30102	1k 5% 0.062W
3818	4822 051 30101	100Ω 5% 0.062W
3819	4822 051 30101	100Ω 5% 0.062W
3820	4822 051 30472	4k7 5% 0.062W
3821	4822 051 30103	10k 5% 0.062W
3822	4822 117 13632	100k 1% 0603 0.62W
3823	4822 051 30103	10k 5% 0.062W
3824	4822 051 30103	10k 5% 0.062W
3825	4822 051 30103	10k 5% 0.062W
3829	5322 117 13052	2k7 1% 0.063W 0603 RC22H
3830	4822 051 30472	4k7 5% 0.062W
3831	4822 051 30103	10k 5% 0.062W
3832	4822 117 13632	100k 1% 0603 0.62W
3833	4822 051 30222	2k2 5% 0.062W
3834	4822 051 30222	2k2 5% 0.062W
3835	4822 051 30103	10k 5% 0.062W
3837	4822 117 13632	100k 1% 0603 0.62W
3838	4822 051 30472	4k7 5% 0.062W
3839	4822 051 30103	10k 5% 0.062W
3840	4822 051 30101	100Ω 5% 0.062W
3841	4822 051 30101	100Ω 5% 0.062W
3842	4822 051 30684	680k 5% 0.062W
3843	4822 051 30103	10k 5% 0.062W
3844	4822 051 30102	1k 5% 0.062W
3845	4822 051 30472	4k7 5% 0.062W
3846	4822 051 30102	1k 5% 0.062W
3847	4822 051 30332	3k3 5% 0.062W
3848	4822 117 12925	47k 1% 0.063W 0603
3849	4822 051 30103	10k 5% 0.062W
3850	4822 051 30472	4k7 5% 0.062W
3851	4822 051 30103	10k 5% 0.062W
3852	4822 117 13632	100k 1% 0603 0.62W
3853	4822 117 13632	100k 1% 0603 0.62W
3854	5322 117 13018	1k0 1% 0.063W 0603 RC22H
3855	4822 051 30472	4k7 5% 0.062W
3856	4822 117 13632	100k 1% 0603 0.62W
3857	4822 051 30222	2k2 5% 0.062W
3858	4822 117 13632	100k 1% 0603 0.62W
3859	4822 117 13632	100k 1% 0603 0.62W
3860	4822 051 30682	6k8 5% 0.062W
3861	4822 051 30103	10k 5% 0.062W
3862	4822 051 30223	22k 5% 0.062W
3863	4822 051 30101	100Ω 5% 0.062W
3864	4822 051 30101	100Ω 5% 0.062W
3865	4822 051 30101	100Ω 5% 0.062W
3866	4822 117 12925	47k 1% 0.063W 0603
3867	4822 051 30101	100Ω 5% 0.062W
3868	4822 051 30103	10k 5% 0.062W
3869	4822 051 30332	3k3 5% 0.062W
3870	4822 051 30101	100Ω 5% 0.062W
3872	4822 051 30103	10k 5% 0.062W
3873	4822 051 30103	10k 5% 0.062W
3874	4822 051 30123	12k 5% 0.062W
3875	4822 051 30102	1k 5% 0.062W
3876	4822 051 30331	330Ω 5% 0.062W
3877	4822 051 30101	100Ω 5% 0.062W
3878	4822 051 30101	100Ω 5% 0.062W
3879	4822 051 30103	10k 5% 0.062W
3880	4822 051 30103	10k 5% 0.062W
3881	4822 051 30103	10k 5% 0.062W
3882	4822 117 13632	100k 1% 0603 0.62W
3883	4822 051 30331	330Ω 5% 0.062W
3885	4822 051 30222	2k2 5% 0.062W
3886	4822 051 30479	47Ω 5% 0.062W
3887	4822 051 30474	470k 5% 0.062W
3888	4822 051 30223	22k 5% 0.062W
3889	4822 051 30102	1k 5% 0.062W
3890	4822 051 30101	100Ω 5% 0.062W
3892	4822 051 30103	10k 5% 0.062W
3893	4822 051 30103	10k 5% 0.062W
3896	4822 051 30103	10k 5% 0.062W
3898	4822 051 30103	10k 5% 0.062W
3899	4822 051 30103	10k 5% 0.062W
3900	4822 051 30103	10k 5% 0.062W
3901	4822 117 12925	47k 1% 0.063W 0603
3902	4822 051 30472	4k7 5% 0.062W
3903	4822 051 30102	1k 5% 0.062W
3904	4822 051 30102	1k 5% 0.062W
3905	4822 051 30102	1k 5% 0.062W
3906	4822 051 30333	33k 5% 0.062W
3907	4822 051 30101	100Ω 5% 0.062W
3908	4822 051 30101	100Ω 5% 0.062W
3909	4822 051 30101	100Ω 5% 0.062W
3910	4822 051 30102	1k 5% 0.062W
3911	4822 051 30472	4k7 5% 0.062W
3912	4822 051 30103	10k 5% 0.062W
3913	4822 117 13632	100k 1% 0603 0.62W
3914	4822 051 30101	100Ω 5% 0.062W
3915	4822 051 30101	100Ω 5% 0.062W
3918	4822 051 30103	10k 5% 0.062W
3919	4822 051 30103	10k 5% 0.062W
3920	4822 117 12891	220k 1% ERJ3Ω
3925	4822 117 12139	22Ω 5% 0.062W
3943	4822 051 30103	10k 5% 0.062W
3944	4822 117 12891	220k 1% ERJ3Ω
3947	4822 051 30103	10k 5% 0.062W
3948	4822 051 30008	0Ω jumper
3950	4822 051 30472	4k7 5% 0.062W
3951	4822 117 13632	100k 1% 0603 0.62W
3952	4822 051 30223	22k 5% 0.062W
3953	4822 051 30153	15k 5% 0.062W
3954	4822 051 30472	4k7 5% 0.062W
3955	4822 051 30472	4k7 5% 0.062W
3956	4822 051 30222	2k2 5% 0.062W
3957	4822 051 30222	2k2 5% 0.062W
3958	4822 051 30472	4k7 5% 0.062W
3959	3198 021 31060	RST SM 0603 10M PM5COL R
3960	3198 021 31060	RST SM 0603 10M PM5COL R
3961	4822 051 30333	33k 5% 0.062W
3962	4822 051 30333	33k 5% 0.062W
3963	4822 051 30333	33k 5% 0.062W
3964	4822 051 30333	33k 5% 0.062W
3965	4822 051 30333	33k 5% 0.062W
3966	4822 051 30333	33k 5% 0.062W
3967	2322 704 65608	RST SM 603 RC22H 5Ω6 PM1
3967	4822 051 30109	10Ω 5% 0.062W
3968	2322 704 65608	RST SM 603 RC22H 5Ω6 PM1
3968	4822 051 30109	10Ω 5% 0.062W
3969	2322 704 65608	RST SM 603 RC22H 5Ω6 PM1
3969	4822 051 30109	10Ω 5% 0.062W
3970	4822 117 12891	220k 1% ERJ3Ω
3971	5322 117 13024	33k 1% 0.063W 0603 RC22H
3972	4822 051 30471	470Ω 5% 0.062W
3973	4822 051 30102	1k 5% 0.062W
3975	4822 051 30563	56k 5% 0.062W
3976	4822 051 30393	39k 5% 0.062W
3976	4822 117 12864	82k 5% 0.6W
3977	4822 051 30223	22k 5% 0.062W
3978	2322 704 65608	RST SM 603 RC22H 5Ω6 PM1
3978	4822 051 30109	10Ω 5% 0.062W
3979	4822 051 30102	1k 5% 0.062W
3980	4822 051 30333	33k 5% 0.062W
3981	4822 051 30153	15k 5% 0.062W
3982	4822 051 30183	18k 5% 0.062W
3983	4822 051 30563	56k 5% 0.062W
3984	4822 051 30102	1k 5% 0.062W

3985	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3986	4822 051 30103	10k 5% 0.062W
3987	4822 051 30102	1k 5% 0.062W
3988	4822 051 30273	27k 5% 0.062W
3989	4822 051 30103	10k 5% 0.062W
3990	4822 117 12925	47k 1% 0.063W 0603
3991	4822 117 12925	47k 1% 0.063W 0603
3992	4822 117 12925	47k 1% 0.063W 0603
3993	4822 051 30101	100Ω 5% 0.062W
3994	4822 051 30101	100Ω 5% 0.062W
3995	4822 051 30103	10k 5% 0.062W
3996	4822 051 30109	10Ω 5% 0.062W
3997	4822 051 30109	10Ω 5% 0.062W

5000	4822 157 11074	100μH
5001	4822 157 11074	100μH
5002	4822 157 11299	EL0305RA-100J
5003	4822 157 11499	BLM11P600SPT
5004	4822 157 11499	BLM11P600SPT
5009	4822 157 11775	6.8μH 5% 5X3
5400	4822 157 11299	EL0305RA-100J
5430	4822 157 11299	EL0305RA-100J
5470	2422 536 00019	TRANSFORMER 6RG (SAGA) B
5600	4822 157 11299	EL0305RA-100J
5601	2422 535 94279	IND FXD EL0305 S 100U PM5 A
5602	4822 157 11299	EL0305RA-100J
5700	4822 157 11074	100μH
5701	4822 157 11775	6.8μH 5% 5X3
5702	2422 549 44162	IND VAR 7MM Y 77M8 B
5703	2422 549 44162	IND VAR 7MM Y 77M8 B
5705	4822 157 11299	EL0305RA-100J
5706	4822 157 11775	6.8μH 5% 5X3
5707	4822 157 11302	EL0305RA-150J
5901	4822 157 11499	BLM11P600SPT
5902	4822 157 11074	100μH
5903	4822 157 11499	BLM11P600SPT
5904	4822 157 11499	BLM11P600SPT
5990	4822 157 11299	EL0305RA-100J
5991	4822 157 11074	100μH

6000	4822 130 83757	BAS216
6402	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6403	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6405	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6430	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6431	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6432	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6439	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6440	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6460	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6461	9322 129 42685	DIO REG SM BZM55-C15 (TEG0) R
6462	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6463	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6464	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6465	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6466	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6468	4822 130 83757	BAS216
6501	9322 129 42685	DIO REG SM BZM55-C15 (TEG0) R
6502	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6503	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6504	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6505	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6506	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6507	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6508	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6509	9322 150 38685	DIO SIG SM BAS385(VISH)R
6600	4822 130 83757	BAS216
6700	4822 130 11525	1SS356
6701	4822 130 11525	1SS356
6702	4822 130 11525	1SS356
6703	4822 130 83757	BAS216
6801	9322 150 38685	DIO SIG SM BAS385(VISH)R
6802	4822 130 83757	BAS216
6803	4822 130 83757	BAS216
6805	9322 150 38685	DIO SIG SM BAS385(VISH)R
6807	4822 130 83757	BAS216
6970	4822 130 83757	BAS216
6971	4822 130 83757	BAS216
6972	4822 130 83757	BAS216

7000	5322 130 42756	BC857C
7001	4822 209 17423	UAD1328T
7002	4822 209 62312	MC33078D
7004	9352 615 37118	IC SM UDA1360TS/N1 (PHSE) R
7321	9322 147 95668	FET SIG SM 2SK2839 (TOSJ)
7323	9322 147 95668	FET SIG SM 2SK2839 (TOSJ)
7324	4822 130 61553	DTC124EU
7329	3198 010 42310	BC847BW
7330	3198 010 42310	BC847BW
7331	3198 010 42310	BC847BW
7332	4822 209 33665	L78M08CV
7400	9322 143 92668	IC SM BA7652AF (RHM0) R
7401	9322 143 92668	IC SM BA7652AF (RHM0) R
7430	9965 000 04716	IC BA7660FS-E2
7431	4822 130 42804	BC817-25
7433	4822 130 42804	BC817-25
7460	4822 130 42804	BC817-25
7461	4822 130 42804	BC817-25
7462	3198 010 42310	BC847BW
7463	4822 130 42804	BC817-25
7464	3198 010 42310	BC847BW
7466	4822 130 42804	BC817-25
7470	5322 209 11517	PC74HCU04T
7500	5322 130 42756	BC857C
7501	5322 130 42756	BC857C
7505	4822 130 42804	BC817-25
7506	4822 130 42804	BC817-25
7507	9322 135 58671	IC SM STV6410AD (ST00) Y
7508	3198 010 42310	BC847BW
7509	3198 010 42310	BC847BW
7510	3198 010 42310	BC847BW
7511	4822 130 42804	BC817-25
7512	3198 010 42310	BC847BW
7513	3198 010 42310	BC847BW
7514	5322 130 42756	BC857C
7515	4822 130 42804	BC817-25
7516	3198 010 42310	BC847BW
7517	5322 130 42756	BC857C
7600	9322 167 63668	IC SM MSP3415G-QG-B8 (MIAS) R
7700	4822 130 61553	DTC124EU
7701	4822 130 61553	DTC124EU
7702	4822 130 61553	DTC124EU
7703	9352 606 11118	IC SM TDA9818T/ V1(PHSE) R
7704	5322 130 42756	BC857C
7705	5322 130 42755	BC847C
7706	5322 130 42756	BC857C
7707	3198 010 42310	BC847BW
7708	4822 130 61553	DTC124EU
7709	3198 010 42310	BC847BW
7800	9322 015 84668	IC SM TL074CD (ST00) R
7801	3198 010 42310	BC847BW
7803	4822 209 16884	
7804	5322 130 42756	BC857C
7805	3198 010 42310	BC847BW
7806	5322 130 42756	BC857C
7807	4822 130 60854	DTA124EU-W
7809	3198 010 42310	BC847BW
7810	4822 209 63604	BA7046F
7811	4822 209 15139	PCF8593T
7812	5322 130 42756	BC857C
7813	3198 010 42310	BC847BW
7815	4822 209 16954	ST24E16M6
7816	3198 010 42310	BC847BW
7817	3198 010 42310	BC847BW
7900	4822 209 16778	TL7705ACD1013TRA
7901	4822 209 73852	PMBT2369
7902	9340 560 36235	FETSIG SM BSH111 (PHSE) R
7906	9322 152 30668	ICSM M29F800AT-70N1(ST00)
7907	9322 161 94668	IC SM CY62128-70SC(CYPR)R
7909	4822 130 61553	DTC124EU
7950	4822 209 60177	LM339D
7951	3198 010 42310	BC847BW
7952	3198 010 42310	BC847BW
7970	4822 209 63709	LM324D
7971	4822 130 44283	BC636
7972	3198 010 42310	BC847BW
7974	3198 010 42310	BC847BW
7975	9340 560 36235	FETSIG SM BSH111 (PHSE) R
7990	4822 209 17505	STV5348D

DIVIO PWB

Various

1101	2422 025 17106	CON BM H 4P F 0.8 IEEE R
1102	2422 543 01115	RES XTL SM 24M576 12P CX-11F R
1200	2422 543 01159	RES XTL SM 11M0592 20P DSX840
1500	2422 025 17084	CON BM V 60P F 0.80 179161 R

2146	4822 126 14305	100nF 10% 16V 0603
2147	4822 126 14305	100nF 10% 16V 0603
2148	4822 126 14305	100nF 10% 16V 0603
2149	4822 126 14305	100nF 10% 16V 0603
2150	4822 126 14305	100nF 10% 16V 0603
2151	4822 126 14305	100nF 10% 16V 0603
2152	4822 126 14305	100nF 10% 16V 0603
2153	4822 126 14305	100nF 10% 16V 0603
2154	4822 126 14305	100nF 10% 16V 0603
2155	4822 126 14305	100nF 10% 16V 0603
2156	4822 126 14305	100nF 10% 16V 0603
2157	4822 126 14305	100nF 10% 16V 0603
2158	3198 017 41050	0603 10V 1μF COL R
2159	3198 017 41050	0603 10V 1μF COL R
2160	3198 017 41050	0603 10V 1μF COL R
2161	2020 557 90731	250V 1nF PM10 R
2162	2020 557 90731	250V 1nF PM10 R
2163	4822 126 14506	270pF 5% 50V 0603
2164	2020 557 90731	250V 1nF PM10 R
2165	2020 557 90731	250V 1nF PM10 R
2166	2020 557 90731	250V 1nF PM10 R
2167	2020 557 90731	250V 1nF PM10 R
2168	2020 557 90731	250V 1nF PM10 R
2169	2020 557 90731	250V 1nF PM10 R
2170	4822 126 11663	12pF
2171	4822 126 11663	12pF
2172	4822 126 14305	100nF 10% 16V 0603
2173	4822 124 23002	10μF 16V
2174	4822 126 14305	100nF 10% 16V 0603
2175	4822 124 23002	10μF 16V
2176	4822 126 14305	100nF 10% 16V 0603
2177	4822 126 14305	100nF 10% 16V 0603
2178	4822 126 14305	100nF 10% 16V 0603
2179	4822 126 14305	100nF 10% 16V 0603
2180	2020 557 90732	250V 4n7 PM10 R
2181	4822 124 12095	100μF 20% 16V
2182	4822 124 23002	10μF 16V
2183	4822 126 14305	100nF 10% 16V 0603
2184	4822 126 14305	100nF 10% 16V 0603
2185	4822 126 14305	100nF 10% 16V 0603
2186	4822 126 14305	100nF 10% 16V 0603
2187	4822 126 14305	100nF 10% 16V 0603
2188	2020 557 90732	250V 4n7 PM10 R
2189	2020 557 90732	250V 4n7 PM10 R
2190	2020 557 90719	1206 B 250V 47nF PM10 R
2200	4822 126 11663	12pF
2201	4822 126 14305	100nF 10% 16V 0603
2202	4822 126 14305	100nF 10% 16V 0603
2203	4822 126 14305	100nF 10% 16V 0603
2204	4822 126 14305	100nF 10% 16V 0603
2205	4822 126 11663	12pF
2206	4822 122 31765	100pF 2% 63V
2207	4822 126 14305	100nF 10% 16V 0603
2300	4822 126 14305	100nF 10% 16V 0603

2301	4822 126 14305	100nF 10% 16V 0603
2302	4822 124 80151	47µF 16V
2303	4822 126 14305	100nF 10% 16V 0603
2304	4822 126 14305	100nF 10% 16V 0603
2305	4822 126 14305	100nF 10% 16V 0603
2306	4822 126 14305	100nF 10% 16V 0603
2307	4822 126 14305	100nF 10% 16V 0603
2308	4822 126 14305	100nF 10% 16V 0603
2309	4822 126 14305	100nF 10% 16V 0603
2310	4822 126 14305	100nF 10% 16V 0603
2311	4822 126 14305	100nF 10% 16V 0603
2312	4822 126 14305	100nF 10% 16V 0603
2313	4822 126 14305	100nF 10% 16V 0603
2314	4822 126 14305	100nF 10% 16V 0603
2315	4822 126 14305	100nF 10% 16V 0603
2316	4822 126 14305	100nF 10% 16V 0603
2317	4822 126 14305	100nF 10% 16V 0603
2318	4822 126 14305	100nF 10% 16V 0603
2319	4822 126 14305	100nF 10% 16V 0603
2320	4822 126 14305	100nF 10% 16V 0603
2321	4822 126 14305	100nF 10% 16V 0603
2322	4822 126 14305	100nF 10% 16V 0603
2323	4822 126 14305	100nF 10% 16V 0603
2324	4822 126 14305	100nF 10% 16V 0603
2325	4822 126 14305	100nF 10% 16V 0603
2326	4822 126 14305	100nF 10% 16V 0603
2327	4822 126 14305	100nF 10% 16V 0603
2328	4822 126 14305	100nF 10% 16V 0603
2329	4822 126 14305	100nF 10% 16V 0603
2330	4822 126 14305	100nF 10% 16V 0603
2331	4822 126 14305	100nF 10% 16V 0603
2400	4822 126 14305	100nF 10% 16V 0603
2401	4822 126 14305	100nF 10% 16V 0603
2402	4822 126 14305	100nF 10% 16V 0603
2403	4822 126 14305	100nF 10% 16V 0603
2404	4822 126 14305	100nF 10% 16V 0603
2405	4822 126 14305	100nF 10% 16V 0603
2406	4822 126 14305	100nF 10% 16V 0603
2407	4822 126 14305	100nF 10% 16V 0603
2408	4822 126 14305	100nF 10% 16V 0603
2409	4822 126 14305	100nF 10% 16V 0603
2410	4822 126 14305	100nF 10% 16V 0603
2411	4822 126 14305	100nF 10% 16V 0603
2412	4822 126 14305	100nF 10% 16V 0603
2413	4822 126 14305	100nF 10% 16V 0603
2414	4822 126 14305	100nF 10% 16V 0603
2415	4822 126 14305	100nF 10% 16V 0603
2416	4822 126 14305	100nF 10% 16V 0603
2417	4822 126 14305	100nF 10% 16V 0603
2418	4822 126 14305	100nF 10% 16V 0603
2419	4822 126 14305	100nF 10% 16V 0603
2420	4822 126 14305	100nF 10% 16V 0603
2421	4822 126 14305	100nF 10% 16V 0603
2500	4822 126 14305	100nF 10% 16V 0603
2501	4822 126 14305	100nF 10% 16V 0603
2502	4822 126 14305	100nF 10% 16V 0603
2503	4822 126 14305	100nF 10% 16V 0603
2504	4822 126 14305	100nF 10% 16V 0603
2505	4822 124 80151	47µF 16V
2506	4822 126 14305	100nF 10% 16V 0603
2507	4822 124 80151	47µF 16V
2508	4822 126 14305	100nF 10% 16V 0603
2509	4822 126 14305	100nF 10% 16V 0603
2510	4822 126 14305	100nF 10% 16V 0603
2511	4822 124 80151	47µF 16V
2512	4822 124 80151	47µF 16V
2514	4822 124 80151	47µF 16V
2515	4822 124 80151	47µF 16V
2516	5322 126 11583	10nF 10% 50V 0603
2517	5322 126 11583	10nF 10% 50V 0603
2518	4822 124 80151	47µF 16V
2519	4822 126 14305	100nF 10% 16V 0603
2520	4822 126 14305	100nF 10% 16V 0603

3100	4822 051 30103	10k 5% 0.062W
3101	4822 051 30103	10k 5% 0.062W
3102	4822 051 30103	10k 5% 0.062W
3104	4822 051 30103	10k 5% 0.062W
3105	4822 051 30332	3k3 5% 0.062W
3106	4822 051 30393	39k 5% 0.062W
3107	4822 051 30393	39k 5% 0.062W
3108	4822 051 30393	39k 5% 0.062W
3109	4822 051 30103	10k 5% 0.062W
3110	4822 051 30103	10k 5% 0.062W
3111	4822 051 30222	2k2 5% 0.062W
3112	4822 051 30391	390Ω 5% 0.062W
3113	4822 051 30103	10k 5% 0.062W
3114	4822 051 20105	1M 5% 0.1W
3115	4822 051 30102	1k 5% 0.062W
3116	4822 051 30479	47Ω 5% 0.062W
3148	2322 704 66342	RST SM 0603 RC22H 6k34 PM1 R
3152	4822 051 30332	3k3 5% 0.062W
3153	4822 051 30393	39k 5% 0.062W
3154	4822 051 30393	39k 5% 0.062W
3155	4822 051 30393	39k 5% 0.062W
3163	4822 051 30391	390Ω 5% 0.062W
3164	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3165	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3166	4822 051 30222	2k2 5% 0.062W
3168	4822 051 30393	39k 5% 0.062W
3169	4822 051 30393	39k 5% 0.062W
3170	4822 051 30393	39k 5% 0.062W
3171	4822 051 30109	10Ω 5% 0.062W
3172	4822 051 30109	10Ω 5% 0.062W
3173	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3174	4822 051 30109	10Ω 5% 0.062W
3175	4822 051 30103	10k 5% 0.062W
3176	4822 051 30109	10Ω 5% 0.062W
3177	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3178	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3179	4822 051 30103	10k 5% 0.062W
3180	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3181	4822 051 30103	10k 5% 0.062W
3182	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3183	4822 051 30103	10k 5% 0.062W
3184	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3185	4822 051 30103	10k 5% 0.062W
3186	4822 051 30103	10k 5% 0.062W
3187	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3188	4822 051 30109	10Ω 5% 0.062W
3189	4822 051 30109	10Ω 5% 0.062W
3190	4822 051 30109	10Ω 5% 0.062W
3191	4822 051 30109	10Ω 5% 0.062W
3191	4822 051 30479	47Ω 5% 0.062W
3192	4822 051 30103	10k 5% 0.062W
3193	4822 051 30393	39k 5% 0.062W
3194	4822 051 30393	39k 5% 0.062W
3195	4822 051 30393	39k 5% 0.062W
3197	4822 051 30103	10k 5% 0.062W
3198	4822 051 30103	10k 5% 0.062W
3199	4822 051 30103	10k 5% 0.062W
3201	4822 051 30479	47Ω 5% 0.062W
3214	4822 051 30102	1k 5% 0.062W
3216	4822 051 30102	1k 5% 0.062W
3224	4822 051 30331	330Ω 5% 0.062W
3300	4822 051 30109	10Ω 5% 0.062W
3301	4822 051 30102	1k 5% 0.062W
3303	4822 051 30102	1k 5% 0.062W
3304	4822 051 30102	1k 5% 0.062W
3305	4822 051 30102	1k 5% 0.062W
3306	4822 051 30102	1k 5% 0.062W
3307	4822 051 30102	1k 5% 0.062W
3312	4822 051 30109	10Ω 5% 0.062W
3313	4822 051 30103	10k 5% 0.062W
3314	4822 051 30103	10k 5% 0.062W
3315	4822 051 30339	33Ω 5% 0.062W
3316	4822 051 30103	10k 5% 0.062W
3317	4822 051 30339	33Ω 5% 0.062W
3318	4822 051 30339	33Ω 5% 0.062W
3319	4822 051 30339	33Ω 5% 0.062W
3320	4822 051 30479	47Ω 5% 0.062W
3321	4822 051 30479	47Ω 5% 0.062W
3322	4822 051 30479	47Ω 5% 0.062W
3325	4822 051 30479	47Ω 5% 0.062W
3327	4822 051 30479	47Ω 5% 0.062W
3328	4822 051 30479	47Ω 5% 0.062W
3400	4822 051 30103	10k 5% 0.062W
3401	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3402	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3403	4822 051 30479	47Ω 5% 0.062W
3404	4822 051 30479	47Ω 5% 0.062W
3405	4822 051 30479	47Ω 5% 0.062W
3502	4822 051 30339	33Ω 5% 0.062W
3504	4822 117 13576	NETW 4 X 33Ω 5% 1206
3505	4822 117 13576	NETW 4 X 33Ω 5% 1206
3506	4822 117 13576	NETW 4 X 33Ω 5% 1206
3518	4822 051 30101	100Ω 5% 0.062W
3519	4822 051 30101	100Ω 5% 0.062W
3520	4822 117 12891	220k 1% ERJ3Ω
3521	4822 117 12891	220k 1% ERJ3Ω
3522	4822 051 30103	10k 5% 0.062W
3523	4822 051 30102	1k 5% 0.062W
3524	4822 051 30109	10Ω 5% 0.062W
3525	4822 051 30339	33Ω 5% 0.062W

5103	4822 157 11499	BLM11P600SPT
5106	4822 157 11499	BLM11P600SPT
5108	4822 157 11499	BLM11P600SPT
5109	4822 157 11499	BLM11P600SPT
5110	4822 157 11499	BLM11P600SPT
5200	4822 157 11499	BLM11P600SPT
5201	4822 157 11499	BLM11P600SPT
5300	4822 157 11499	BLM11P600SPT
5301	4822 157 11499	BLM11P600SPT
5302	4822 157 11499	BLM11P600SPT
5303	4822 157 11499	BLM11P600SPT
5304	4822 157 11499	BLM11P600SPT
5402	4822 157 11499	BLM11P600SPT
5403	4822 157 11499	BLM11P600SPT
5404	4822 157 11499	BLM11P600SPT
5500	4822 157 11499	BLM11P600SPT
5501	4822 157 11499	BLM11P600SPT
5502	4822 157 11499	BLM11P600SPT
5503	4822 157 11499	BLM11P600SPT

6300	4822 209 17398	LD1117DT33

7100	9322 138 58688	OPT CP SM TLP627-LF1 (TOSJ) R
7101	9352 636 86551	IC SM PDI1394P11ABD (PHSE) Y
7103	9352 633 73551	IC SM PDI1394L21BE (PHSE) Y
7105	9322 138 58688	OPT CP SM TLP627-LF1 (TOSJ) R
7106	2722 012 00475	MOD SM HFP143YL05031 (MURA) Y
7200	9351 869 80118	
7201	4822 209 91023	UM62256EM-70LL
7202	9340 310 30215	PDTC144ET (
7203	9352 654 41118	IC SM P89C51RD2HBA/00 (PHSE) R
7204	5322 130 60803	BST72A
7207	9340 310 30215	PDTC144ET (
7208	9352 456 40115	IC SM 74HCT1G04GW (PHSE) R
7300	3104 123 96431	IC OTP EPC1441 ASSY
7301	9322 166 64668	IC SM CY7C1019BV33-10VC(CYPR)R
7302	9322 166 64668	IC SM CY7C1019BV33-10VC(CYPR)R
7303	9322 150 51671	IC SM EPF6024AQC208-3 (ALTO) Y
7304	2422 543 89006	OSC XTL SM 27MHZ 15P FX0-35F R
7305	9322 166 64668	IC SM CY7C1019BV33-10VC(CYPR)R
7306	9322 166 64668	IC SM CY7C1019BV33-10VC(CYPR)R
7307	3104 123 96402	IC FLASH CY2071 AUDIO ASSY
7308	3104 123 96511	IC FLASH CY2071 VIDEO ASSY
7402	4822 209 17375	GM71V18163CJ-6
7403	4822 209 17375	GM71V18163CJ-6
7404	9322 169 98671	IC SM NW701 TQFP160 (DIIN) Y
7500	9352 424 20118	IC SM 74LVC04APW (PHSE) R
7505	9352 351 50118	IC SM 74LVC16244ADGG (PHSE) R
7506	9352 668 39118	IC SM UDA1334ATS/N2 (PHSE) R

SERVO PWB

Various

1100	2422 025 16143	CON BM H 45P F 0.5 54132 R
1100	2422 025 17425	CON BM H45P F 0.5 54132R
1201	2422 540 98428	RES CER SM 8M467 CSTCC8.46MHz R
1300	4822 267 51454	CONN. 11P FEMALE
1302	2422 025 16158	CON BM H 8P F 1.00 FFC 0.3 R
1303	2422 025 17427	CON BM H 4P F 1.00 FFC 0.3 R

1401	2422 540 98428	RES CER SM 8M467 CSTCC8.46MHz R
1402	2422 025 17276	CON BM H 30P F 1.00 FFC SMT R

2002	5322 126 11583	10nF 10% 50V 0603
2003	4822 124 23002	10µF 16V
2004	5322 126 11583	10nF 10% 50V 0603
2005	4822 124 23002	10µF 16V
2008	5322 126 11583	10nF 10% 50V 0603
2009	4822 124 23002	10µF 16V
2010	5322 126 11583	10nF 10% 50V 0603
2011	4822 124 23002	10µF 16V
2012	5322 126 11583	10nF 10% 50V 0603
2013	4822 124 23002	10µF 16V
2014	4822 124 12084	1µF 20% SM 50V
2015	4822 126 14305	100nF 10% 16V 0603
2016	4822 124 23002	10µF 16V
2017	5322 126 11583	10nF 10% 50V 0603
2018	4822 126 14305	100nF 10% 16V 0603
2019	4822 124 23002	10µF 16V
2020	4822 126 14305	100nF 10% 16V 0603
2100	4822 126 14305	100nF 10% 16V 0603
2102	4822 126 14305	100nF 10% 16V 0603
2104	5322 126 11583	10nF 10% 50V 0603
2105	5322 126 11583	10nF 10% 50V 0603
2106	4822 122 33735	27nF 10% 63V
2110	4822 126 14305	100nF 10% 16V 0603
2111	4822 126 14305	100nF 10% 16V 0603
2116	4822 126 14305	100nF 10% 16V 0603
2121	5322 126 11579	3.3nF 10% 63V
2122	5322 126 11582	6.8nF 10% 63V
2125	5322 126 11583	10nF 10% 50V 0603
2200	4822 126 14305	100nF 10% 16V 0603
2202	4822 126 14305	100nF 10% 16V 0603
2203	4822 124 23002	10µF 16V
2207	4822 126 14305	100nF 10% 16V 0603
2208	4822 126 14305	100nF 10% 16V 0603
2209	4822 126 14305	100nF 10% 16V 0603
2210	4822 126 14305	100nF 10% 16V 0603
2211	4822 126 14305	100nF 10% 16V 0603
2212	5322 126 11583	10nF 10% 50V 0603
2214	4822 126 14305	100nF 10% 16V 0603
2218	4822 126 14305	100nF 10% 16V 0603
2219	4822 126 14305	100nF 10% 16V 0603
2220	4822 126 14305	100nF 10% 16V 0603
2221	4822 126 14305	100nF 10% 16V 0603
2222	4822 126 14305	100nF 10% 16V 0603
2223	4822 126 14305	100nF 10% 16V 0603
2224	4822 126 14305	100nF 10% 16V 0603
2225	4822 126 14305	100nF 10% 16V 0603
2226	4822 126 14305	100nF 10% 16V 0603
2227	4822 126 14305	100nF 10% 16V 0603
2228	4822 126 14305	100nF 10% 16V 0603
2232	4822 126 14305	100nF 10% 16V 0603
2233	4822 122 33753	150pF 5% 50V
2234	4822 122 33753	150pF 5% 50V
2235	4822 126 14305	100nF 10% 16V 0603
2236	4822 126 14305	100nF 10% 16V 0603
2237	4822 126 14305	100nF 10% 16V 0603
2238	4822 126 14305	100nF 10% 16V 0603
2300	5322 126 11583	10nF 10% 50V 0603
2301	4822 124 23002	10µF 16V
2302	3198 017 34730	0603 16V 47nF COL
2303	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2304	5322 126 11583	10nF 10% 50V 0603
2305	4822 124 23002	10µF 16V
2309	3198 016 31020	0603 25V 1nF
2310	3198 016 31020	0603 25V 1nF
2311	4822 126 14494	22nF 10% 25V 0603
2312	2238 786 11554	0603 16V 2N2 PM5 R
2313	4822 126 14305	100nF 10% 16V 0603
2314	3198 016 31020	0603 25V 1nF
2315	4822 126 14305	100nF 10% 16V 0603
2316	4822 126 14305	100nF 10% 16V 0603
2317	5322 126 11583	10nF 10% 50V 0603
2318	3198 016 31020	0603 25V 1nF
2319	4822 126 14305	100nF 10% 16V 0603
2320	3198 016 31020	0603 25V 1nF
2321	3198 016 31020	0603 25V 1nF
2322	4822 126 14305	100nF 10% 16V 0603
2323	4822 126 14494	22nF 10% 25V 0603
2324	5322 124 41945	22µF 20% 35V
2325	4822 126 14305	100nF 10% 16V 0603
2326	3198 017 31530	0603 50V 15nF COL R
2327	4822 126 14305	100nF 10% 16V 0603
2328	3198 017 31530	0603 50V 15nF COL R
2329	4822 126 14305	100nF 10% 16V 0603
2331	4822 126 14305	100nF 10% 16V 0603
2332	4822 126 14305	100nF 10% 16V 0603
2333	5322 124 41945	22µF 20% 35V
2334	4822 126 14305	100nF 10% 16V 0603
2335	2238 786 11554	0603 16V 2N2 PM5 R
2336	3198 017 34730	0603 16V 47nF COL
2337	3198 017 34730	0603 16V 47nF COL
2338	2238 786 11554	0603 16V 2N2 PM5 R
2339	4822 124 23002	10µF 16V
2400	4822 124 23002	10µF 16V
2401	5322 126 11583	10nF 10% 50V 0603
2402	4822 126 14305	100nF 10% 16V 0603
2403	4822 126 14305	100nF 10% 16V 0603
2404	4822 126 14494	22nF 10% 25V 0603
2405	4822 126 14494	22nF 10% 25V 0603
2406	4822 126 14305	100nF 10% 16V 0603
2407	4822 126 14305	100nF 10% 16V 0603
2409	4822 126 14305	100nF 10% 16V 0603
2410	4822 122 33777	47pF 5% 63V
2411	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2412	4822 126 14494	22nF 10% 25V 0603
2413	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2414	4822 126 14238	0603 50V 2N2 COL R
2421	4822 122 33761	22pF 5% 50V
2422	4822 126 14305	100nF 10% 16V 0603
2423	4822 126 14305	100nF 10% 16V 0603
2424	4822 126 14305	100nF 10% 16V 0603
2425	4822 126 14305	100nF 10% 16V 0603
2426	4822 126 14305	100nF 10% 16V 0603
2427	4822 126 14305	100nF 10% 16V 0603
2428	4822 126 14305	100nF 10% 16V 0603
2429	4822 126 14305	100nF 10% 16V 0603
2430	4822 126 14305	100nF 10% 16V 0603
2431	4822 126 14305	100nF 10% 16V 0603
2432	4822 126 14305	100nF 10% 16V 0603
2434	4822 122 33741	10pF 10% 50V
2435	4822 122 33761	22pF 5% 50V
2436	4822 122 33761	22pF 5% 50V
2437	4822 122 33761	22pF 5% 50V
2438	4822 122 33761	22pF 5% 50V
2439	4822 122 33761	22pF 5% 50V
2440	4822 122 33761	22pF 5% 50V
2441	4822 122 33761	22pF 5% 50V
2446	5322 126 11583	10nF 10% 50V 0603

3005	4822 051 30121	120Ω 5% 0.062W
3006	2322 704 64309	RST SM 0603 RC22H 43Ω PM1
3100	4822 051 30103	10k 5% 0.062W
3103	5322 117 13029	47k 1% 0.063W 0603 RC22H
3105	4822 051 30681	680Ω 5% 0.062W
3107	4822 051 30101	100Ω 5% 0.062W
3108	4822 051 30101	100Ω 5% 0.062W
3114	4822 051 30101	100Ω 5% 0.062W
3115	4822 051 30101	100Ω 5% 0.062W
3121	4822 051 30681	680Ω 5% 0.062W
3122	4822 051 30152	1k5 5% 0.062W
3129	4822 051 30154	150k 5% 0.062W
3130	4822 051 30101	100Ω 5% 0.062W
3200	4822 051 30103	10k 5% 0.062W
3201	4822 051 30103	10k 5% 0.062W
3204	4822 117 12917	1Ω 5% 0.062W CASE0603
3205	4822 051 30103	10k 5% 0.062W
3210	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3214	4822 051 30103	10k 5% 0.062W
3216	4822 051 30103	10k 5% 0.062W
3217	4822 051 30103	10k 5% 0.062W
3221	4822 051 30472	4k7 5% 0.062W
3222	4822 051 30103	10k 5% 0.062W
3224	4822 051 30105	1M 5% 0.062W
3225	4822 051 30331	330Ω 5% 0.062W
3226	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3227	4822 117 13525	24k 1% 0.62W RC22H 0603
3231	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3235	4822 051 30103	10k 5% 0.062W
3236	4822 051 30103	10k 5% 0.062W
3237	4822 051 30223	22k 5% 0.062W
3238	4822 051 30222	2k2 5% 0.062W
3241	4822 051 30103	10k 5% 0.062W
3244	4822 051 30103	10k 5% 0.062W
3245	4822 051 30472	4k7 5% 0.062W
3246	4822 051 30479	47Ω 5% 0.062W
3249	4822 051 30103	10k 5% 0.062W
3250	4822 051 30479	47Ω 5% 0.062W
3251	4822 051 30222	2k2 5% 0.062W
3252	4822 051 30222	2k2 5% 0.062W
3253	4822 051 30273	27k 5% 0.062W
3254	4822 051 30273	27k 5% 0.062W
3255	4822 051 30273	27k 5% 0.062W
3256	4822 051 30273	27k 5% 0.062W
3257	4822 051 30273	27k 5% 0.062W
3258	4822 051 30273	27k 5% 0.062W
3259	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3260	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3261	4822 051 30103	10k 5% 0.062W
3262	4822 117 11817	1k2 1% 1/16W
3264	4822 117 13632	100k 1% 0603 0.62W
3265	4822 117 13632	100k 1% 0603 0.62W
3266	4822 051 30103	10k 5% 0.062W
3267	4822 051 30103	10k 5% 0.062W
3268	4822 051 30103	10k 5% 0.062W
3269	4822 051 30102	1k 5% 0.062W
3270	4822 051 30102	1k 5% 0.062W
3271	4822 051 30102	1k 5% 0.062W
3272	4822 051 30103	10k 5% 0.062W
3274	4822 051 30103	10k 5% 0.062W
3275	4822 051 30103	10k 5% 0.062W
3276	4822 051 30103	10k 5% 0.062W
3300	4822 051 30272	2k7 5% 0.062W
3302	4822 051 30272	2k7 5% 0.062W
3303	4822 051 30102	1k 5% 0.062W
3304	4822 051 30102	1k 5% 0.062W
3305	4822 117 13608	4.7Ω 5% 0603 0.0016W
3307	5322 117 13068	82Ω 1% 0.063W 0603 RC22H
3308	4822 051 20108	1Ω 5% 0.1W
3309	4822 051 20108	1Ω 5% 0.1W
3310	4822 117 12917	1Ω 5% 0.062W CASE0603
3311	4822 117 12917	1Ω 5% 0.062W CASE0603
3312	4822 117 12917	1Ω 5% 0.062W CASE0603
3314	4822 051 20108	1Ω 5% 0.1W
3315	4822 051 20108	1Ω 5% 0.1W
3316	4822 051 20228	2Ω2 5% 0.1W
3317	4822 051 20228	2Ω2 5% 0.1W
3318	4822 051 20228	2Ω2 5% 0.1W
3319	4822 051 20228	2Ω2 5% 0.1W
3320	4822 051 30332	3k3 5% 0.062W
3321	4822 051 30563	56k 5% 0.062W
3323	4822 051 30222	2k2 5% 0.062W
3324	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
3325	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
3326	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
3327	4822 051 30103	10k 5% 0.062W
3328	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
3329	4822 117 13632	100k 1% 0603 0.62W
3330	4822 051 30332	3k3 5% 0.062W
3331	4822 051 30103	10k 5% 0.062W
3332	2322 704 62003	RST SM 0603 RC22H 20k PM1 R
3335	5322 117 13068	82Ω 1% 0.063W 0603 RC22H
3336	4822 117 12864	82k 5% 0.6W
3337	4822 051 30273	27k 5% 0.062W
3338	4822 051 30103	10k 5% 0.062W
3339	4822 117 12864	82k 5% 0.6W
3340	4822 051 30332	3k3 5% 0.062W
3341	4822 051 30102	1k 5% 0.062W
3342	4822 051 30273	27k 5% 0.062W
3343	4822 051 30103	10k 5% 0.062W
3344	4822 051 30332	3k3 5% 0.062W
3345	4822 051 30102	1k 5% 0.062W
3346	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
3347	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
3348	4822 117 13632	100k 1% 0603 0.62W
3351	4822 051 30472	4k7 5% 0.062W
3352	4822 051 30153	15k 5% 0.062W
3353	4822 051 30123	12k 5% 0.062W
3354	4822 117 11817	1k2 1% 1/16W
3355	4822 051 30332	3k3 5% 0.062W
3356	4822 051 30472	4k7 5% 0.062W
3357	4822 117 13632	100k 1% 0603 0.62W
3358	4822 051 30102	1k 5% 0.062W
3359	2322 704 62002	RST SM 0603 RC22H 2k PM1 R
3361	4822 051 30563	56k 5% 0.062W
3362	4822 051 30103	10k 5% 0.062W
3364	4822 051 30272	2k7 5% 0.062W
3365	4822 051 30272	2k7 5% 0.062W
3366	4822 051 30471	470Ω 5% 0.062W
3368	4822 051 30471	470Ω 5% 0.062W
3370	4822 051 30103	10k 5% 0.062W
3400	4822 117 11817	1k2 1% 1/16W
3401	2350 035 10152	RST NETW SM ARV24 4X1k5 PM5 R
3407	4822 117 13525	24k 1% 0.62W RC22H 0603
3408	4822 051 30103	10k 5% 0.062W

3409	4822 051 30183	18k 5% 0.062W
3410	2350 035 10152	RST NETW SM ARV24 4X1k5 PM5 R
3411	4822 117 12139	22Ω 5% 0.062W
3415	4822 051 30101	100Ω 5% 0.062W
3416	4822 051 30105	1M 5% 0.062W
3417	4822 051 30331	330Ω 5% 0.062W
3418	4822 117 13578	4X10k 5% MNR14
3419	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3420	2350 035 91001	RST NETW SM ARV24 4X jumper R
3430	4822 117 13578	4X10k 5% MNR14
3431	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3439	4822 051 30109	10Ω 5% 0.062W
3440	4822 051 30109	10Ω 5% 0.062W
3448	2350 035 91001	RST NETW SM ARV24 4X jumper R
3449	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3450	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3451	4822 117 11817	1k2 1% 1/16W
3461	4822 051 30102	1k 5% 0.062W
3463	4822 051 30101	100Ω 5% 0.062W
3468	4822 051 30101	100Ω 5% 0.062W
3469	4822 051 30101	100Ω 5% 0.062W

5100	4822 157 11074	100μH
5102	4822 157 11074	100μH
5104	4822 157 11074	100μH
5200	4822 157 11074	100μH
5201	2422 549 43769	IND FXD SM EMI 100mH z 30R R
5202	2422 549 43769	IND FXD SM EMI 100mH z 30R R
5203	2422 549 43769	IND FXD SM EMI 100mH z 30R R
5300	2422 549 43769	IND FXD SM EMI 100mH z 30R R
5301	2422 549 43769	IND FXD SM EMI 100mH z 30R R
5302	2422 549 43769	IND FXD SM EMI 100mH z 30R R
5400	4822 157 11074	100μH
5401	4822 157 11074	100μH
5402	2422 549 43769	IND FXD SM EMI 100mH z 30R R

6301	4822 130 11397	BAS316

7000	9322 150 89668	IC SM LM337D2T (ONSE) R
7001	9322 121 67668	IC SM LF33CD (ST00) R
7101	9352 688 06157	IC SM TZA1031HL (PHSE) Y
7200	4822 130 60373	BC856B
7201	9322 155 26685	IC SM ADM810SART (ANA0) Y
7202	3104 123 96450	IC FLASH BASIC ENGINE DVD+RW
7203	9352 687 34557	IC SM SAA7830HL (PHSE) Y
7204	9322 036 99685	CY7C1399-15ZC
7205	4822 130 60373	BC856B
7206	3104 123 96541	IC EPLD BASIC ENGINE
7301	9322 139 85668	BA6665FM
7302	4822 209 17229	BA5938FM
7304	4822 209 30095	LM833D
7306	9322 166 66668	IC SM BA5944FP (RHM0) R
7308	9340 547 21215	FET POW SM BSH205 (PHSE) R
7309	4822 130 60511	BC847B
7310	4822 130 60511	BC847B
7311	4822 130 60511	BC847B
7312	9322 144 97668	IC SM LD1117DT (ST00) R
7400	5322 209 30676	TDA8703T/C4
7401	9322 171 97671	IC SM UPD65943GC-081 (NEC0) Y
7402	9352 687 36557	IC SM SAA7831HL (PHSE) Y

ACCESSORIES

Various

0318	3104 207 10652	IRT PROD ASSY RC2050/01 PACKED
0320	4822 321 22611	AUDIO CORD GOLD PLATED
0321	3104 128 92490	VIDEO CORD SET GOLD PLATED
0322	2422 070 98133	MAINSCORD EUR
0322	4622 001 60590	MAINSCORD UK
0323	4822 321 61847	SCART CABLE
0324	3111 170 21592	CORDON ANT. L.1,50M
0370	4822 321 61849	S-VIDEO CORD

DIGITAL PWB

Various

1100	2422 025 17018	CON BM V 15P F 1.00 FFC 0.3 R
1101	2422 025 17018	CON BM V 15P F 1.00 FFC 0.3 R
1200	2422 025 16957	CON BM V 24P F 1.00 FFC 0.3 R
1501	2422 025 16939	CON BM V 60P F 0.80 84616 R
1600	2422 025 16729	CON BM V 10P F 1.00 FFC 0.3 R
1601	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1602	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R

2100	4822 126 14305	100nF 10% 16V 0603
2101	4822 126 14305	100nF 10% 16V 0603
2102	4822 126 14305	100nF 10% 16V 0603
2103	4822 126 14305	100nF 10% 16V 0603
2104	4822 126 14305	100nF 10% 16V 0603
2105	4822 126 14305	100nF 10% 16V 0603
2106	4822 126 14305	100nF 10% 16V 0603
2107	4822 126 14305	100nF 10% 16V 0603
2108	4822 126 14305	100nF 10% 16V 0603
2109	4822 126 14305	100nF 10% 16V 0603
2110	4822 126 14305	100nF 10% 16V 0603
2111	4822 126 14305	100nF 10% 16V 0603
2112	4822 126 14305	100nF 10% 16V 0603
2113	4822 126 14305	100nF 10% 16V 0603
2114	4822 126 14305	100nF 10% 16V 0603
2115	4822 126 14305	100nF 10% 16V 0603
2116	4822 126 14305	100nF 10% 16V 0603
2117	4822 126 14305	100nF 10% 16V 0603
2118	4822 126 14305	100nF 10% 16V 0603
2119	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2120	4822 126 14305	100nF 10% 16V 0603
2121	4822 126 14305	100nF 10% 16V 0603
2122	4822 126 14305	100nF 10% 16V 0603
2123	4822 126 14305	100nF 10% 16V 0603
2124	4822 126 14305	100nF 10% 16V 0603
2125	4822 126 14305	100nF 10% 16V 0603
2126	4822 126 14305	100nF 10% 16V 0603
2127	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2128	4822 126 14494	22nF 10% 25V 0603
2129	4822 126 14305	100nF 10% 16V 0603
2202	4822 126 14305	100nF 10% 16V 0603
2203	4822 124 12095	100μF 20% 16V
2207	4822 124 23002	10μF 16V
2208	4822 126 14305	100nF 10% 16V 0603
2209	5322 126 11579	3.3nF 10% 63V
2210	4822 126 14241	0603 50V 330P COL R
2211	4822 126 14305	100nF 10% 16V 0603
2212	4822 126 14305	100nF 10% 16V 0603
2213	4822 126 14305	100nF 10% 16V 0603
2214	4822 126 14305	100nF 10% 16V 0603
2215	4822 126 14305	100nF 10% 16V 0603
2216	4822 126 14305	100nF 10% 16V 0603
2217	4822 126 14305	100nF 10% 16V 0603
2218	4822 126 14305	100nF 10% 16V 0603
2219	4822 126 14305	100nF 10% 16V 0603
2220	4822 126 14305	100nF 10% 16V 0603
2221	4822 126 14305	100nF 10% 16V 0603
2222	4822 126 14305	100nF 10% 16V 0603
2223	4822 126 14305	100nF 10% 16V 0603
2224	4822 126 14305	100nF 10% 16V 0603
2225	4822 126 14305	100nF 10% 16V 0603
2226	4822 126 14305	100nF 10% 16V 0603
2227	4822 126 14305	100nF 10% 16V 0603
2228	4822 126 14305	100nF 10% 16V 0603
2229	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2230	4822 126 14305	100nF 10% 16V 0603
2231	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2241	3198 016 31020	0603 25V 1nF
2300	4822 126 14305	100nF 10% 16V 0603
2301	4822 126 14305	100nF 10% 16V 0603
2302	4822 126 14305	100nF 10% 16V 0603
2303	4822 126 14305	100nF 10% 16V 0603
2304	4822 126 14305	100nF 10% 16V 0603
2305	4822 126 14305	100nF 10% 16V 0603
2306	4822 126 14305	100nF 10% 16V 0603
2307	4822 126 14305	100nF 10% 16V 0603
2308	4822 126 14305	100nF 10% 16V 0603
2309	4822 126 14305	100nF 10% 16V 0603
2310	4822 126 14305	100nF 10% 16V 0603
2311	4822 126 14305	100nF 10% 16V 0603
2312	4822 126 14305	100nF 10% 16V 0603
2313	4822 126 14305	100nF 10% 16V 0603
2314	4822 126 14305	100nF 10% 16V 0603
2315	4822 126 14305	100nF 10% 16V 0603
2316	4822 126 14305	100nF 10% 16V 0603
2317	4822 126 14305	100nF 10% 16V 0603
2318	4822 126 14305	100nF 10% 16V 0603
2319	4822 126 14305	100nF 10% 16V 0603
2320	4822 124 12095	100μF 20% 16V
2321	4822 124 12095	100μF 20% 16V
2322	4822 124 12095	100μF 20% 16V
2323	4822 126 14305	100nF 10% 16V 0603
2400	4822 126 14305	100nF 10% 16V 0603
2401	4822 126 14305	100nF 10% 16V 0603
2402	4822 126 14305	100nF 10% 16V 0603
2403	4822 126 14305	100nF 10% 16V 0603
2404	4822 126 14305	100nF 10% 16V 0603
2405	4822 126 14305	100nF 10% 16V 0603
2406	4822 126 14305	100nF 10% 16V 0603
2407	4822 126 14305	100nF 10% 16V 0603
2408	4822 126 14305	100nF 10% 16V 0603
2409	4822 126 14305	100nF 10% 16V 0603
2410	4822 126 14305	100nF 10% 16V 0603
2411	4822 126 14305	100nF 10% 16V 0603
2412	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2413	4822 126 14305	100nF 10% 16V 0603
2414	4822 126 14305	100nF 10% 16V 0603
2415	4822 126 14305	100nF 10% 16V 0603
2416	4822 126 14305	100nF 10% 16V 0603
2417	4822 126 14305	100nF 10% 16V 0603
2418	4822 126 14305	100nF 10% 16V 0603
2419	4822 126 14305	100nF 10% 16V 0603
2420	4822 126 14305	100nF 10% 16V 0603
2421	4822 126 14305	100nF 10% 16V 0603
2422	4822 126 14305	100nF 10% 16V 0603
2423	4822 126 14305	100nF 10% 16V 0603
2424	4822 126 14305	100nF 10% 16V 0603
2425	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2426	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2550	4822 126 14305	100nF 10% 16V 0603
2551	4822 126 14305	100nF 10% 16V 0603
2552	4822 126 14305	100nF 10% 16V 0603
2553	4822 126 14305	100nF 10% 16V 0603
2554	4822 126 14305	100nF 10% 16V 0603
2555	4822 126 14305	100nF 10% 16V 0603
2556	4822 126 14305	100nF 10% 16V 0603
2557	4822 126 14305	100nF 10% 16V 0603
2558	4822 126 14305	100nF 10% 16V 0603
2559	4822 122 33761	22pF 5% 50V
2560	4822 122 33761	22pF 5% 50V
2561	4822 126 14305	100nF 10% 16V 0603
2562	4822 126 14305	100nF 10% 16V 0603
2563	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2564	4822 126 14305	100nF 10% 16V 0603
2565	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2566	4822 126 14305	100nF 10% 16V 0603
2567	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2568	4822 126 14305	100nF 10% 16V 0603
2569	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2570	4822 126 14305	100nF 10% 16V 0603
2571	4822 126 14305	100nF 10% 16V 0603
2572	4822 126 14305	100nF 10% 16V 0603
2573	4822 126 14305	100nF 10% 16V 0603
2574	4822 126 14305	100nF 10% 16V 0603
2575	4822 126 14305	100nF 10% 16V 0603
2576	4822 126 14305	100nF 10% 16V 0603

2577	4822 126 14305	100nF 10% 16V 0603
2578	4822 126 14305	100nF 10% 16V 0603
2579	4822 126 14305	100nF 10% 16V 0603
2580	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2581	4822 126 14305	100nF 10% 16V 0603
2582	4822 126 14305	100nF 10% 16V 0603
2583	4822 126 14305	100nF 10% 16V 0603
2584	4822 126 14305	100nF 10% 16V 0603
2585	4822 126 14305	100nF 10% 16V 0603
2586	4822 126 14305	100nF 10% 16V 0603
2587	4822 126 14305	100nF 10% 16V 0603
2588	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2589	4822 126 14305	100nF 10% 16V 0603
2590	4822 126 14305	100nF 10% 16V 0603
2591	4822 126 14305	100nF 10% 16V 0603
2592	4822 126 14305	100nF 10% 16V 0603
2593	4822 126 14305	100nF 10% 16V 0603
2594	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2595	4822 126 14305	100nF 10% 16V 0603
2596	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2600	4822 126 14305	100nF 10% 16V 0603
2601	4822 122 33777	47pF 5% 63V
2602	4822 122 33777	47pF 5% 63V
2603	4822 126 14305	100nF 10% 16V 0603
2605	4822 126 14305	100nF 10% 16V 0603
2606	4822 122 33777	47pF 5% 63V
2607	4822 122 33777	47pF 5% 63V
2608	4822 126 14305	100nF 10% 16V 0603
2609	4822 126 14305	100nF 10% 16V 0603
2610	4822 126 14305	100nF 10% 16V 0603
2611	4822 122 33777	47pF 5% 63V
2612	4822 122 33777	47pF 5% 63V
2613	4822 126 14305	100nF 10% 16V 0603
2614	4822 126 14305	100nF 10% 16V 0603
2615	4822 126 14305	100nF 10% 16V 0603
2616	4822 122 33777	47pF 5% 63V
2617	4822 122 33777	47pF 5% 63V
2618	4822 126 14305	100nF 10% 16V 0603
2619	4822 126 14305	100nF 10% 16V 0603
2620	4822 126 14305	100nF 10% 16V 0603
2621	4822 122 33777	47pF 5% 63V
2622	4822 122 33777	47pF 5% 63V
2625	4822 126 14305	100nF 10% 16V 0603
2626	4822 122 33777	47pF 5% 63V
2627	4822 122 33777	47pF 5% 63V
2628	4822 126 14305	100nF 10% 16V 0603
2629	4822 126 14305	100nF 10% 16V 0603
2630	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2633	4822 126 14305	100nF 10% 16V 0603
2634	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2637	4822 126 14305	100nF 10% 16V 0603
2642	4822 122 33761	22pF 5% 50V
2643	4822 122 33761	22pF 5% 50V
2644	4822 122 33761	22pF 5% 50V
2645	4822 126 14305	100nF 10% 16V 0603
2646	4822 126 14494	22nF 10% 25V 0603
2647	4822 126 14247	0603 50V 1N5 COL R
2648	4822 126 14247	0603 50V 1N5 COL R
2700	5322 126 11583	10nF 10% 50V 0603
2701	3198 017 44740	0603 10V 470nF COL
2702	4822 126 14305	100nF 10% 16V 0603
2703	4822 126 14305	100nF 10% 16V 0603
2704	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2705	4822 124 12084	1µF 20% SM 50V
2706	4822 126 14305	100nF 10% 16V 0603
2707	4822 124 12084	1µF 20% SM 50V
2708	4822 126 14305	100nF 10% 16V 0603
2709	4822 124 12084	1µF 20% SM 50V
2710	4822 126 14305	100nF 10% 16V 0603
2711	4822 124 12084	1µF 20% SM 50V
2712	4822 126 14305	100nF 10% 16V 0603
2713	4822 126 14305	100nF 10% 16V 0603
2800	4822 126 14305	100nF 10% 16V 0603
2801	4822 126 14305	100nF 10% 16V 0603
2802	4822 126 14305	100nF 10% 16V 0603
2803	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2804	4822 126 14305	100nF 10% 16V 0603
2805	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2806	4822 126 14305	100nF 10% 16V 0603
2807	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2808	4822 126 14305	100nF 10% 16V 0603
2809	4822 126 14305	100nF 10% 16V 0603
2813	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2814	4822 126 14305	100nF 10% 16V 0603
2818	5322 124 41945	22µF 20% 35V
2819	4822 126 13956	68pF 5% 63V CASE 0603
2821	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2900	4822 126 14305	100nF 10% 16V 0603
2901	4822 126 14305	100nF 10% 16V 0603
2902	4822 126 14305	100nF 10% 16V 0603
2903	4822 126 14305	100nF 10% 16V 0603
2904	4822 126 14305	100nF 10% 16V 0603
2912	4822 122 33741	10pF 10% 50V
2914	4822 122 33741	10pF 10% 50V
2916	4822 122 33741	10pF 10% 50V
2917	4822 122 33741	10pF 10% 50V
2918	4822 122 33741	10pF 10% 50V
2919	4822 122 33741	10pF 10% 50V
2920	4822 122 33761	22pF 5% 50V
2921	4822 126 14305	100nF 10% 16V 0603
2922	4822 126 14305	100nF 10% 16V 0603
2923	4822 126 14305	100nF 10% 16V 0603
2924	4822 126 14305	100nF 10% 16V 0603
2925	4822 126 14305	100nF 10% 16V 0603
3100	4822 051 30103	10k 5% 0.062W
3101	4822 051 30222	2k2 5% 0.062W
3102	4822 051 30472	4k7 5% 0.062W
3104	4822 051 30109	10Ω 5% 0.062W
3105	4822 051 30109	10Ω 5% 0.062W
3106	4822 051 30109	10Ω 5% 0.062W
3107	4822 051 30109	10Ω 5% 0.062W
3108	4822 051 30109	10Ω 5% 0.062W
3109	4822 051 30109	10Ω 5% 0.062W
3110	4822 051 30109	10Ω 5% 0.062W
3111	4822 051 30472	4k7 5% 0.062W
3112	4822 051 30472	4k7 5% 0.062W
3113	4822 051 30472	4k7 5% 0.062W
3114	4822 051 30472	4k7 5% 0.062W
3115	4822 051 30103	10k 5% 0.062W
3116	4822 051 30103	10k 5% 0.062W
3117	4822 051 30222	2k2 5% 0.062W
3119	4822 051 30479	47Ω 5% 0.062W
3120	4822 051 30479	47Ω 5% 0.062W
3121	4822 117 13576	NETW 4 X 33Ω 5% 1206
3122	4822 117 13576	NETW 4 X 33Ω 5% 1206
3123	4822 117 12917	1Ω 5% 0.062W CASE0603
3124	4822 117 12917	1Ω 5% 0.062W CASE0603
3125	4822 117 12917	1Ω 5% 0.062W CASE0603
3126	4822 117 12917	1Ω 5% 0.062W CASE0603
3200	4822 051 30332	3k3 5% 0.062W
3201	5322 117 13068	82Ω 1% 0.063W 0603 RC22H
3205	4822 051 30101	100Ω 5% 0.062W
3206	4822 051 30101	100Ω 5% 0.062W
3207	4822 051 30103	10k 5% 0.062W
3208	5322 117 13068	82Ω 1% 0.063W 0603 RC22H
3209	4822 117 13578	4X10k 5% MNR14
3210	4822 117 12917	1Ω 5% 0.062W CASE0603
3211	4822 051 30222	2k2 5% 0.062W
3212	3198 031 11010	RST NETW 1206 4X100Ω PM5 COL R
3213	3198 031 11010	RST NETW 1206 4X100Ω PM5 COL R
3214	4822 051 30101	100Ω 5% 0.062W
3215	4822 051 30101	100Ω 5% 0.062W
3216	4822 051 30109	10Ω 5% 0.062W
3217	4822 051 30101	100Ω 5% 0.062W
3218	4822 051 30101	100Ω 5% 0.062W
3221	4822 117 12139	22Ω 5% 0.062W
3236	4822 051 30152	1k5 5% 0.062W
3237	4822 051 30152	1k5 5% 0.062W
3238	4822 051 30332	3k3 5% 0.062W
3240	4822 051 30332	3k3 5% 0.062W
3241	4822 051 30103	10k 5% 0.062W
3242	4822 051 30103	10k 5% 0.062W
3243	4822 051 30103	10k 5% 0.062W
3250	4822 051 30103	10k 5% 0.062W
3251	4822 051 30332	3k3 5% 0.062W
3252	4822 051 30103	10k 5% 0.062W
3253	4822 051 30332	3k3 5% 0.062W
3254	4822 051 30103	10k 5% 0.062W
3263	4822 051 30103	10k 5% 0.062W
3264	4822 051 30103	10k 5% 0.062W
3266	4822 051 30221	220Ω 5% 0.062W
3267	4822 051 30103	10k 5% 0.062W
3269	4822 117 12706	10k 1% 0.063W CASE0603 RC22H
3270	5322 117 13033	15k 1% 0.063W 0603 RC22H
3272	5322 117 13047	330Ω 1% 0.063W 0603 RC22H
3273	5322 117 13051	680Ω 1% 0.063W 0603 RC22H
3304	4822 051 30103	10k 5% 0.062W
3305	4822 051 30103	10k 5% 0.062W
3400	4822 051 30472	4k7 5% 0.062W
3401	4822 051 30472	4k7 5% 0.062W
3402	4822 051 30472	4k7 5% 0.062W
3403	4822 051 30103	10k 5% 0.062W
3405	4822 051 30101	100Ω 5% 0.062W
3406	4822 051 30101	100Ω 5% 0.062W
3407	4822 051 30339	33Ω 5% 0.062W
3408	4822 117 13576	NETW 4 X 33Ω 5% 1206
3409	4822 117 13576	NETW 4 X 33Ω 5% 1206
3410	4822 117 13576	NETW 4 X 33Ω 5% 1206
3552	4822 051 30101	100Ω 5% 0.062W
3553	4822 051 30101	100Ω 5% 0.062W
3554	4822 117 12917	1Ω 5% 0.062W CASE0603
3555	4822 051 30103	10k 5% 0.062W
3556	4822 051 30222	2k2 5% 0.062W
3557	4822 051 30472	4k7 5% 0.062W
3559	4822 051 30103	10k 5% 0.062W
3560	4822 051 30103	10k 5% 0.062W
3561	4822 051 30222	2k2 5% 0.062W
3562	4822 051 30472	4k7 5% 0.062W
3563	4822 051 30008	0Ω jumper
3601	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3602	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3603	4822 051 30102	1k 5% 0.062W
3604	4822 117 12139	22Ω 5% 0.062W
3605	4822 117 12917	1Ω 5% 0.062W CASE0603
3606	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3607	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3608	4822 051 30102	1k 5% 0.062W
3610	4822 117 12917	1Ω 5% 0.062W CASE0603
3611	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3612	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3613	4822 051 30102	1k 5% 0.062W
3616	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3617	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3618	4822 051 30102	1k 5% 0.062W
3619	4822 051 30109	10Ω 5% 0.062W
3621	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3622	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3624	4822 051 30102	1k 5% 0.062W
3626	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3627	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3628	4822 051 30102	1k 5% 0.062W
3629	4822 051 30181	180Ω 5% 0.062W
3630	4822 051 30181	180Ω 5% 0.062W
3631	4822 117 12917	1Ω 5% 0.062W CASE0603
3632	4822 051 30561	560Ω 5% 0.062W
3633	4822 051 30561	560Ω 5% 0.062W
3641	4822 117 12139	22Ω 5% 0.062W
3642	4822 051 30101	100Ω 5% 0.062W
3643	4822 051 30101	100Ω 5% 0.062W
3644	4822 051 30101	100Ω 5% 0.062W
3645	4822 051 30222	2k2 5% 0.062W
3646	4822 051 30181	180Ω 5% 0.062W
3647	4822 051 30561	560Ω 5% 0.062W
3648	4822 051 30101	100Ω 5% 0.062W
3649	4822 051 30101	100Ω 5% 0.062W
3650	4822 117 13632	100k 1% 0603 0.62W
3651	4822 051 30103	10k 5% 0.062W
3652	4822 051 30682	6k8 5% 0.062W
3653	4822 117 13632	100k 1% 0603 0.62W
3654	4822 051 30101	100Ω 5% 0.062W
3655	4822 117 13632	100k 1% 0603 0.62W
3656	4822 051 30103	10k 5% 0.062W
3657	4822 051 30682	6k8 5% 0.062W
3700	4822 051 30103	10k 5% 0.062W
3701	4822 051 30103	10k 5% 0.062W
3702	4822 051 30103	10k 5% 0.062W
3703	4822 051 30222	2k2 5% 0.062W
3704	4822 051 30103	10k 5% 0.062W
3705	4822 051 30103	10k 5% 0.062W
3706	4822 051 30103	10k 5% 0.062W
3707	4822 051 30101	100Ω 5% 0.062W
3708	4822 051 30101	100Ω 5% 0.062W
3709	4822 051 30103	10k 5% 0.062W
3710	4822 051 30103	10k 5% 0.062W
3711	4822 051 30103	10k 5% 0.062W
3712	4822 051 30103	10k 5% 0.062W

3713	4822 051 30472	4k7 5% 0.062W
3714	4822 051 30472	4k7 5% 0.062W
3715	4822 051 30102	1k 5% 0.062W
3716	4822 051 30103	10k 5% 0.062W
3717	4822 051 30103	10k 5% 0.062W
3718	4822 051 30103	10k 5% 0.062W
3719	4822 117 13576	NETW 4 X 33Ω 5% 1206
3720	4822 117 13576	NETW 4 X 33Ω 5% 1206
3721	4822 117 13576	NETW 4 X 33Ω 5% 1206
3722	4822 117 13576	NETW 4 X 33Ω 5% 1206
3723	4822 117 13576	NETW 4 X 33Ω 5% 1206
3724	4822 051 30339	33Ω 5% 0.062W
3725	4822 051 30339	33Ω 5% 0.062W
3800	4822 051 30103	10k 5% 0.062W
3802	4822 051 30759	75Ω 5% 0.062W
3803	4822 051 30121	120Ω 5% 0.062W
3804	4822 117 12917	1Ω 5% 0.062W CASE0603
3805	2322 704 62002	RST SM 0603 RC22H 2k PM1 R
3806	4822 117 12139	22Ω 5% 0.062W
3807	5322 117 13068	82Ω 1% 0.063W 0603 RC22H
3809	4822 051 30123	12k 5% 0.062W
3810	2322 704 63002	RST SM 0603 RC22H 3k PM1 R
3811	4822 117 12891	220k 1% ERJ3Ω
3812	4822 117 12139	22Ω 5% 0.062W
3814	5322 117 13033	15k 1% 0.063W 0603 RC22H
3815	4822 051 30222	2k2 5% 0.062W
3816	4822 117 12925	47k 1% 0.063W 0603
3817	4822 117 13632	100k 1% 0603 0.62W
3818	4822 117 12139	22Ω 5% 0.062W
3819	5322 117 13068	82Ω 1% 0.063W 0603 RC22H
3820	2120 611 00019	NTC SM 0603 0W1 4k7 PM5 R
3900	4822 051 30103	10k 5% 0.062W
3901	4822 051 30101	100Ω 5% 0.062W
3902	4822 051 30101	100Ω 5% 0.062W
3906	4822 117 12925	47k 1% 0.063W 0603
3907	4822 117 12925	47k 1% 0.063W 0603
3908	4822 117 12925	47k 1% 0.063W 0603
3911	4822 051 30101	100Ω 5% 0.062W
3912	4822 051 30101	100Ω 5% 0.062W
3913	4822 051 30103	10k 5% 0.062W
3914	4822 051 30479	47Ω 5% 0.062W
3915	4822 051 30479	47Ω 5% 0.062W
3916	4822 051 30479	47Ω 5% 0.062W
3917	4822 051 30479	47Ω 5% 0.062W
3918	4822 051 30479	47Ω 5% 0.062W
3919	4822 051 30479	47Ω 5% 0.062W
3920	4822 051 30479	47Ω 5% 0.062W
3921	4822 051 30479	47Ω 5% 0.062W
3922	4822 051 30479	47Ω 5% 0.062W
3923	4822 051 30479	47Ω 5% 0.062W
3924	4822 051 30479	47Ω 5% 0.062W
3925	4822 051 30479	47Ω 5% 0.062W
3926	4822 051 30479	47Ω 5% 0.062W
3927	4822 051 30479	47Ω 5% 0.062W
3928	4822 051 30222	2k2 5% 0.062W
3929	4822 117 12925	47k 1% 0.063W 0603

5100	4822 157 11717	BLM31P500SPT
5101	4822 157 11717	BLM31P500SPT
5102	4822 157 11499	BLM11P600SPT
5103	4822 157 11717	BLM31P500SPT
5200	4822 157 11717	BLM31P500SPT
5201	4822 157 70649	4.7μH (NL322522T-4R7J)
5202	4822 157 70649	4.7μH (NL322522T-4R7J)
5300	4822 157 11499	BLM11P600SPT
5301	4822 157 11499	BLM11P600SPT
5302	4822 157 11499	BLM11P600SPT
5400	4822 157 11499	BLM11P600SPT
5402	4822 157 11499	BLM11P600SPT
5404	4822 157 11499	BLM11P600SPT
5550	2422 543 01115	RES XTL SM 24M576 12P CX-11F R
5552	4822 157 11499	BLM11P600SPT
5553	4822 157 11499	BLM11P600SPT
5554	4822 157 11499	BLM11P600SPT
5555	4822 157 11499	BLM11P600SPT
5556	4822 157 11499	BLM11P600SPT
5557	4822 157 11499	BLM11P600SPT
5558	4822 157 11499	BLM11P600SPT
5559	4822 157 11499	BLM11P600SPT
5560	4822 157 11499	BLM11P600SPT
5600	4822 157 70298	15μH (NL322522T-150J)
5601	4822 157 11717	BLM31P500SPT
5602	4822 157 11717	BLM31P500SPT
5605	4822 157 70298	15μH (NL322522T-150J)
5606	4822 157 70649	4.7μH (NL322522T-4R7J)
5607	4822 157 70649	4.7μH (NL322522T-4R7J)
5610	4822 157 70298	15μH (NL322522T-150J)
5615	4822 157 70298	15μH (NL322522T-150J)
5620	4822 157 70298	15μH (NL322522T-150J)
5625	4822 157 70298	15μH (NL322522T-150J)
5700	4822 157 11499	BLM11P600SPT
5701	4822 157 11717	BLM31P500SPT
5801	4822 157 11499	BLM11P600SPT
5802	4822 157 11499	BLM11P600SPT
5803	4822 157 11499	BLM11P600SPT
5805	4822 157 11499	BLM11P600SPT
5807	4822 157 11499	BLM11P600SPT
5813	4822 157 11499	BLM11P600SPT
5900	4822 157 11717	BLM31P500SPT
5901	4822 157 11717	BLM31P500SPT

7100	9352 692 48557	IC SM SAA7333HL/M1 (PHSE) Y
7101	9322 144 96668	IC SM MT48LC4M16A2TG-8E (MRN)R
7102	9322 170 16685	IC SM NC7SZ58 (FSC0) R
7103	9352 456 80115	
7200	9322 130 41668	IC SM M24C64-WMN6 (ST00) R
7202	9322 151 16671	STI5505AVC
7300	4822 209 17375	GM71V18163CJ-6
7301	4822 209 17375	GM71V18163CJ-6
7305	9352 499 60118	IC SM 74LVC00AD (PHSE) R
7306	9322 144 59668	IC SM MT48LC1M16A1TG-7S (MRN)R
7307	9322 144 59668	IC SM MT48LC1M16A1TG-7S (MRN)R
7400	4822 209 17375	GM71V18163CJ-6
7401	4822 209 17375	GM71V18163CJ-6
7402	4822 209 17375	GM71V18163CJ-6
7403	4822 209 17375	GM71V18163CJ-6
7410	9352 378 90557	IC SM SAA6750H/V1 (PHSE) Y
7551	9352 500 60118	IC SM 74LVC32AD (PHSE) R
7552	9352 673 95518	IC SM SAA7118E/V1 (PHSE) R
7553	5322 130 60803	BST72A
7554	5322 130 60803	BST72A
7600	4822 130 60511	BC847B
7601	9352 456 80115	
7602	5322 209 71568	PC74HCT14T
7606	4822 130 60511	BC847B
7610	4822 130 60511	BC847B
7615	4822 130 60511	BC847B
7620	4822 130 60511	BC847B
7625	4822 130 60511	BC847B
7644	4822 130 60511	BC847B
7700	9322 166 64668	IC SM CY7C1019BV33-10VC(CYPR)R
7701	9322 166 64668	IC SM CY7C1019BV33-10VC(CYPR)R
7702	9322 166 64668	IC SM CY7C1019BV33-10VC(CYPR)R
7703	9322 131 98671	IC SM DSP56362-80 (MOTA) Y
7704	2422 543 01185	OSC XTL SM 8MHZ00 15P FX0-31 R
7800	9322 151 71668	IC SM MK2703STR (MICL) R
7801	4822 209 16399	74LVC04AD
7802	4822 242 10838	27MHZ 120P FX0-31FT
7803	4822 130 60511	BC847B
7806	5322 209 16384	PC74HCT9046AD
7900	5322 209 11578	PCF8574T
7901	9352 456 50115	HC1G04
7913	4822 209 16318	MC33464N-30A
7916	9352 317 00118	IC
7917	5322 209 11578	PCF8574T
7918	9352 500 20118	IC SM 74LVC08AD (PHSE) R

PSU 50PS203

Various

0010	4822 492 63066	
0021	4822 492 63066	
0025	4822 492 63524	FIX. TRANSISTOR
0040	4822 492 63066	
0060	4822 492 63066	
0090	4822 492 63066	
0101▲	4822 265 31015	
0120▲	4822 265 11253	FUSE HOLDER 2P
1120▲	4822 253 30383	19181 (2,5A)
1520▲	4822 252 11144	19398E1(3,150A)

2119▲	2020 554 90186	CERSAF KX 250V S 1nF PM20 A
2120▲	4822 121 10697	220nF 20% 275V
2125	2222 151 90053	EL 151 400V S 68μF PM20
2129	4822 121 70162	10nF 5% 400V
2130	4822 126 14525	47pF 5% 1KV
2131▲	2020 554 90186	CERSAF KX 250V S 1nF PM20 A
2136	4822 126 12263	220pF 10%) 1KV
2139	2222 580 15649	100nF 10% 50V
2140	2222 580 15649	100nF 10% 50V
2141	4822 126 13881	470pF 5% 50V
2142	4822 122 33575	220pF 5% 63V CASE
2143	4822 126 14305	100nF 10% 16V 0603
2144	4822 126 14583	470nF 10% 16V XTR
2145	4822 126 14583	470nF 10% 16V XTR
2146	5322 122 34099	470pF 10% 63V
2147	4822 124 40248	10μF 20% 63V
2151	2222 580 15649	100nF 10% 50V
2152	4822 126 14241	0603 50V 330P COL R
2153	4822 126 13694	68pF 1% 63V
2200	4822 124 11566	47μF 20% 50V
2201	2222 580 15649	100nF 10% 50V
2210	2020 021 91657	EL YXG 16V S 680μF PM20 B
2211	4822 124 40255	100μF 20% 63V
2214	4822 124 12285	2200μF 20% 16V YXG EL
2220	4822 124 80144	220μF 20% 25V
2221	4822 124 40255	100μF 20% 63V
2223	2222 580 15649	100nF 10% 50V
2230	4822 124 40255	100μF 20% 63V
2235	2020 012 93762	EL YK 50V S 330μF PM20 B
2240	2020 021 91664	EL YXG 16V S 1000μF PM20 B
2241	4822 124 40255	100μF 20% 63V
2251	4822 126 14494	22nF 10% 25V 0603
2501	4822 126 14494	22nF 10% 25V 0603
2502	4822 124 40255	100μF 20% 63V
2506	4822 124 40255	100μF 20% 63V
2511	4822 126 14305	100nF 10% 16V 0603
2512	4822 124 40255	100μF 20% 63V
2513	2222 580 15649	100nF 10% 50V
2515	4822 124 40255	100μF 20% 63V
2520	4822 126 14494	22nF 10% 25V 0603
2521	4822 124 40255	100μF 20% 63V

3120▲	2122 550 00147	VDR DC 1M A/423V S MAX 775V B
3122▲	4822 053 21684	680k 5% 0.5W
3125	4822 116 83866	1M 5% 0.5W
3126	4822 116 83866	1M 5% 0.5W
3127	4822 116 83874	220k 5% 0.5W
3128	4822 116 83874	220k 5% 0.5W
3131	4822 116 52195	47Ω 5% 0.5W
3132	4822 116 52195	47Ω 5% 0.5W
3133	4822 116 80676	1Ω5 5% 0.5W
3134	4822 116 80676	1Ω5 5% 0.5W
3135	4822 116 80676	1Ω5 5% 0.5W
3139	4822 117 13632	100k 1% 0603 0.62W
3140	4822 051 30272	2k7 5% 0.062W
3141	4822 116 52257	22k 5% 0.5W
3142	4822 051 30221	220Ω 5% 0.062W
3143	4822 051 30102	1k 5% 0.062W
3144	4822 051 30102	1k 5% 0.062W
3145	4822 051 20223	22k 5% 0.1W
3146	4822 116 52175	100Ω 5% 0.5W
3147	4822 051 30222	2k2 5% 0.062W
3148	4822 116 52256	2k2 5% 0.5W
3149	4822 116 52256	2k2 5% 0.5W
3150	4822 053 10689	68Ω 5% 1W
3151	4822 117 13632	100k 1% 0603 0.62W
3152	4822 116 52261	24k 5% 0.5W
3200	4822 116 52263	2k7 5% 0.5W
3201	4822 051 20333	33k 5% 0.1W
3220	4822 051 30222	2k2 5% 0.062W
3221	4822 051 30223	22k 5% 0.062W
3222	4822 051 30472	4k7 5% 0.062W
3223	4822 116 52283	4k7 5% 0.5W
3230▲	4822 052 10479	47Ω 5% 0.33W
3233	4822 117 10833	10k 1% 0.1W
3234	4822 117 10833	10k 1% 0.1W
3250	4822 116 83883	470Ω 5% 0.5W

3253	4822 117 12925	47k 1% 0.063W 0603
3254	4822 116 83883	470Ω 5% 0.5W
3255	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3256	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3501	4822 116 52256	2k2 5% 0.5W
3502	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3503	4822 051 30681	680Ω 5% 0.062W
3504	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3511	4822 051 30103	10k 5% 0.062W
3512	4822 051 20472	4k7 5% 0.1W
3513	4822 117 12925	47k 1% 0.063W 0603
3514	4822 050 21003	10k 1% 0.6W
3515	4822 117 10833	10k 1% 0.1W
3516	4822 051 30103	10k 5% 0.062W
3520	4822 051 20511	510Ω 5% 0.1W
3521	4822 051 30102	1k 5% 0.062W
3522	4822 117 11449	2k2 5% 0.1W 0805
3523	4822 051 30681	680Ω 5% 0.062W
3524	4822 051 20332	3k3 5% 0.1W
3525	5322 117 13036	1k2 1% 0.063W 0603 RC22H

5110	2422 535 94634	IND FXD LHL08 S 2U2 PM20 A
5115	2422 535 94634	IND FXD LHL08 S 2U2 PM20 A
5120▲	4822 157 11846	
5125	4822 157 70826	2.4μH
5131▲	4822 146 10402	TRAFO CT395FANF/PVF
5210	2422 535 94639	IND FXD LHL08 S 10U PM20
5240	2422 535 94632	IND FXD LHL08 S 1U PM30 A
5501	2422 535 94634	IND FXD LHL08 S 2U2 PM20 A
5505	2422 535 94639	IND FXD LHL08 S 10U PM20
5511	2422 535 94639	IND FXD LHL08 S 10U PM20
5515	2422 535 94639	IND FXD LHL08 S 10U PM20
5520	2422 535 94634	IND FXD LHL08 S 2U2 PM20 A

6125	4822 130 42606	BYD33J
6130	5322 130 34574	1N4004G
6131	5322 130 34574	1N4004G
6132	5322 130 34574	1N4004G
6140	4822 130 30842	BAV21
6141	4822 130 83757	BAS216
6142	4822 130 30842	BAV21
6143	4822 130 30842	BAV21
6144	9340 387 30115	DIO REG SM BZX284-C16 (PHSE) R
6145	4822 130 83757	BAS216
6146	4822 130 83757	BAS216
6151	4822 130 31603	1N4006
6152	4822 130 31603	1N4006
6153	4822 130 31603	1N4006
6154	4822 130 31603	1N4006
6200	4822 130 42606	BYD33J
6201	4822 130 34142	BZX79-B33
6210	4822 130 11596	BYW29EX-200
6211	5322 130 34574	1N4004G
6215	9322 161 46687	DIO REC STPS745FP (ST00) L
6220	5322 130 31938	BYV27-200
6221	4822 130 30842	BAV21
6230	4822 130 42606	BYD33J
6231	4822 130 34142	BZX79-B33
6240	4822 130 11596	BYW29EX-200
6505	4822 130 32245	BYV10-40
6511	4822 130 11666	BZX284-C8V2
6512	5322 130 34574	1N4004G
6515	4822 130 34278	BZX79-B6V8
6520	4822 130 83757	BAS216

7125	9322 126 65687	STP5NB60FP
7140	5322 130 60159	BC846B
7141	4822 130 60373	BC856B
7142	5322 130 60159	BC846B
7143	5322 130 60159	BC846B
7200▲	9322 149 04682	OPT CP TCET1102(G) (VISH) L
7220	4822 209 72684	L7905CV
7241	4822 130 60373	BC856B
7251	4822 209 81397	TL431CLPST
7501	9322 163 53685	FET POW SM IRLML2502 (INR0) R
7502	4822 209 81397	TL431CLPST
7511	9322 163 53685	FET POW SM IRLML2502 (INR0) R
7512	5322 130 60159	BC846B
7515	9322 163 53685	FET POW SM IRLML2502 (INR0) R
7520	4822 130 11336	STP16NE06FP
7521	4822 209 81397	TL431CLPST